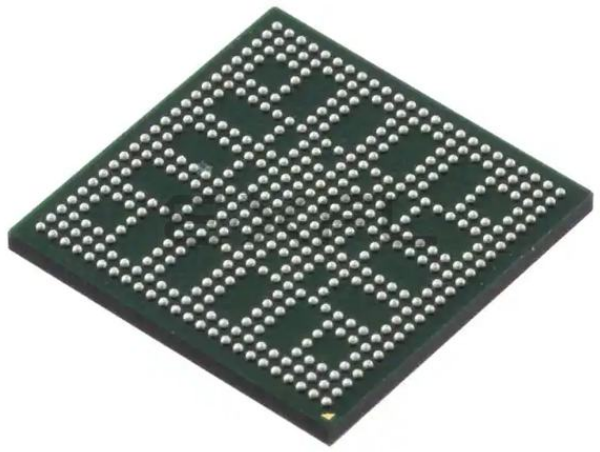

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l3dvn10ab

The i.MX 6SoloLite processor features:

- Applications processor—The processor enhances the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processor has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: 2D BLit engine, a 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—The processor supports connections to a variety of interfaces: LCD controller, CMOS sensor interface (parallel), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Mbps Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Electronic Paper Display Controller—The processor integrates EPD controller that supports E-INK color and monochrome with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh and 5-bit grayscale (32-levels per color channel). The processor also integrates an EPD controller that supports SiPix monochrome panels.
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6SoloLite security reference manual. Contact your local Freescale representative for more information.
- Integrated power management—The processor integrates linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.
- GPIO with interrupt capabilities—The new GPIO pad design supports configurable dual voltage rails at 1.8V and 3.3V supplies. The pad is configurable to interface at either voltage level.

Table 4. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-Chip Termination
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 18
Operating Ranges	on page 21
External Clock Sources	on page 22
Maximal Supply Currents	on page 23
Low Power Mode Supply Currents	on page 24
USB PHY Current Consumption	on page 26

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6SoloLite Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDD_ARM_IN and VDD_SOC_IN are connected to different external supply sources, then VDD_ARM_IN supply must be turned ON together with VDD_SOC_IN supply or not delayed more than 1 ms.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6SoloLite reference manual for further details and to ensure that all necessary requirements are being met.

Table 19. ARM PLL's Electrical Parameters (continued)

Parameter	Value
Reference clock	24 MHz
Lock time	<2250 reference cycles (50 μs)

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. It also implements a power mux such that the oscillator can be powered from VDD1P1 or VDD_SOC. VDD_1P1 should be the cleaner supply and is the preferable choice, but if the oscillator is needed to run in "stop mode" then it is necessary to run from VDD_SOC, which is 0.9 V in stop mode.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

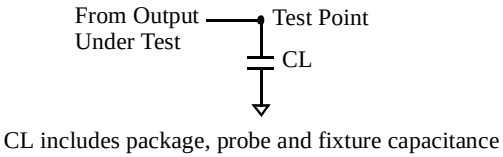

Figure 5. Load Circuit for Output

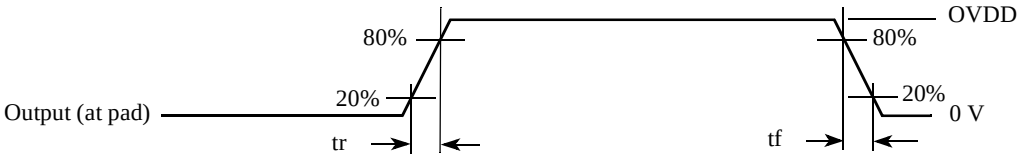

Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.8.3 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 32 shows DDR I/O output buffer impedance of i.MX 6SoloLite processor.

Table 32. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	 Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloLite processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 33 lists the timing parameters.

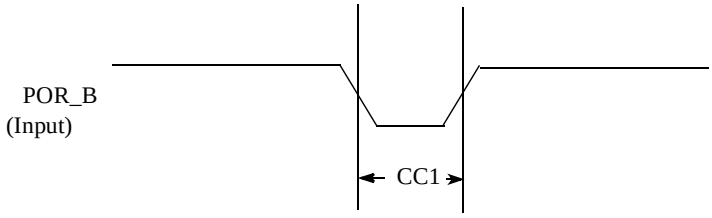

Figure 8. Reset Timing Diagram

Table 33. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope <= 5 ns)	1	—	XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 34 lists the timing parameters.

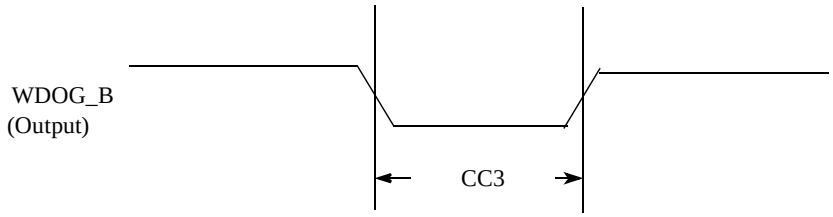

Figure 9. WDOG_B Timing Diagram

Table 34. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	XTALI cycle

NOTE

XTALI is approximately 32 kHz. XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 37 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

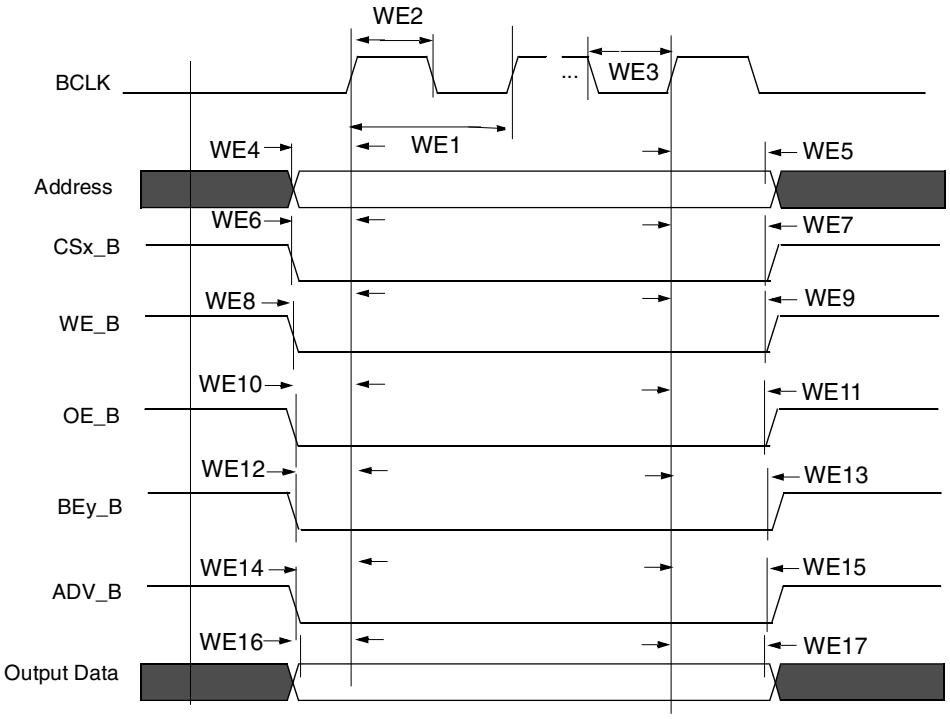

Figure 10. EIM Output Timing Diagram

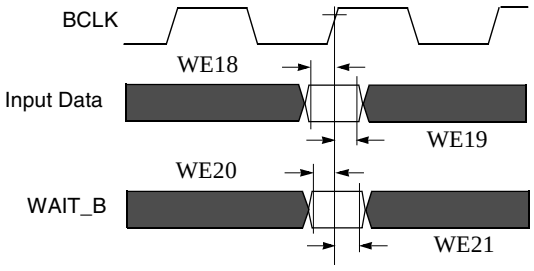

Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 37. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	BCLK cycle time[2]	t*(k+1)	—	ns
WE2	BCLK high level width	0.4*t*(k+1)	—	ns

Figure 24 shows the DDR3 read timing diagram. The timing parameters for this diagram appear in Table 41.

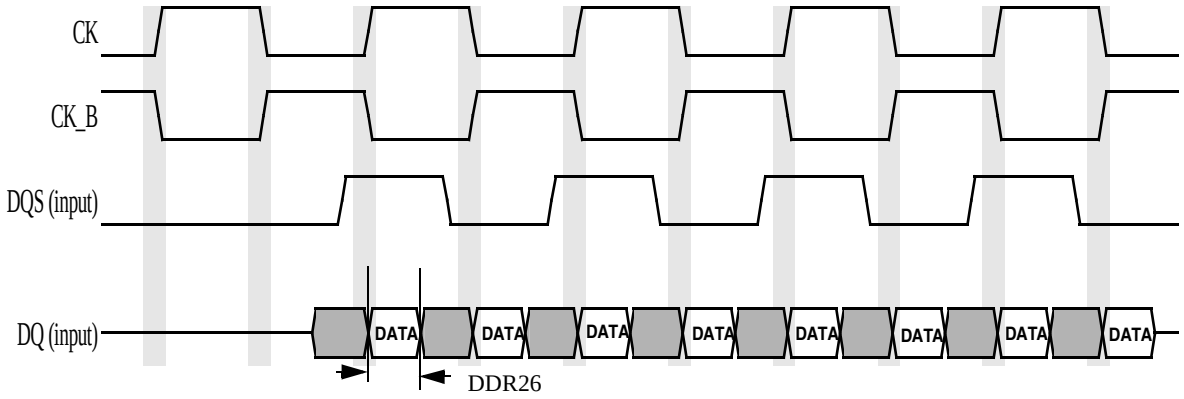

Figure 24. DDR3 Read Cycle

Table 41. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	—	450	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Table 47. ECSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS3	SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 3	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2	ns
CS8	MISO Setup Time	t_{Smiso}	8.5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow include:

ECSPI2/EPDC_SDLE, ECSPI3/EPDC_D9, ECSPI4/EPDC_D1

2 ECSPI fast include:

ECSPI1/LCD_DAT1, ECSPI1/ECSPI1_MISO, ECSPI2/LCD_DAT10, ECSPI2/ECSPI2_MISO, ECSPI3/AUD_TXC, ECSPI3/SD2_DAT1, ECSPI4/KEY_ROW1, ECSPI4/FEC_CRS_DV

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

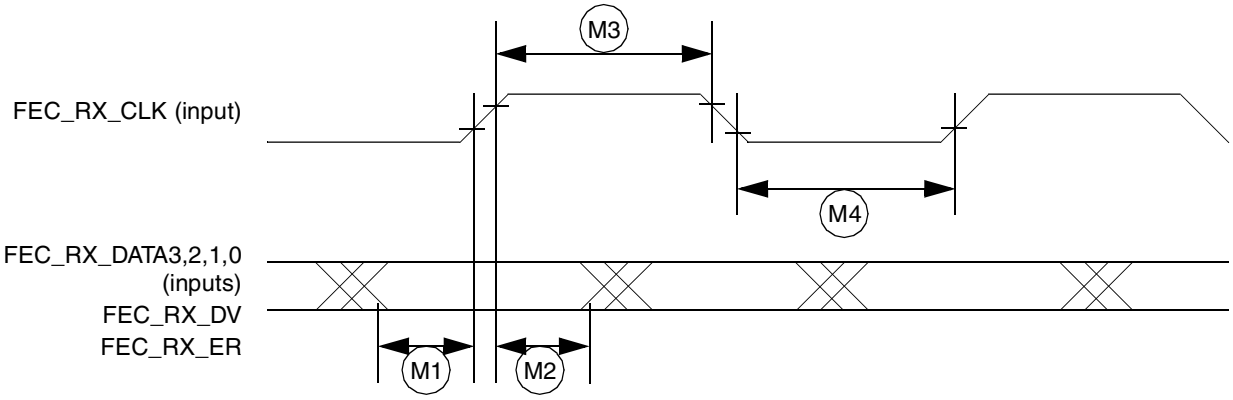

Figure 36. MII Receive Signal Timing Diagram

4.10.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 53 lists MII transmit channel timing parameters. Figure 37 shows MII transmit signal timing diagram for the values listed in Table 53.

Table 53. MII Transmit Signal Timing

Num	Characteristic[1] [2]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

1 FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

2 Test conditions: 25pF on each output signal.

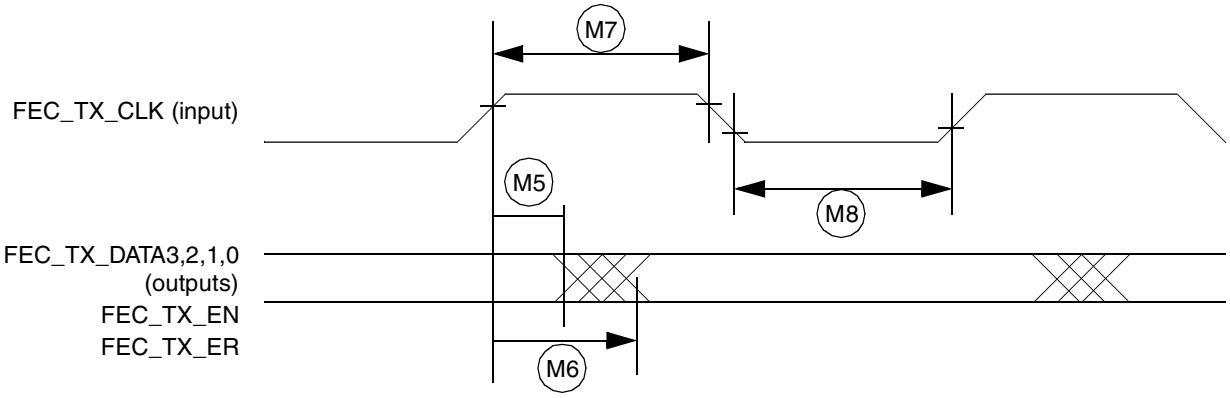

Figure 37. MII Transmit Signal Timing Diagram

4.10.5.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 54 lists MII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 54.

Table 54. MII Async Inputs Signal Timing

Num	Characteristic [1]	Min	Max	Unit
M9[2]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

1 Test conditions: 25pF on each output signal.

2 FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

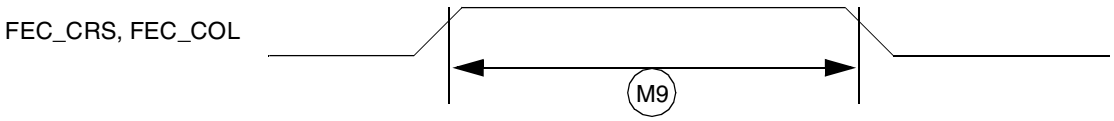

Figure 38. MII Async Inputs Timing Diagram

4.10.5.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 55 lists MII serial management channel timings. Figure 39 shows MII serial management channel timings listed in Table 55. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 55. MII Transmit Signal Timing

ID	Characteristics[1]	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns

Table 55. MII Transmit Signal Timing (continued)

ID	Characteristics[1]	Min	Max	Unit
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40 %	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40 %	60%	FEC_MDC period

1 Test conditions: 25pF on each output signal.

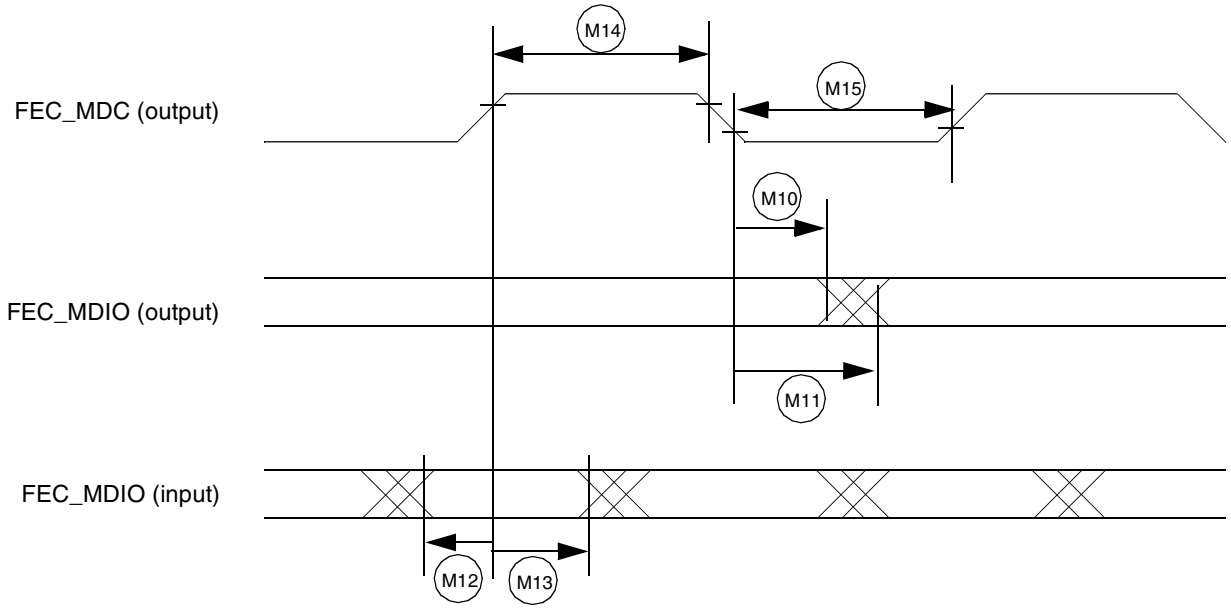

Figure 39. MII Serial Management Channel Timing Diagram

4.10.5.5 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 56 and Figure 40.

Table 56. RMII Signal Timing

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns

Table 56. RMII Signal Timing (continued)

No.	Characteristics[1]	Min	Max	Unit
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

1 Test conditions: 25pF on each output signal.

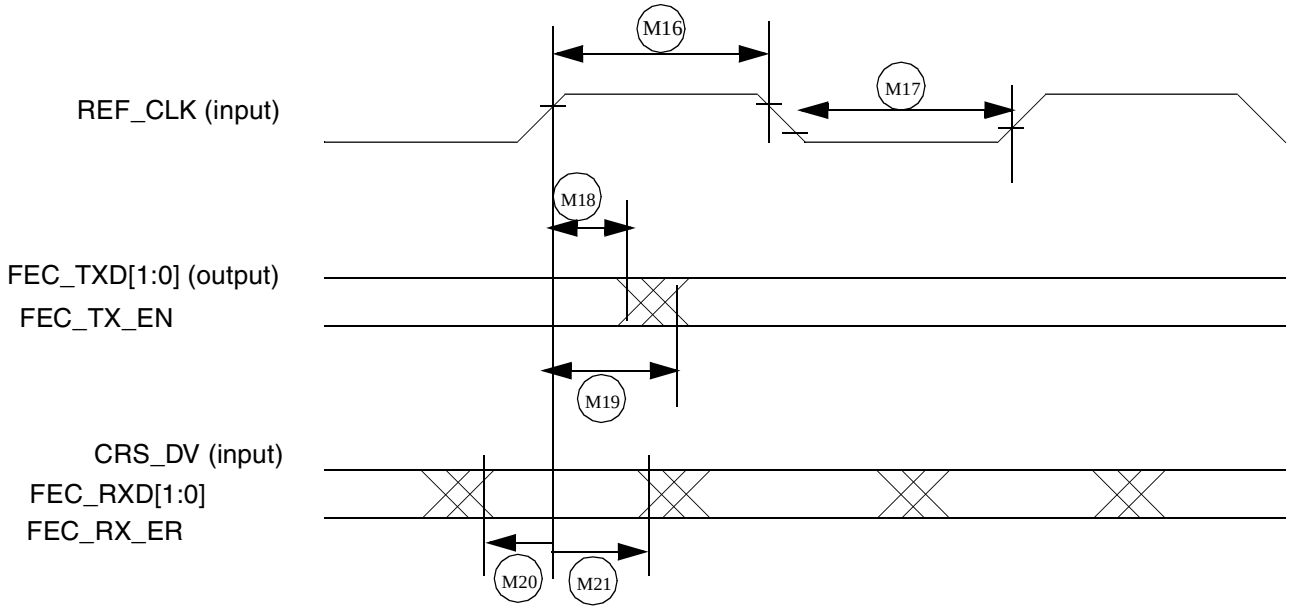

Figure 40. RMII Mode Signal Timing Diagram

4.10.6 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 57 lists the I²C module timing characteristics.

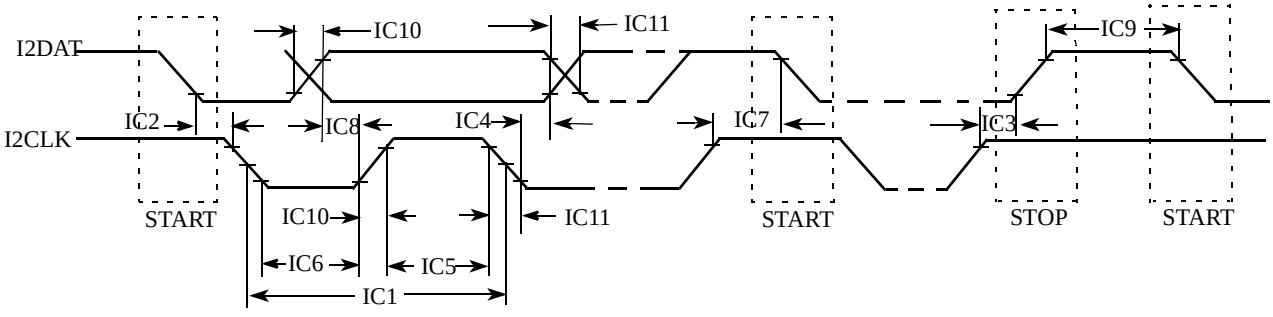

Figure 41. I²C Bus Timing

Table 62. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 76 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloLite Fuse Map document and the System Boot chapter of the i.MX 6SoloLite reference manual.

Table 76. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
TAMPER	Y18	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_TD1	Input	
TEST_MODE	U15	VDD_SNVS_IN	GPIO	ALT0	Reserved—Factory Use Only	Input	
UART1_RXD	B19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[16]	Input	Keeper
UART1_TXD	D19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[17]	Input	Keeper
USB_OTG_CHD_B	AC22	USB_OTG_VBUS	ANALOG		USB_OTG_CHD_B	—	—
USB_OTG1_DN	AD19	USB_OTG_VBUS	ANALOG		USB_OTG1_DN	—	—
USB_OTG1_DP	AC19	USB_OTG_VBUS	ANALOG		USB_OTG1_DP	—	—
USB_OTG2_DN	AD17	USB_OTG_VBUS	ANALOG		USB_OTG2_DN	—	—
USB_OTG2_DP	AC17	USB_OTG_VBUS	ANALOG		USB_OTG2_DP	—	—
WDOG_B	F18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[18]	Input	Keeper
XTALI	AD21	NVCC_PLL	ANALOG		XTALI	—	—
XTALO	AC21	NVCC_PLL	ANALOG		XTALO	—	—
ZQPAD	H2	NVCC_DRAM	ZQPAD		ZQPAD	Input	Hi-Z

[1] The state immediately after reset and before ROM firmware or software has executed.

6.1.3 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 81 shows the MAPBGA 13 x 13mm, 0.5 mm pitch ball map.

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD
24	GND	KEY_ROW7	KEY_ROW6	KEY_COL5	KEY_ROW2	KEY_ROW1	KEY_ROW0	LCD_RESET	LCD_ENABLE	LCD_DAT23	LCD_DAT21	LCD_DAT19	LCD_DAT16	LCD_DAT13	LCD_DAT11	LCD_DAT9	LCD_DAT7	LCD_DAT4	LCD_DAT2	LCD_DAT0	SD2_DAT4	SD2_CMD	SD2_CLK	GND
23	SD1_DAT1	SD1_DAT0	KEY_COL7	KEY_ROW5	KEY_COL2	KEY_COL1	KEY_COL0	LCD_HSYNC	LCD_VSYNC	LCD_DAT22	LCD_DAT20	LCD_DAT18	LCD_DAT15	LCD_DAT12	LCD_DAT10	LCD_DAT8	LCD_DAT6	LCD_DAT3	LCD_DAT1	SD2_RST	SD2_DAT3	SD2_DAT1	CLK1_P	CLK1_N

7 Revision History

Table 83 provides a revision history for this data sheet.

Table 83. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Updated Table 77, "Interfaces Allocation During Boot," on page 97.
Rev 0.1	11/2012	• Updated Table 8, "Package Thermal Resistance Data," on page 18. • Corrected title of Table 79, “13 x 13 mm Supplies Contact Assignment,” on page 100. • Corrected title of Table 81, “13 x 13 mm, 0.5 mm Pitch Ball Map,” on page 110.
Rev. 0	10/2012	• Initial public release.