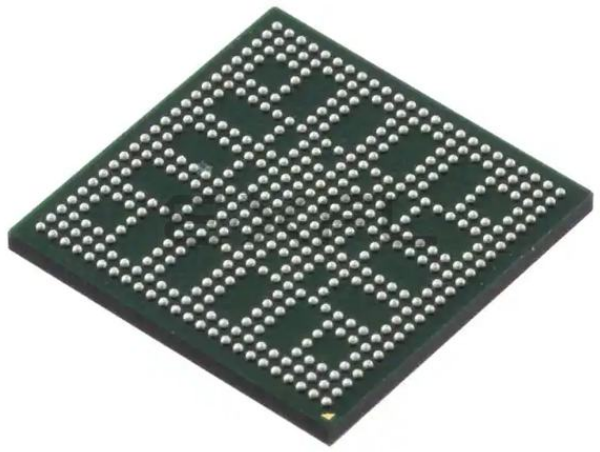

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l3evn10ab

3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 9 provides the operating ranges of the i.MX 6SoloLite processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]		1.5	V	LDO output set at 1.250V minimum for operation up to 996MHz.
		1.275[2]		1.5	V	LDO output set at 1.150V minimum for operation up to 792MHz
		1.075[2]		1.5	V	LDO output set at 0.95V minimum for operation up to 396MHz
		1.075[2]		1.5	V	LDO output set at 0.950V minimum for operation up to 192MHz
		1.050[2]		1.5	V	LDO output set at 0.9250V minimum for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]		1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250		1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 396 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 192MHz
		0.925		1.3	V	LDO bypassed for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]		1.3	V	
Standby/DSM Mode	VDD_ARM_IN	0.9		1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 24.
	VDD_SOC_IN VDD_PU_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8		3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	

Table 15. Audio/Video PLL's Electrical Parameters (continued)

Parameter	Value
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 16. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 Ethernet PLL

Table 17. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.4 480 MHz PLL

Table 18. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles (15 μs)

4.4.5 ARM PLL

Table 19. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc		32.768 kHz		This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption		4 μA		The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA should be added to this value.
Bias resistor		14 MΩ		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 kΩ		Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Dual Voltage General Ppurpose I/O cell set (DVGPIO)
- Single Voltage General Purpose I/O cell set (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.9.3.1 EIM Signal Cross Reference

Table 35 is a guide intended to help the user identify the signals in the EIM chapter of the i.MX 6SoloLite reference manual that are identical to those mentioned in this data sheet.

Table 35. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.9.3.2 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit, and 8-bit devices operating in address/data separate or multiplexed modes. Table 36 provides EIM interface pads allocation in different modes.

Table 36. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode			Multiplexed Address/Data mode	
	8 Bit		16 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001	MUM = 1, DSZ = 010	MUM = 1, DSZ = 011
A[15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]
A[25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_D [9:0]
D[7:0], EIM_EB0	EIM_D [7:0]	—	EIM_D [7:0]	EIM_DA_A [7:0]	EIM_DA_A [7:0]
D[15:8], EIM_EB1	—	EIM_D [15:8]	EIM_D [15:8]	EIM_DA_A [15:8]	EIM_DA_A [15:8]
D[23:16], EIM_EB2	—	—	—	—	EIM_D [7:0]
D[31:24], EIM_EB3	—	—	—	—	EIM_D [15:8]

1 For more information on configuration ports mentioned in this table, see the i.MX 6SololLite reference manual.

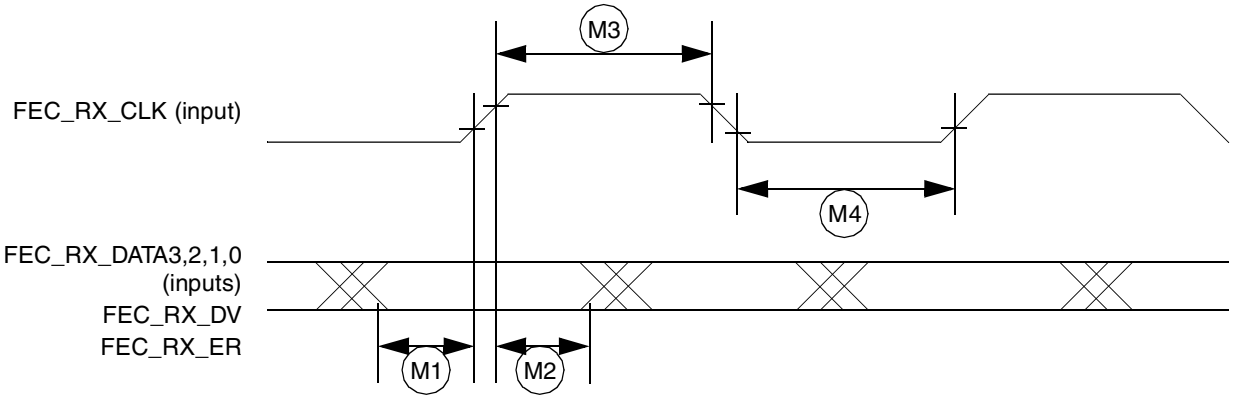

Figure 36. MII Receive Signal Timing Diagram

4.10.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 53 lists MII transmit channel timing parameters. Figure 37 shows MII transmit signal timing diagram for the values listed in Table 53.

Table 53. MII Transmit Signal Timing

Num	Characteristic[1] [2]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

1 FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

2 Test conditions: 25pF on each output signal.

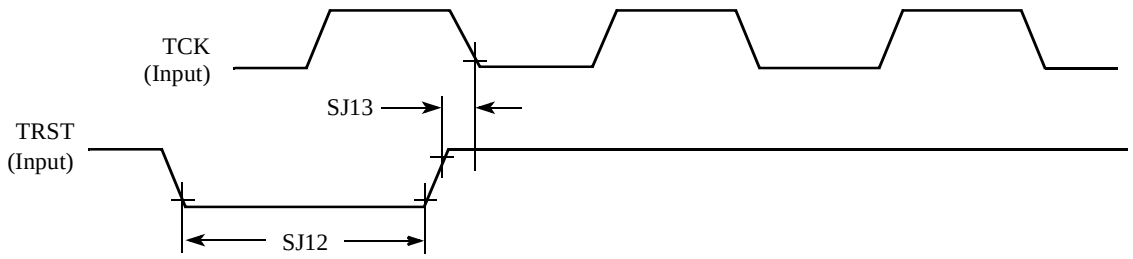

Figure 46. $\overline{\text{TRST}}$ Timing Diagram

Table 59. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.10.9 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 60 and Figure 47 and Figure 48 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 62. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 63. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 64. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 72. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.13 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 76 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloLite Fuse Map document and the System Boot chapter of the i.MX 6SoloLite reference manual.

Table 76. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 78. 13 x 13, 0.5 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	0.88	-	1.1
Stand Off	A1	0.16	-	0.26
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.54 REF		
Body Size	D	13 BSC		
	E	13 BSC		
Ball Diameter		0.3		
Ball Opening		0.275		
Ball Width	b	0.27	-	0.37
Ball Pitch	e	0.5 BSC		
Ball Count	n	432		
Edge Ball Center to Center	D1	11.5 BSC		
	E1	11.5 BSC		
Body Center to Contact Ball	SD	0.25 BSC		
	SE	0.25 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Coplanarity	ddd	0.08		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.05		

6.1.2 13 x 13 mm Ground, Power, Sense, Not Connected and Reference Contact Assignments

Table 79 shows the device connection list for ground, power, sense, and reference contact signals.

Table 79. 13 x 13 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DDR_VREF	N5	
GND	A1, A4, A7, A24, C6, C10, C14, C19, D1, D2, E5, G1, G8, G9, G10, G11, G13, G14, G15, G17, G18, H3, H7, H18, H22, J5, K1, L7, L9, L10, L11, L12, L13, L14, L15, L16, M5, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N3, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N22, P9, P10, P11, P12, P13, P14, P15, P16, R1, T5, U3, U7, U18, U22, V1, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18, Y5, AA1, AA2, AB10, AB14, AB18, AC18, AD1, AD4, AD7, AD24	
GND_Kelvin	V17	Must be connected
GPANAIO	AD22	Analog pad
NVCC_1P2V	W7	
NVCC18_IO	E14, E15, M20, Y11	
NVCC33_IO	H10, H11, H14, H15, L18, M18, T19, U10, U11	
NVCC_DRAM	E6, Y6, G7, H6, J6, N6, P7, T6, U6, V7	Supply of the DDR Interface
NVCC_DRAM_2P5	M6	
NVCC_PLL	Y19	
NVCC_SD1		
NVCC_SD2		
NVCC_SD3		
VDD_ARM_CAP	J15, J16, J17, J18, K15, K16, K17, K18	Secondary Supply for the ARM0 and ARM1 Cores (internal regulator output—requires capacitor if internal regulator is used)
VDD_ARM_IN	J12, J13, J14, K12, K13, K14	Primary Supply, for the ARM0 and ARM1 Core' Regulator
VDD_HIGH_CAP	R14, R15, T14, T15	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDD_HIGH_IN	R12, R13, T12, T13	Primary Supply for the 2.5 V Regulator
VDD_PU_CAP	R7, R8, R9, T7, T8, T9	Secondary Supply for the VPU and GPU's (internal regulator output—requires capacitor if internal regulator is used)
VDD_PU_IN	R10, R11, T10, T11	

Table 79. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	
USB_OTG2_VBUS	AD18	
ZQPAD	AE17	
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 80 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 80. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_MCLK	H19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	Keeper
AUD_RXFS	J19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_TXC	H20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP			CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_DQM2	AB3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[2]	Output	0
DRAM_DQM3	C3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[3]	Output	0
DRAM_RAS_B	N1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RAS	Output	0
DRAM_RESET_B	D6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RESET	Output	0
DRAM_SDBA0	J1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[0]	Output	0
DRAM_SDBA1	T1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[1]	Output	0
DRAM_SDBA2	H1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[2]	Output	0
DRAM_SDCKE0	P2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[0]	Output	0
DRAM_SDCKE1	M2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[1]	Output	0
DRAM_SDCLK_0	L1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK0	Input	Hi-Z
DRAM_SDCLK_0_B	M1	NVCC_DRAM	DDRCLK		DRAM_SDCLK_0_B	—	—
DRAM_SDODT0	Y4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[0]	Output	0
DRAM_SDODT1	E4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[1]	Output	0
DRAM_SDQS0	W2	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	W1	NVCC_DRAM	DDRCLK		DRAM_SDQS0_B	—	—
DRAM_SDQS1	F1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	F2	NVCC_DRAM	DDRCLK		DRAM_SDQS1_B	—	—
DRAM_SDQS2	AC3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AD2	NVCC_DRAM	DDRCLK		DRAM_SDQS2_B	—	—
DRAM_SDQS3	B3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	A2	NVCC_DRAM	DDRCLK		DRAM_SDQS3_B	—	—
DRAM_WE_B	U1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDWE	Output	0
ECSPI1_MISO	M19	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	Keeper
ECSPI1_MOSI	N20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[9]	Input	Keeper
ECSPI1_SCLK	N19	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[8]	Input	Keeper
ECSPI1_SS0	M21	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[11]	Input	Keeper
ECSPI2_MISO	T20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[14]	Input	Keeper
ECSPI2_MOSI	U20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[13]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
ECSPI2_SCLK	U19	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[12]	Input	Keeper
ECSPI2_SS0	T21	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[15]	Input	Keeper
EPDC_BDR0	C18	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[5]	Input	Keeper
EPDC_BDR1	B18	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[6]	Input	Keeper
EPDC_D0	A18	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[7]	Input	Keeper
EPDC_D1	A17	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[8]	Input	Keeper
EPDC_D10	G16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[17]	Input	Keeper
EPDC_D11	F14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[18]	Input	Keeper
EPDC_D12	D14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[19]	Input	Keeper
EPDC_D13	B14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[20]	Input	Keeper
EPDC_D14	A14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[21]	Input	Keeper
EPDC_D15	A13	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[12]	Input	Keeper