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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6l8dvn10aa

Table 11. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	
NVCC33_IO	N=156	Use maximal IO Equation[5]	
NVCC18_IO	N=156	Use maximal IO Equation[5]	
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximal power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW

4.6.3.2 DDR3 Mode I/O DC Parameters

The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 24 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

4.7 I/O AC Parameters

Table 24. DDR3 I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA Voh (DSE = 001)	0.8*OVDD[1]	—	V
		Ioh = -1 mA Voh (for all except DSE = 001)			
Low-level output voltage	Vol	Iol = 0.1 mA Vol (DSE = 001)	—	0.2*OVDD	V
		Iol = 1 mA Vol (for all except DSE = 001)			
Input reference voltage	Vref[2]		0.49*OVDD	0.51*OVDD	
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	See Note[3]	V
Differential input Logic Low	Vil(diff)	—	See Note[3]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	μA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance[4]	Rkeep	—	105	175	kΩ

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3)

2 Vref – DDR3 external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 28).

4 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Dual Voltage General Purpose I/O (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.8.3 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 32 shows DDR I/O output buffer impedance of i.MX 6SoloLite processor.

Table 32. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	 Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloLite processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 33 lists the timing parameters.

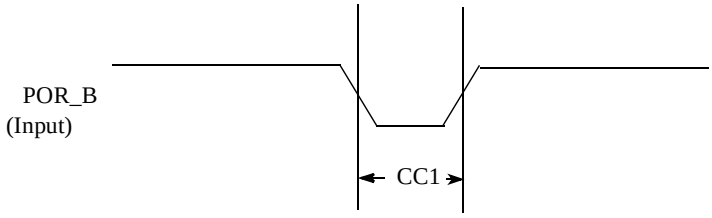


Figure 8. Reset Timing Diagram

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 37 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

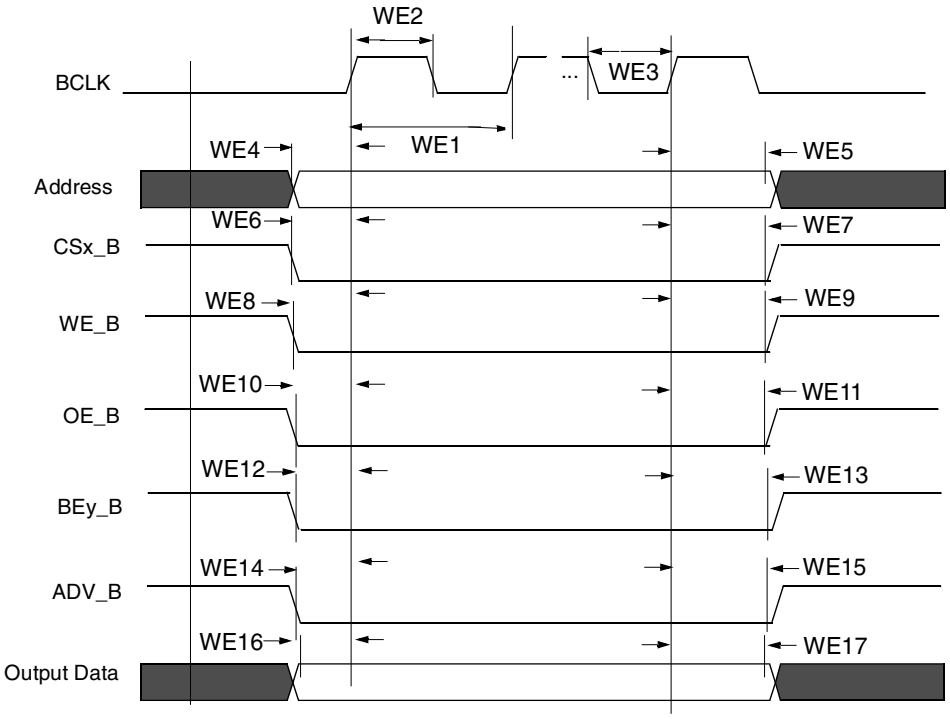


Figure 10. EIM Output Timing Diagram

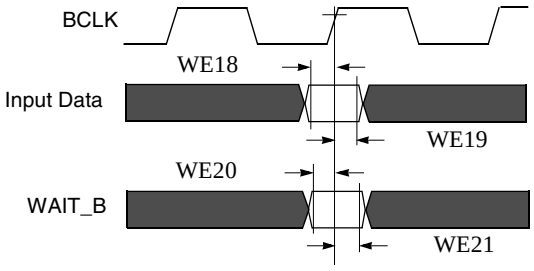


Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 37. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	BCLK cycle time[2]	t*(k+1)	—	ns
WE2	BCLK high level width	0.4*t*(k+1)	—	ns

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20, and Table 38 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6SoloLite reference manual for the EIM programming model.

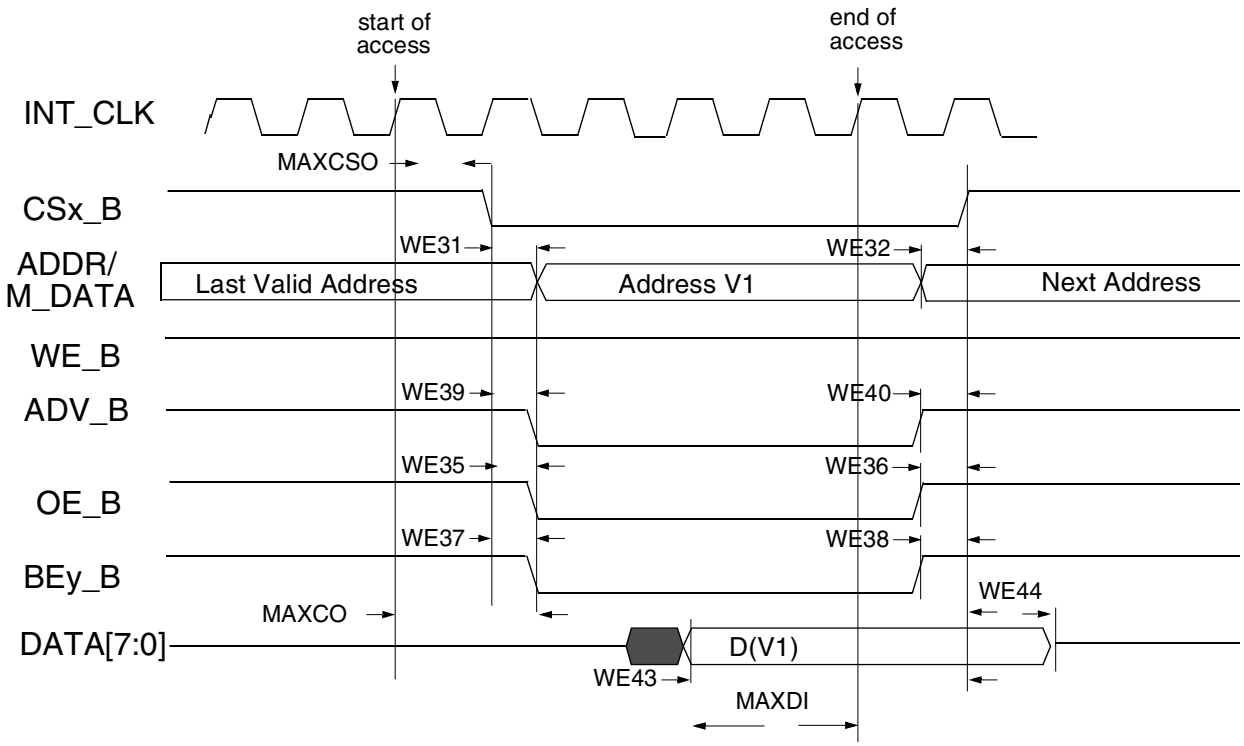


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

Table 38. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output maximum delay from internal driving ADDR/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	Data maximum delay from chip input data to its internal FF	6	—	—	ns
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK maximum delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	ns
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

2 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

3 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

4 t is axi_clk cycle time.

5 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

6 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 42.

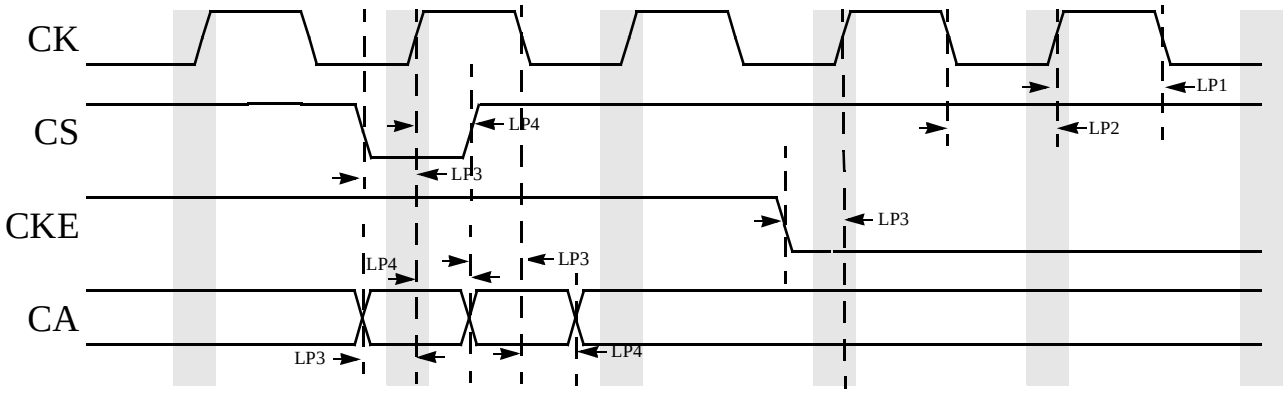


Figure 25. LPDDR2 Command and Address Timing Diagram

Table 42. LPDDR2 Timing Parameter

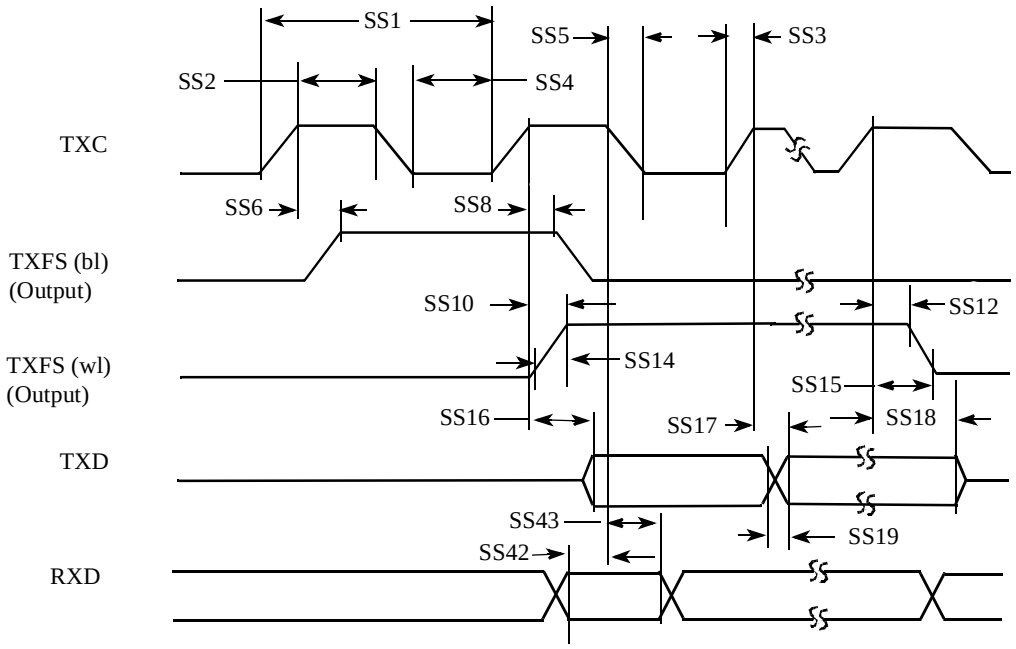
ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CS, CKE setup time	t_{IS}	380	—	ps
LP4	CS, CKE hold time	t_{IH}	380	—	ps
LP3	CA setup time	t_{IS}	770	—	ps
LP4	CA hold time	t_{IH}	770	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10.10.1 SSI Transmitter Timing with Internal Clock

Figure 49 depicts the SSI transmitter internal clock timing and Table 62 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 49. SSI Transmitter Internal Clock Timing Diagram

Table 62. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

Table 64. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.14 EPD Timing Controller

4.10.14.1 Source and Gate Driver for K7902 (SPDC)

4.10.14.1.1 Source Driver

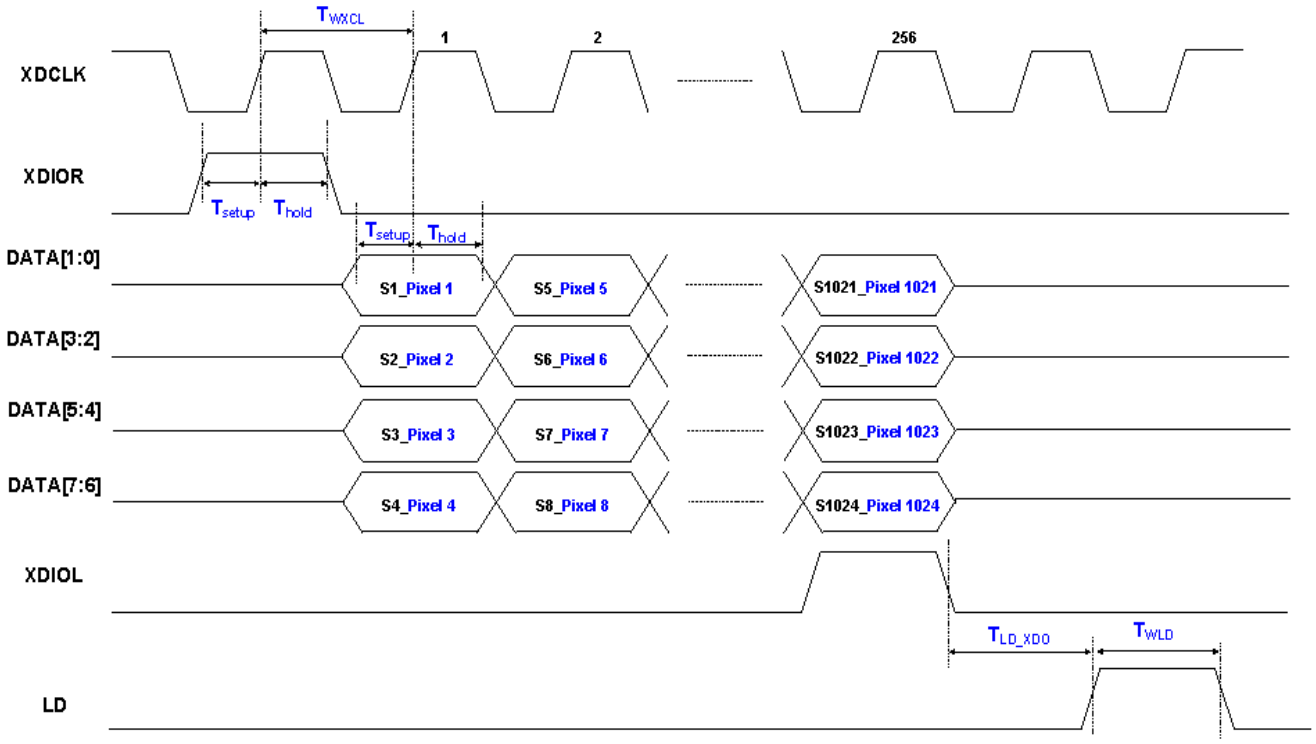


Figure 59. Source Driver Diagram

Table 73. Source Driver Details

Parameter	Symbol	Conditions	Min.	Max.	Unit
Clock period		T_{WXCL}	VDD=3.3V	50	nS
Data setup time		T_{setup}	VDD=3.3V	8	nS
Data hold time		T_{hold}	VDD=3.3V	2	nS
LD pulse width		T_{WLD}	VDD=3.3V	1	XDCLK
Time from XDIOL/XDIOR to LD		T_{LD_XDO}	VDD=3.3V	1	XDCLK

5.2 Boot Devices Interfaces Allocation

Table 77 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 77. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	
EIM	EIM	LCD_DAT[6-21], KEY_COL[0-7], KEY_ROW[0-7], EPDC_D[8-15], EPDC_VCOM0, EPDC_VCOM1, EPDC_BDR0, EPDC_PWRCTRL[0-2], EPDC_SDCE1	
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D5, NANDF_D6, NANDF_D7, NANDF_D8, KEY_ROW1	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit Fastboot (UHSI not supported)
SD/MMC	USDHC-4	FEC_MDIO, FEC_TX_CLK, FEC_RX_ER, FEC_CRS_DV, FEC_RXD1, FEC_TXD0, FEC_MDC, FEC_RXD0, FEC_TX_EN, FEC_TXD1, EPDC_PWCTRL1, FEC_REFOUT	1, 4, or 8 bit Fastboot
I2C	I2C-1	I2C1_SCL, I2C1_SDA	—
I2C	I2C-2	I2C2_SCL, I2C2_SDA	—
I2C	I2C-3	AUD_RXFS, AUD_RXC	—
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B USB_OTG1_DP, USB_OTG1_DN, and USB_OTG1_VBUS	—

Table 79. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	
USB_OTG2_VBUS	AD18	
ZQPAD	AE17	
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 80 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 80. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_MCLK	H19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	Keeper
AUD_RXFS	J19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_TXC	H20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP			CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D12	C1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[12]	Input	PU (100K)
DRAM_D13	C2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[13]	Input	PU (100K)
DRAM_D14	B1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[14]	Input	PU (100K)
DRAM_D15	B2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[15]	Input	PU (100K)
DRAM_D16	AD8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[16]	Input	PU (100K)
DRAM_D17	AC7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[17]	Input	PU (100K)
DRAM_D18	AD6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[18]	Input	PU (100K)
DRAM_D19	AC6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[19]	Input	PU (100K)
DRAM_D2	AB2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[2]	Input	PU (100K)
DRAM_D20	AD5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[20]	Input	PU (100K)
DRAM_D21	AC5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[21]	Input	PU (100K)
DRAM_D22	AC4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[22]	Input	PU (100K)
DRAM_D23	AD3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[23]	Input	PU (100K)
DRAM_D24	A3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[24]	Input	PU (100K)
DRAM_D25	B4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[25]	Input	PU (100K)
DRAM_D26	B5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[26]	Input	PU (100K)
DRAM_D27	A5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[27]	Input	PU (100K)
DRAM_D28	B6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[28]	Input	PU (100K)
DRAM_D29	A6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[29]	Input	PU (100K)
DRAM_D3	AB1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[3]	Input	PU (100K)
DRAM_D30	B7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[30]	Input	PU (100K)
DRAM_D31	A8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[31]	Input	PU (100K)
DRAM_D4	AA3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[4]	Input	PU (100K)
DRAM_D5	Y3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[5]	Input	PU (100K)
DRAM_D6	Y1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[6]	Input	PU (100K)
DRAM_D7	Y2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[7]	Input	PU (100K)
DRAM_D8	E2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[8]	Input	PU (100K)
DRAM_D9	E1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[9]	Input	PU (100K)
DRAM_DQM0	V2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[0]	Output	0
DRAM_DQM1	G2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[1]	Output	0

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_DQM2	AB3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[2]	Output	0
DRAM_DQM3	C3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[3]	Output	0
DRAM_RAS_B	N1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RAS	Output	0
DRAM_RESET_B	D6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RESET	Output	0
DRAM_SDBA0	J1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[0]	Output	0
DRAM_SDBA1	T1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[1]	Output	0
DRAM_SDBA2	H1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[2]	Output	0
DRAM_SDCKE0	P2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[0]	Output	0
DRAM_SDCKE1	M2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[1]	Output	0
DRAM_SDCLK_0	L1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK0	Input	Hi-Z
DRAM_SDCLK_0_B	M1	NVCC_DRAM	DDRCLK		DRAM_SDCLK_0_B	—	—
DRAM_SDODT0	Y4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[0]	Output	0
DRAM_SDODT1	E4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[1]	Output	0
DRAM_SDQS0	W2	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	W1	NVCC_DRAM	DDRCLK		DRAM_SDQS0_B	—	—
DRAM_SDQS1	F1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	F2	NVCC_DRAM	DDRCLK		DRAM_SDQS1_B	—	—
DRAM_SDQS2	AC3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AD2	NVCC_DRAM	DDRCLK		DRAM_SDQS2_B	—	—
DRAM_SDQS3	B3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	A2	NVCC_DRAM	DDRCLK		DRAM_SDQS3_B	—	—
DRAM_WE_B	U1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDWE	Output	0
ECSPI1_MISO	M19	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	Keeper
ECSPI1_MOSI	N20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[9]	Input	Keeper
ECSPI1_SCLK	N19	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[8]	Input	Keeper
ECSPI1_SS0	M21	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[11]	Input	Keeper
ECSPI2_MISO	T20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[14]	Input	Keeper
ECSPI2_MOSI	U20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[13]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
LCD_DAT15	N23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[24]	Input	Keeper
LCD_DAT5	U21	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		src_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_WAKEUP_ALARM	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
PWM1	Y7	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[22]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
RTC_XTALI	AB19	VDD_SNVS_CAP			RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP			RTC_XTALO	—	—
SD1_CLK	B20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[13]	Input	Keeper
SD1_DAT3	B22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[6]	Input	Keeper
SD1_DAT4	A22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[12]	Input	Keeper
SD1_DAT5	A21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[9]	Input	Keeper
SD1_DAT6	A20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[7]	Input	Keeper
SD1_DAT7	A19	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[10]	Input	Keeper
SD2_CLK	AC24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[5]	Input	Keeper
SD2_CMD	AB24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[4]	Input	Keeper
SD2_DAT0	AB22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[1]	Input	Keeper
SD2_DAT1	AB23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[30]	Input	Keeper
SD2_DAT2	AA22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[3]	Input	Keeper
SD2_DAT3	AA23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[28]	Input	Keeper
SD2_DAT4	AA24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[2]	Input	Keeper
SD2_DAT5	Y20	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[31]	Input	Keeper
SD2_DAT6	Y21	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[29]	Input	Keeper
SD2_DAT7	Y22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[0]	Input	Keeper
SD2_RST	Y23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[27]	Input	Keeper
SD3_CLK	AB11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[18]	Input	Keeper
SD3_CMD	AA11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[21]	Input	Keeper
SD3_DAT0	AC11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[19]	Input	Keeper
SD3_DAT1	AD11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[20]	Input	Keeper
SD3_DAT2	AC12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[16]	Input	Keeper
SD3_DAT3	AD12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[17]	Input	Keeper

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

8	9	10	11	12	13	14
DRAM_D31	EPDC_SDCE3	EPDC_SDCE1	EPDC_GDSP	EPDC_GDCLK	EPDC_D15	EPDC_D14
EPDC_SDLE	EPDC_SDCE2	EPDC_SDCLK	EPDC_PRWCOM	EPDC_GDRL	EPDC_GDOE	EPDC_D13
NC	**NC**	GND	EPDC_SDCE0	**NC**	**NC**	GND
NC	**NC**	EPDC_PWRWAKEUP	EPDC_PWRCTRL0	**NC**	**NC**	EPDC_D12
NC	**NC**	EPDC_PWRSTAT	EPDC_PWRCTRL1	**NC**	**NC**	NVCC18_IO
NC	**NC**	EPDC_PWRINT	EPDC_PWRCTRL2	**NC**	**NC**	EPDC_D11
GND	GND	GND	GND	EPDC_PWRCTRL3	GND	GND
NC	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	NVCC33_IO
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
NC	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
NC	GND	GND	GND	GND	GND	GND
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
NC	**NC**	NVCC_3V3	NHVCC_3V3	**NC**	**NC**	VDD_USB_CAP
GND	GND	GND	GND	GND	GND	GND
NC	**NC**	FEC_REF_CLK	FEC_TXD1	**NC**	**NC**	JTAG_TDI
NC	**NC**	FEC_TXD0	NVCC18_IO	**NC**	**NC**	JTAG_MOD
NC	**NC**	FEC_RXD0	SD3_CMD	**NC**	**NC**	JTAG_TCK
NC	**NC**	GND	SD3_CLk	**NC**	**NC**	GND
FEC_TX_CLK	FEC_CRS_DV	FEC_RXD1	SD3_DAT0	SD3_DAT2	I2C1_SCL	REF_CLK_24M
DRAM_D16	FEC_RX_ER	FEC_TX_EN	SD3_DAT1	SD3_DAT3	I2C1_SDA	REF_CLK_32K

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

1	2	3	4	5	6	7
GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND
DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30
DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0
GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1
DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE
DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR
GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND
DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP
GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP
DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND
DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND
DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND
DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP
DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP
DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND
GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2
DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1
GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC
DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO
DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17
GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D20	GND