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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6l8dvn10ab

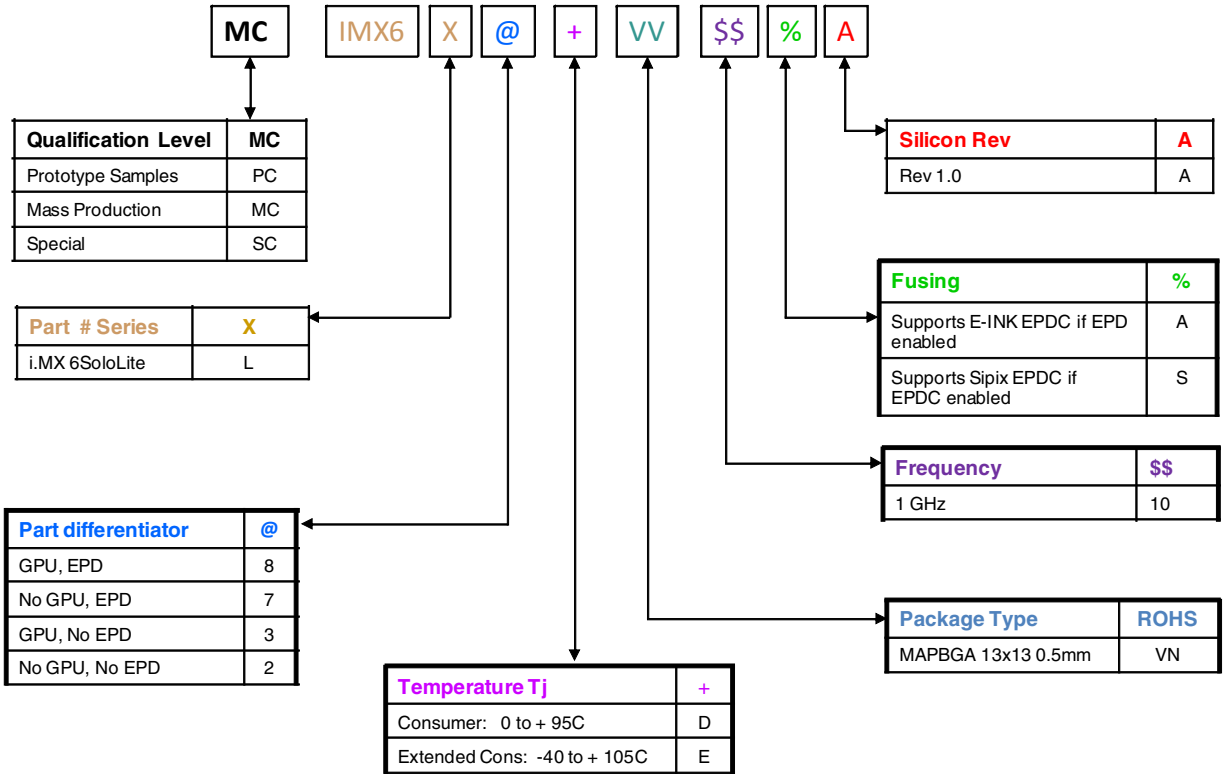

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

  - EPDC, color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
  - SPDC, color, and monochrome SiPix panels
- Camera sensors:
  - Parallel Camera port (up to 16 bit)
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - One USB 2.0 (480 Mbps) hosts:
    - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
  - Three I^2S/SSI/AC97 supported
  - Five UARTs, up to 4.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Four eCSPI (Enhanced CSPI)
  - Three I^2C, supporting 400 kbps
  - Ethernet Controller, 10/100 Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloLite processor uses dedicated HW accelerators to meet the targeted multimedia performance. The use of HW accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloLite processor incorporates the following hardware accelerators:

- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as 2D hardware graphics acceleration, E-Ink or SiPix may not be enabled for specific part numbers.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD. either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Softwareitching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDC	Electrophoretic Display Controller	Peripherals	The SPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive SiPix™ EPD panels, supporting a wide variety of TFT backplanes.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • One Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDD_ARM_IN and VDD_SOC_IN are connected to different external supply sources, then VDD_ARM_IN supply must be turned ON together with VDD_SOC_IN supply or not delayed more than 1 ms.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6SoloLite reference manual for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

4.2.2 Power-Down Sequence

Table 14 shows the power down sequence orders. The two cases shown are, using the i.MX6 SoloLite internal supplies (non-bypass) and bypassing the internal LDO supplies.

Table 14. Power-Down Sequencing Order

Power Rail Name	Using all internal LDOs (non-bypass mode)	Internal LDOs Bypassed
VDD_SNVS_IN	7	9
VDD_HIGH_IN / NVCC33_IO	6	8
VDD_HIGH_CAP	6	7
NVCC18_IO	5	6
NVCC_PLL	6	5
NVCC_DRAM	4	4
VDD_ARM_IN	3	3
VDD_PU_IN	2	2
VDD_SOC_IN	1	1
USB_VBUS	N/A	N/A

NOTE

- VDD_ARM_IN, VDD_PU_IN, and VDD_SOC_IN can startup at the same. However, VDD_ARM_IN and VDD_PU_IN must be at their target values within 0.5 ms of VDD_SOC_IN.
- There are no special timing requirements for USB_VBUS.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 80, "13 x 13 mm Functional Contact Assignments," on page 101.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 15. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz

Table 22. GPIO I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Sink current in Open Drain mode	Iskod	—	—	7	mA
Sink/source current in Push-Pull mode	Isspp	—	—	7	mA

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The parameters in Table 23 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 23. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9*OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1*OVDD	V
Input reference voltage	Vref		0.49*OVDD	0.51*OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)		0.26	See Note [2]	
Differential Input Logic Low	Vil(diff)		See Note [2]	-0.26	
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	µA
Pull-up/pull-down impedance Mismatch	MMpupd		-15	+15	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 27).

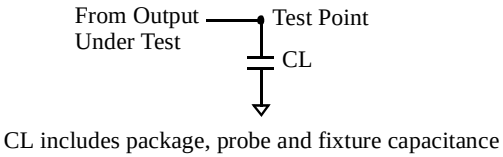

Figure 5. Load Circuit for Output

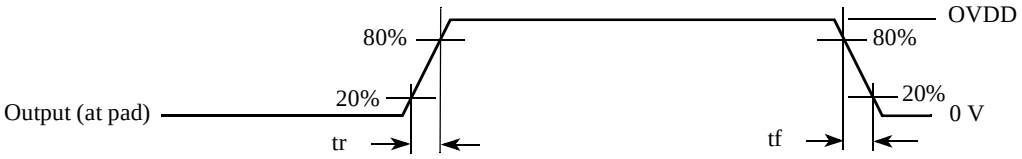

Figure 6. Output Transition Time Waveform

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 42.

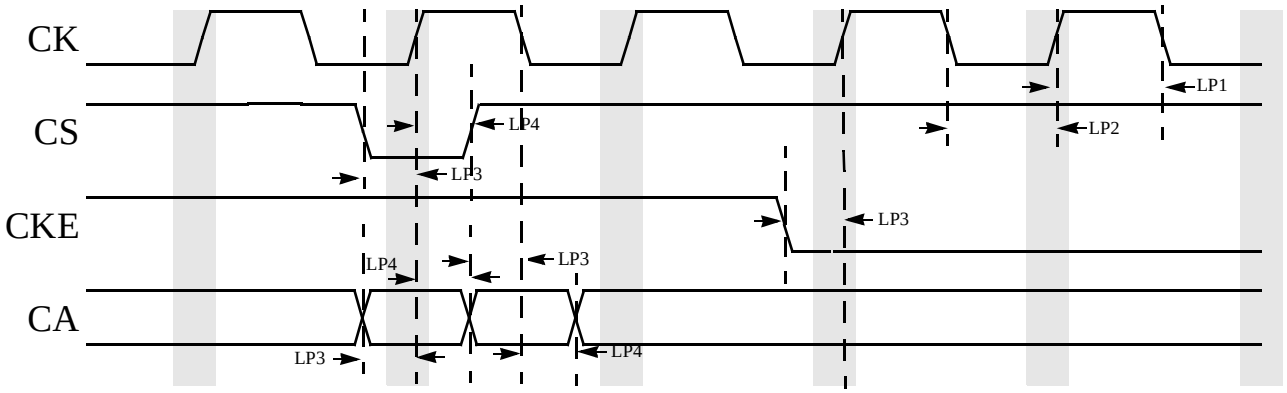

Figure 25. LPDDR2 Command and Address Timing Diagram

Table 42. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CS, CKE setup time	t_{IS}	380	—	ps
LP4	CS, CKE hold time	t_{IH}	380	—	ps
LP3	CA setup time	t_{IS}	770	—	ps
LP4	CA hold time	t_{IH}	770	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10.2 CMOS Sensor Interface (CSI) Timing Parameters

4.10.2.0.1 Gated Clock Mode Timing

Figure 28 and Figure 29 shows the gated clock mode timings for CSI, and Table 45 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

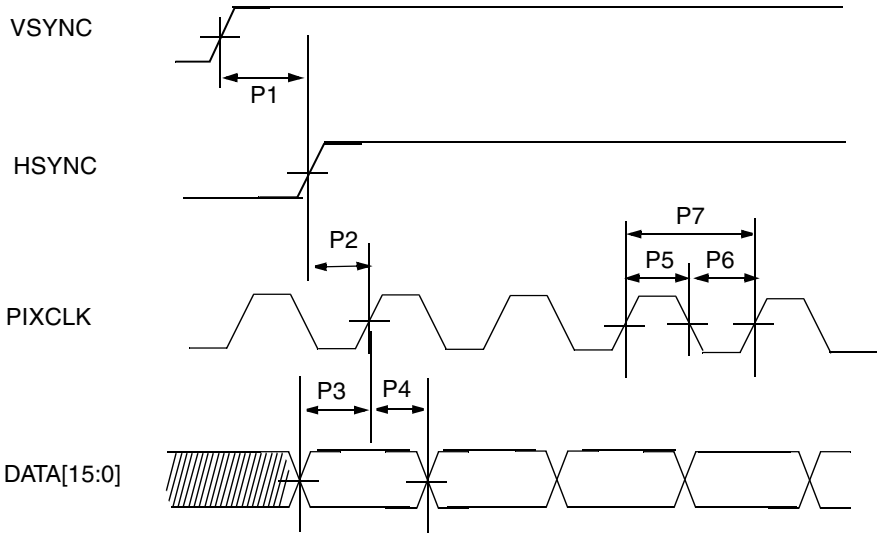

Figure 28. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

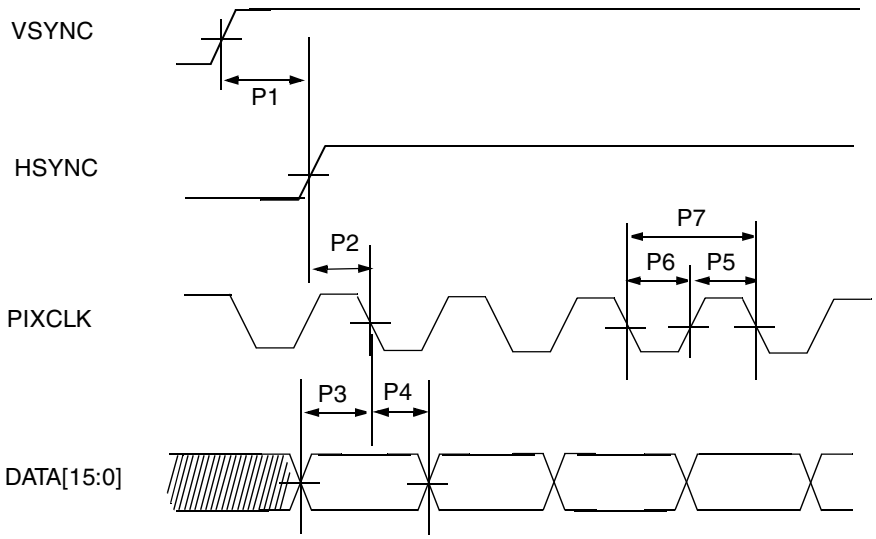

Figure 29. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 55. MII Transmit Signal Timing (continued)

ID	Characteristics[1]	Min	Max	Unit
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40 %	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40 %	60%	FEC_MDC period

1 Test conditions: 25pF on each output signal.

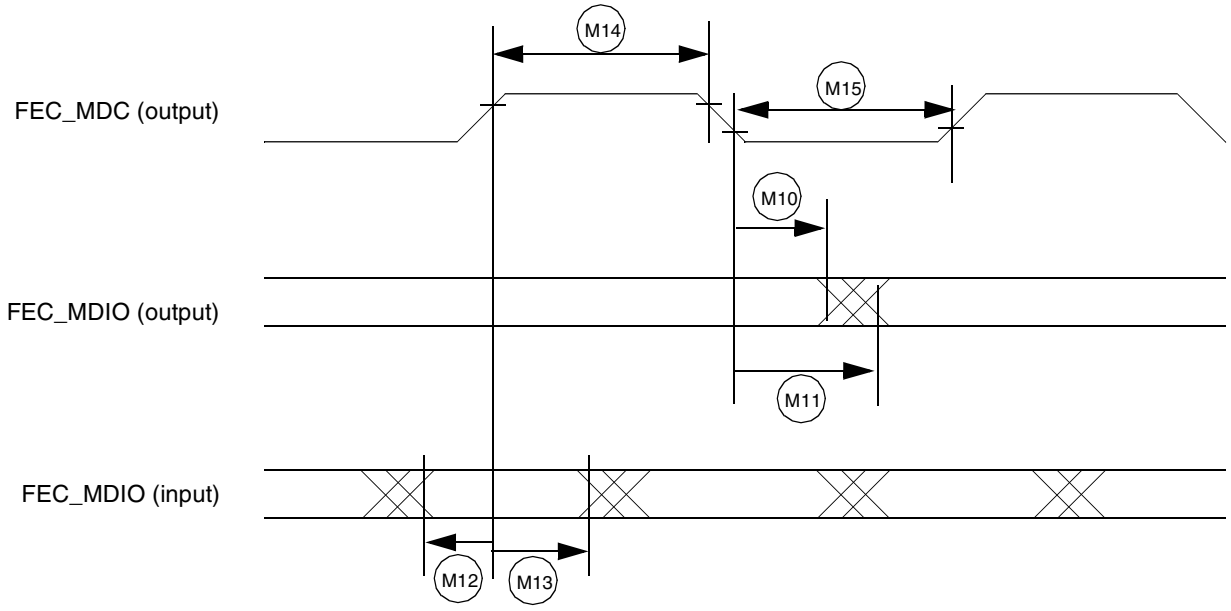

Figure 39. MII Serial Management Channel Timing Diagram

4.10.5.5 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 56 and Figure 40.

Table 56. RMII Signal Timing

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns

Table 60. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

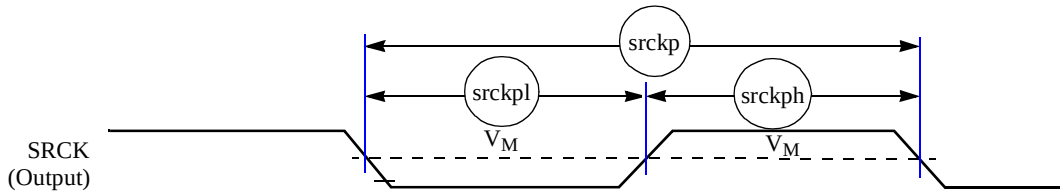

Figure 47. SRCK Timing Diagram

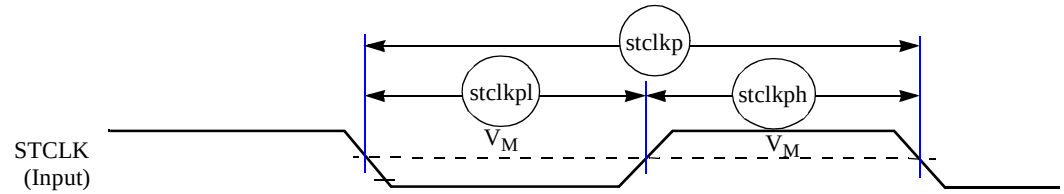

Figure 48. STCLK Timing Diagram

4.10.10.3 SSI Transmitter Timing with External Clock

Figure 51 depicts the SSI transmitter external clock timing and Table 64 lists the timing parameters for the transmitter timing with the external clock.

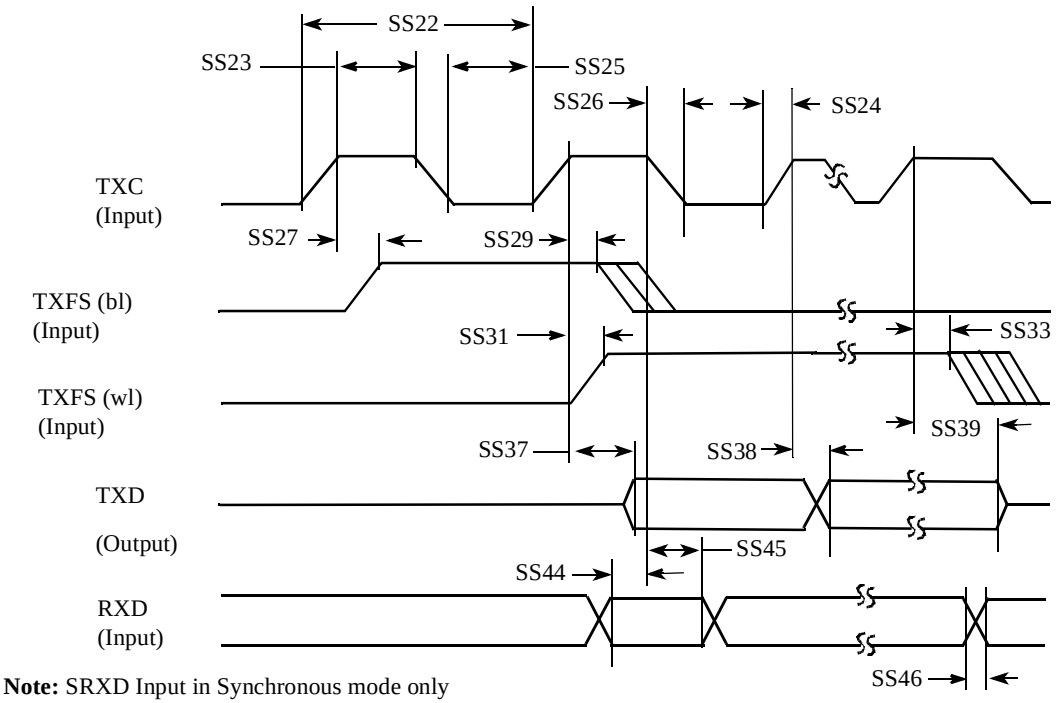

Figure 51. SSI Transmitter External Clock Timing Diagram

Table 64. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 72. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.13 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host.

Table 76. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
LCD_DAT0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DAT1	Input	BOOT_CFG1[1]	
LCD_DAT2	Input	BOOT_CFG1[2]	
LCD_DAT3	Input	BOOT_CFG1[3]	
LCD_DAT4	Input	BOOT_CFG1[4]	
LCD_DAT5	Input	BOOT_CFG1[5]	
LCD_DAT6	Input	BOOT_CFG1[6]	
LCD_DAT7	Input	BOOT_CFG1[7]	
LCD_DAT8	Input	BOOT_CFG2[0]	
LCD_DAT9	Input	BOOT_CFG2[1]	
LCD_DAT10	Input	BOOT_CFG2[2]	
LCD_DAT11	Input	BOOT_CFG2[3]	
LCD_DAT12	Input	BOOT_CFG2[4]	
LCD_DAT13	Input	BOOT_CFG2[5]	
LCD_DAT14	Input	BOOT_CFG2[6]	
LCD_DAT15	Input	BOOT_CFG2[7]	
LCD_DAT16	Input	BOOT_CFG4[0]	
LCD_DAT17	Input	BOOT_CFG4[1]	
LCD_DAT18	Input	BOOT_CFG4[2]	
LCD_DAT19	Input	BOOT_CFG4[3]	
LCD_DAT20	Input	BOOT_CFG4[4]	
LCD_DAT21	Input	BOOT_CFG4[5]	
LCD_DAT22	Input	BOOT_CFG4[6]	
LCD_DAT23	Input	BOOT_CFG4[7]	

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 13 x 13mm Package Information

6.1.1 Case 2240, 13 x 13 mm, 0.5 mm Pitch, 24 x 24 Ball Matrix

Figure 62 shows the top, bottom, and side views of the 13×13 mm BGA package

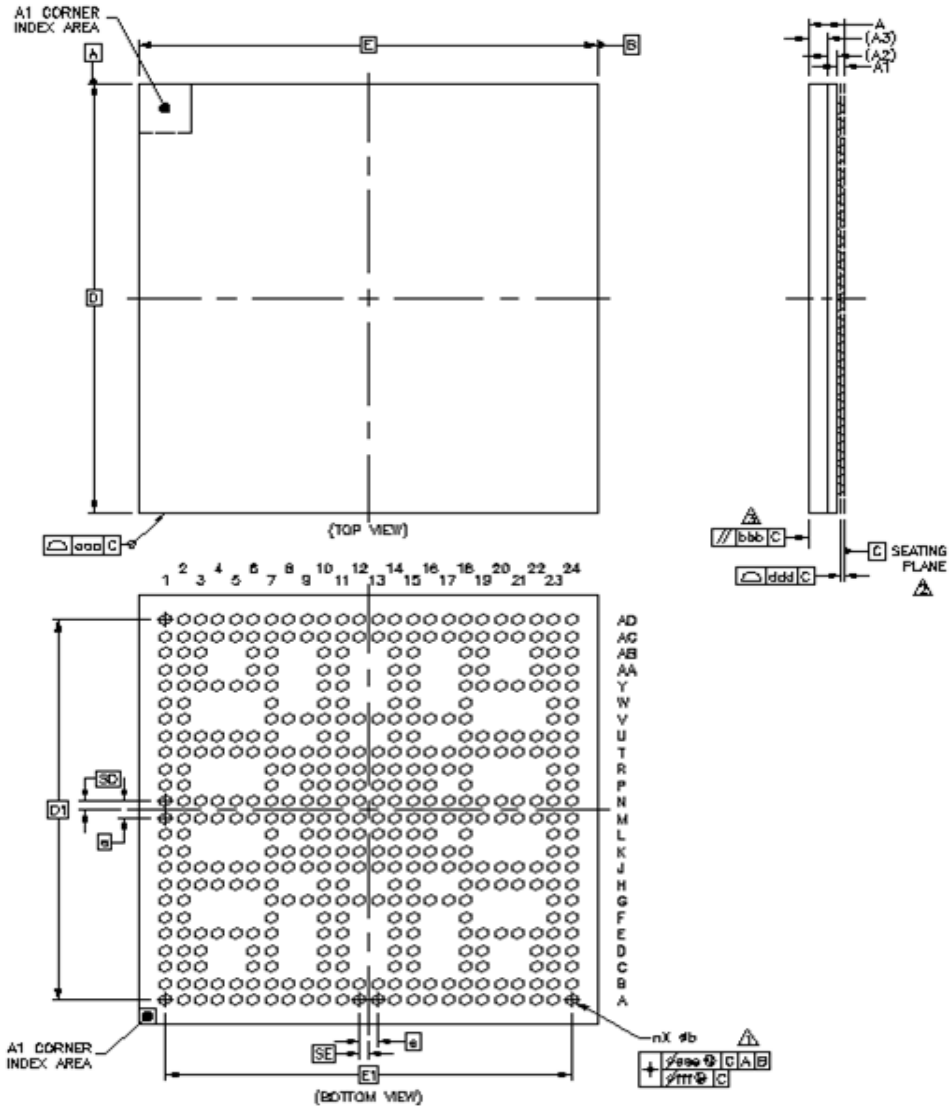

Figure 62. 13 x 13, 0.5 mm BGA Package Top, Bottom, and Side Views

Table 78 shows the 13 x 13 mm BGA package details

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

1	2	3	4	5	6	7
GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND
DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30
DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0
GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1
DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE
DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR
GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND
DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP
GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP
DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND
DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND
DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND
DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP
DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP
DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND
GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM
DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2
DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1
GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC
DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO
DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17
GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D20	GND