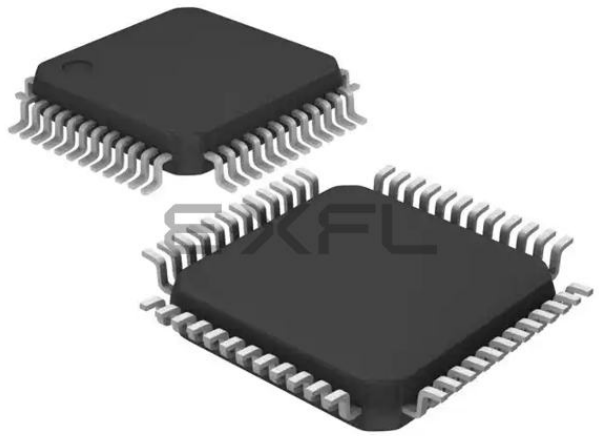

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103cbt6tr

Figure 5. STM32F103xx performance line UFBGA100 pinout

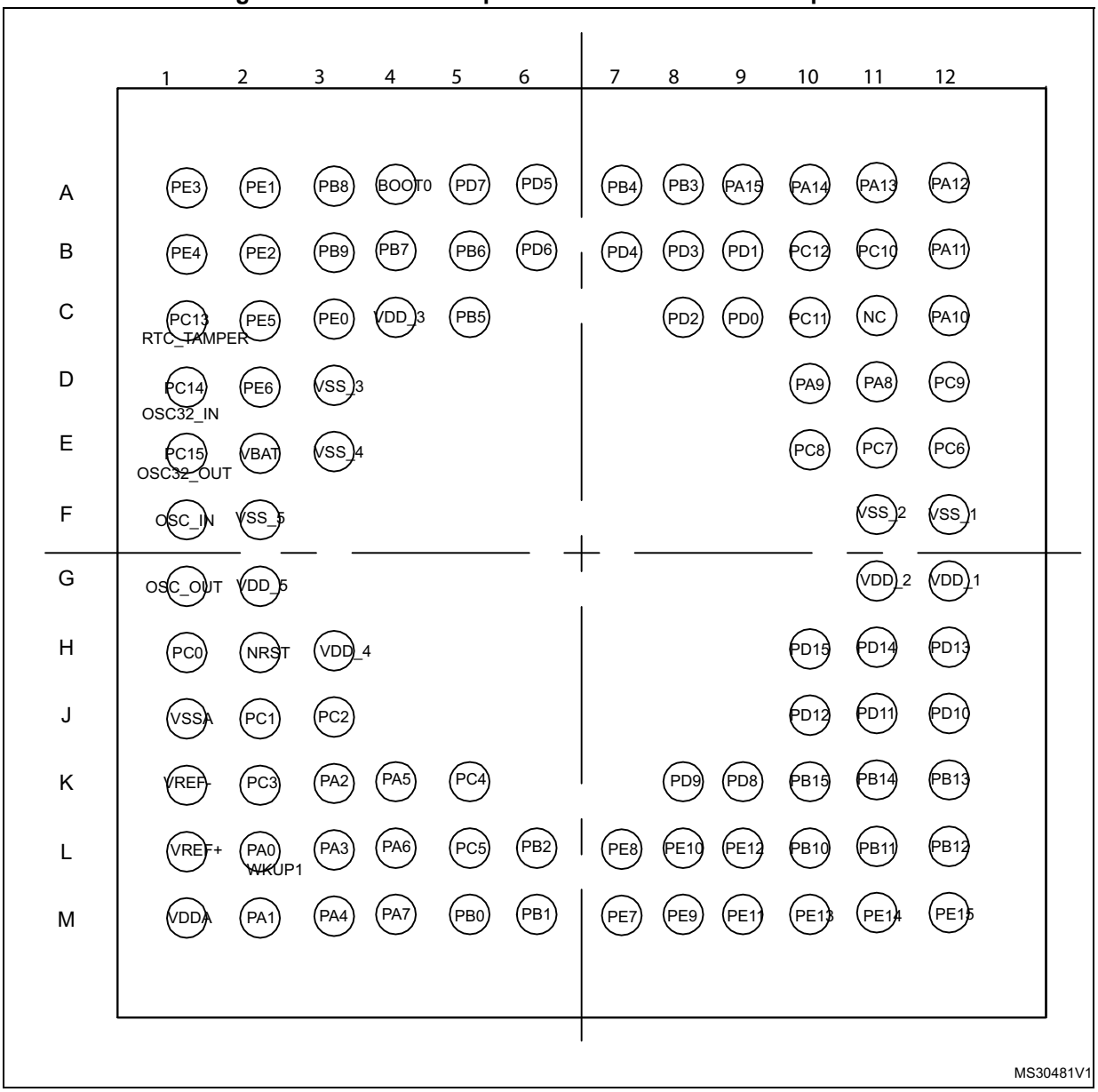


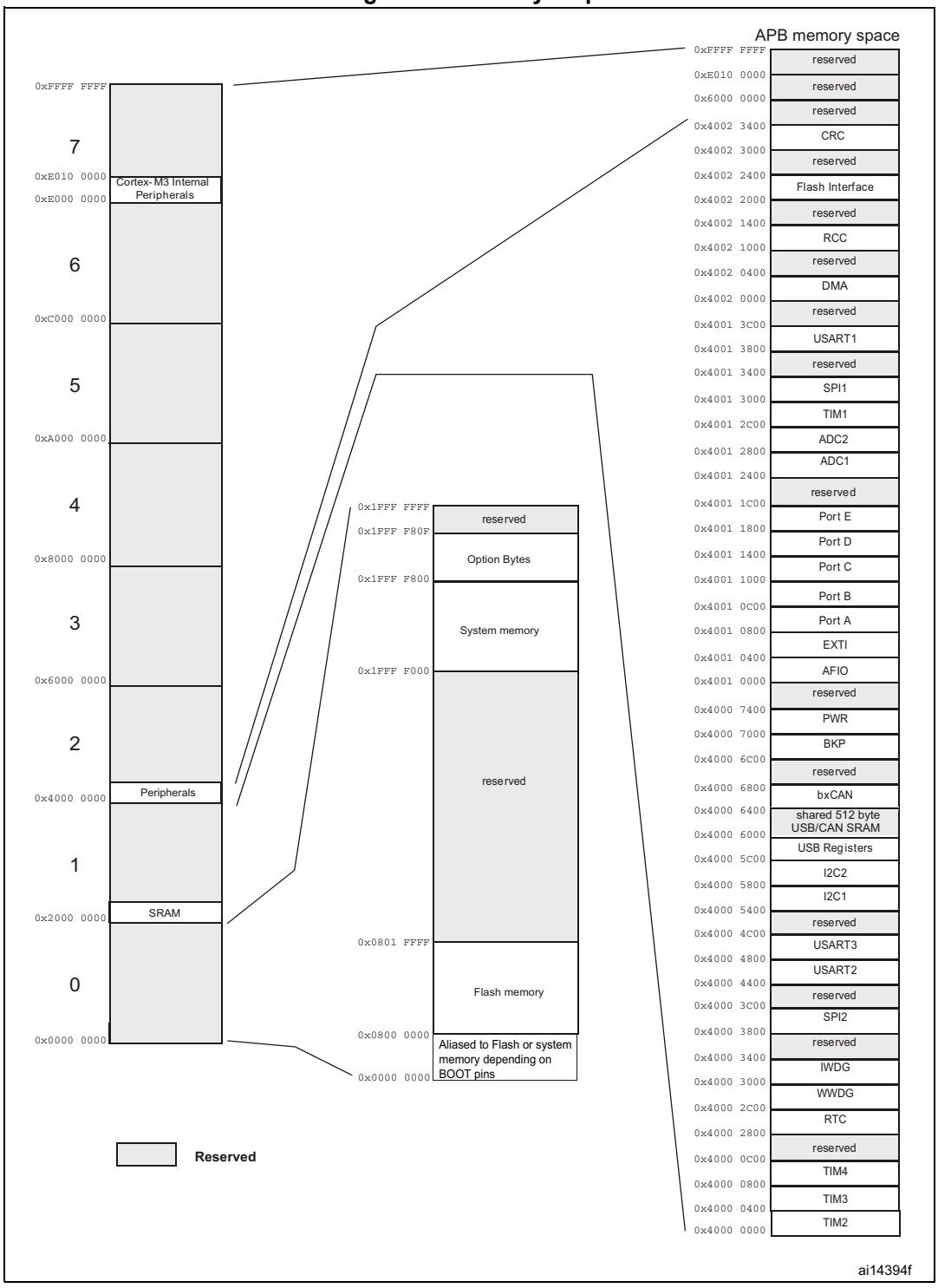
Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A9	A10	37	A7	49	76	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
A8	A9	38	A6	50	77	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ ETR/ PA15 /SPI1_NSS
B9	B11	-	B7	51	78		PC10	I/O	FT	PC10	-	USART3_TX
B8	C10	-	B6	52	79		PC11	I/O	FT	PC11	-	USART3_RX
C8	B10	-	C5	53	80		PC12	I/O	FT	PC12	-	USART3_CK
-	C9	-	C1	-	81	2	PD0	I/O	FT	PD0	-	CANRX
-	B9	-	D1	-	82	3	PD1	I/O	FT	PD1	-	CANTX
B7	C8		B5	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	-
C7	B8	-	-	-	84	-	PD3	I/O	FT	PD3	-	USART2_CTS
D7	B7	-	-	-	85	-	PD4	I/O	FT	PD4	-	USART2_RTS
B6	A6	-	-	-	86	-	PD5	I/O	FT	PD5	-	USART2_TX
C6	B6	-	-	-	87	-	PD6	I/O	FT	PD6	-	USART2_RX
D6	A5	-	-	-	88	-	PD7	I/O	FT	PD7	-	USART2_CK
A7	A8	39	A5	55	89	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI1_SCK
A6	A7	40	A4	56	90	31	PB4	I/O	FT	JNTRST	-	TIM3_CH1/ PB4/ SPI1_MISO
C5	C5	41	C4	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
B5	B5	42	D3	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL(9)/ TIM4_CH1(9)	USART1_TX
A5	B4	43	C3	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA(9)/ TIM4_CH2(9)	USART1_RX
D5	A4	44	B4	60	94	35	BOOT0	I		BOOT0	-	-

4 Memory mapping

The memory map is shown in *Figure 11*.

Figure 11. Memory map



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} –V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		

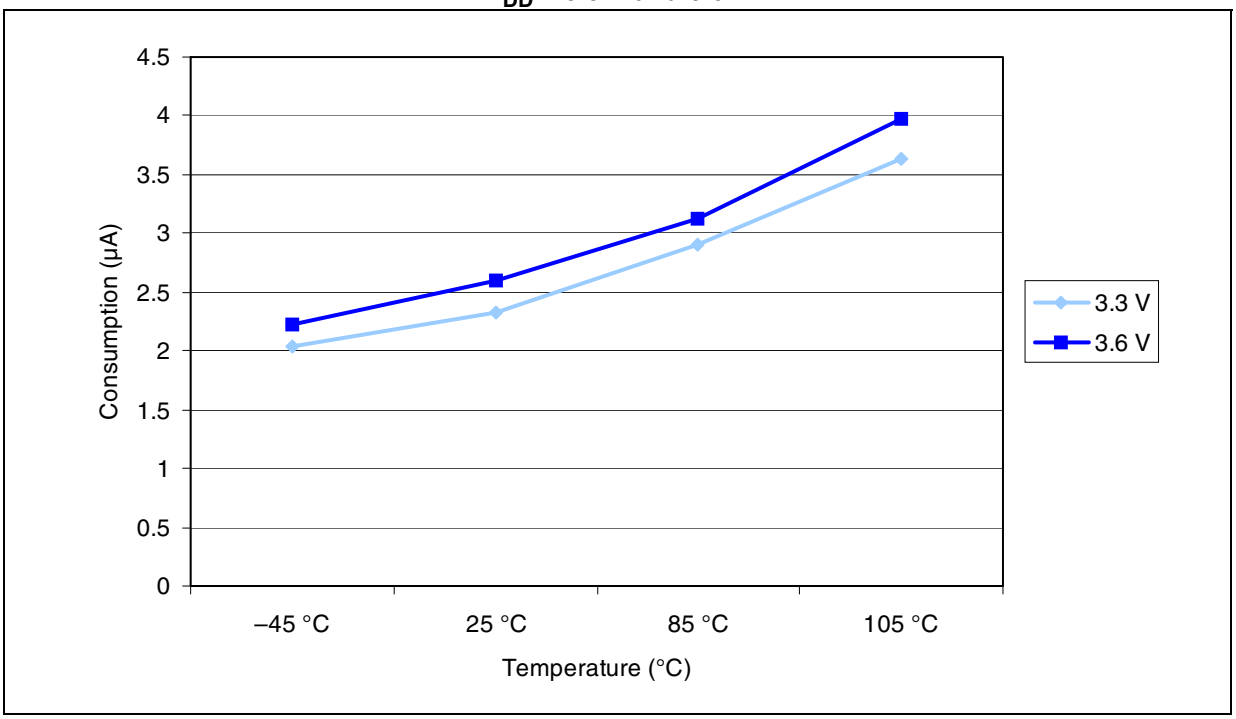
1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note *2. on page 76*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Figure 21. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*

Table 19. Peripheral current consumption

Peripherals		µA/MHz
AHB (up to 72 MHz)	DMA1	16.53
	BusMatrix(1)	8.33
APB1 (up to 36 MHz)	APB1-Bridge	10.28
	TIM2	32.50
	TIM3	31.39
	TIM4	31.94
	SPI2	4.17
	USART2	12.22
	USART3	12.22
	I2C1	10.00
	I2C2	10.00
	USB	17.78
	CAN1	18.06
	WWDG	2.50
	PWR	1.67
	BKP	2.50
	IWDG	11.67

Table 30. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 31. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	12	12	dBµV
			30 to 130 MHz	22	19	
			130 MHz to 1GHz	23	29	
			SAE EMI Level	4	4	-

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 34*

Table 34. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 28. 5 V tolerant I/O input characteristics - CMOS port

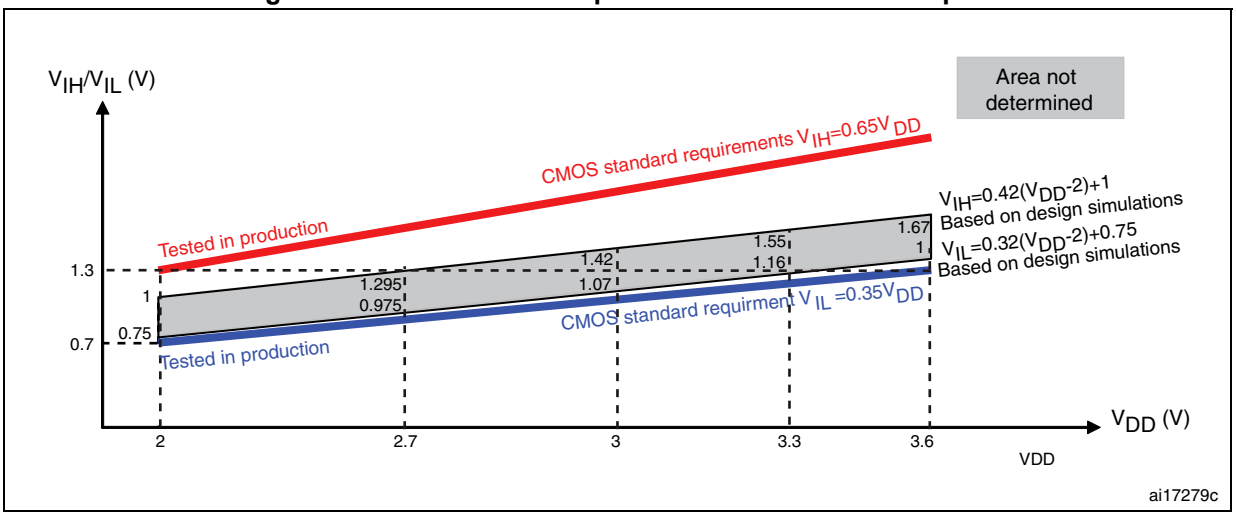
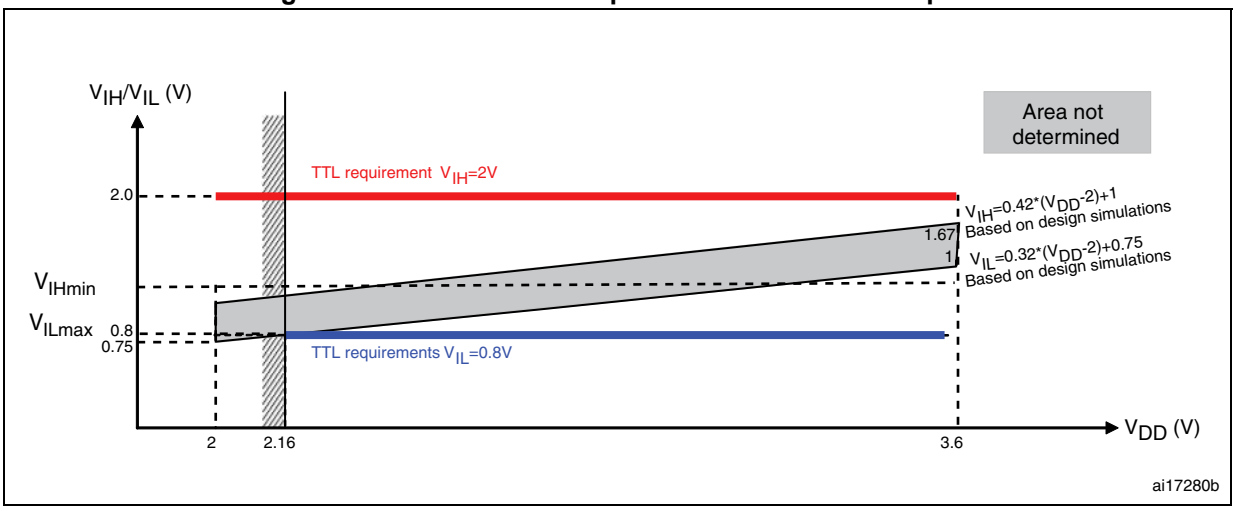


Figure 29. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

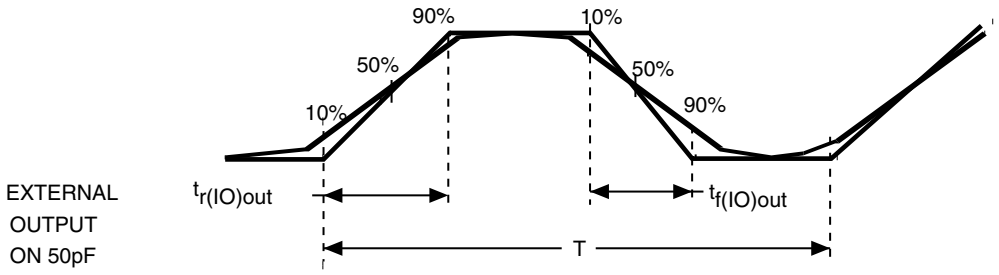
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2), I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed based on test during characterization.

Figure 30. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 35*).

Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 38. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 47. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

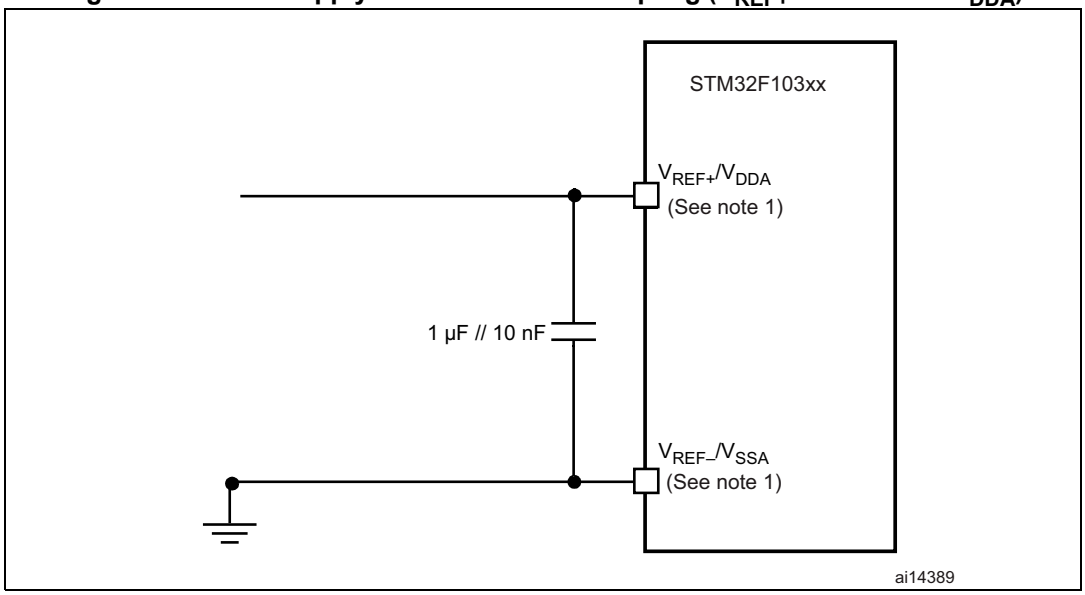
1. Guaranteed based on test during characterization.

Table 48. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Guaranteed based on test during characterization.

Figure 40. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 Temperature sensor characteristics

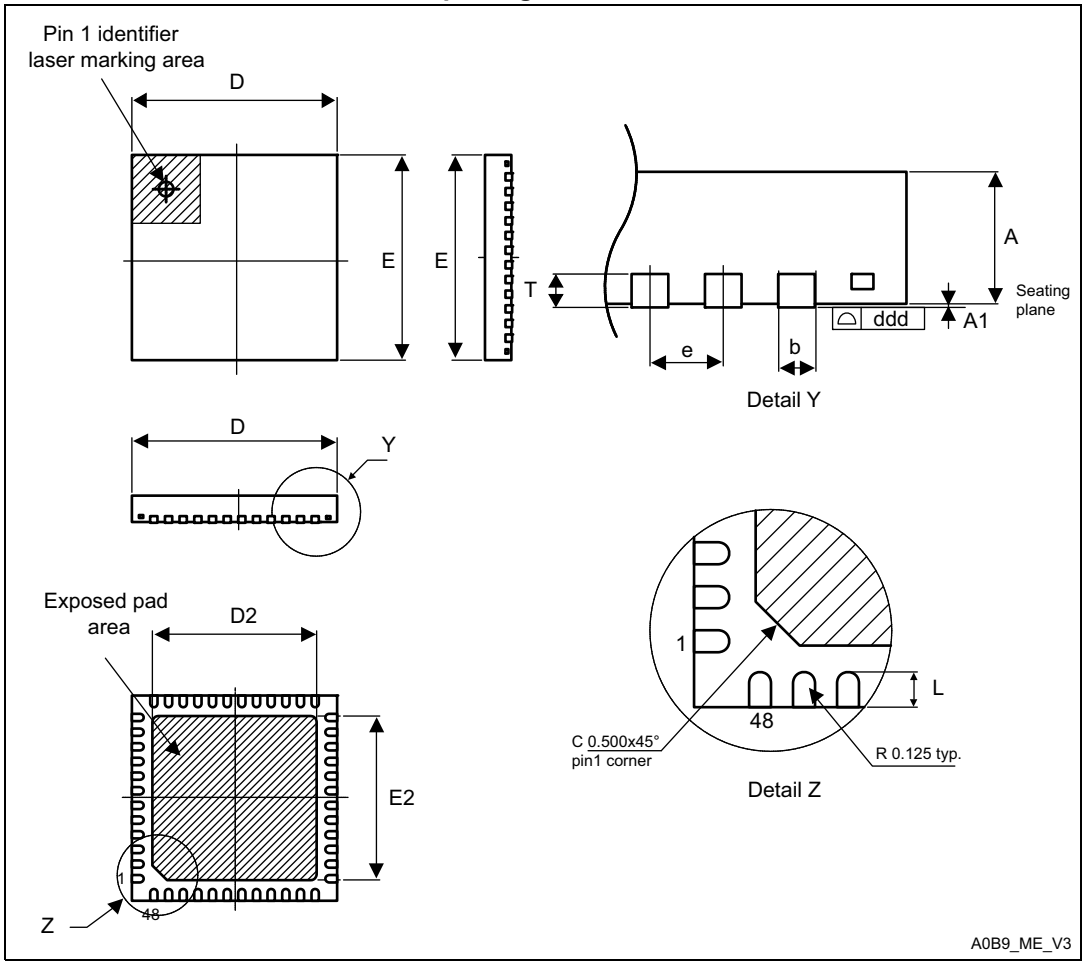
Table 50. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed based on test during characterization.
2. Guaranteed by design.
3. Shortest sampling time can be determined in the application by multiple iterations.

6.2 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 44. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the QFPN package, this pad is not internally connected to the VSS or VDD power pads. It is recommended to connect it to VSS.
3. All leads/pads should also be soldered to the PCB to improve the lead solder joint life.

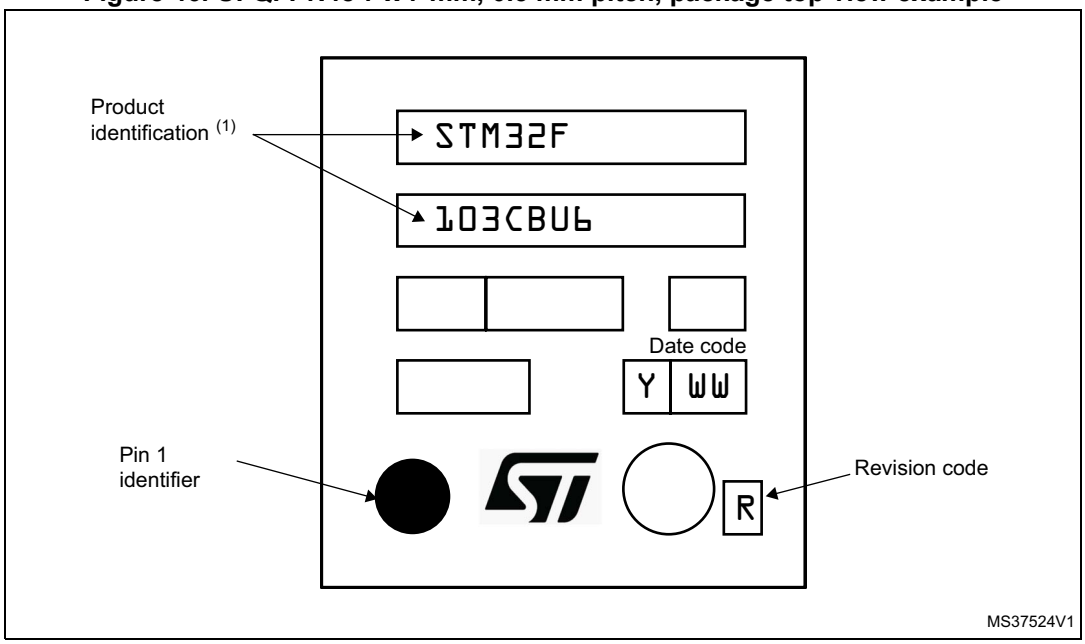
Table 52. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 46. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 53. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint

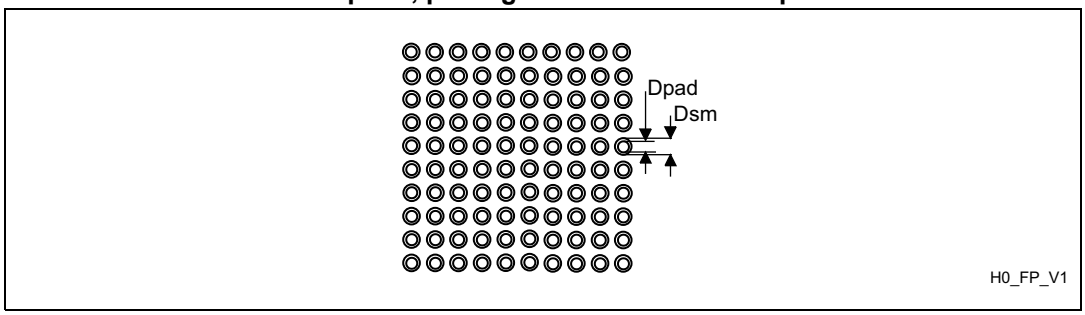
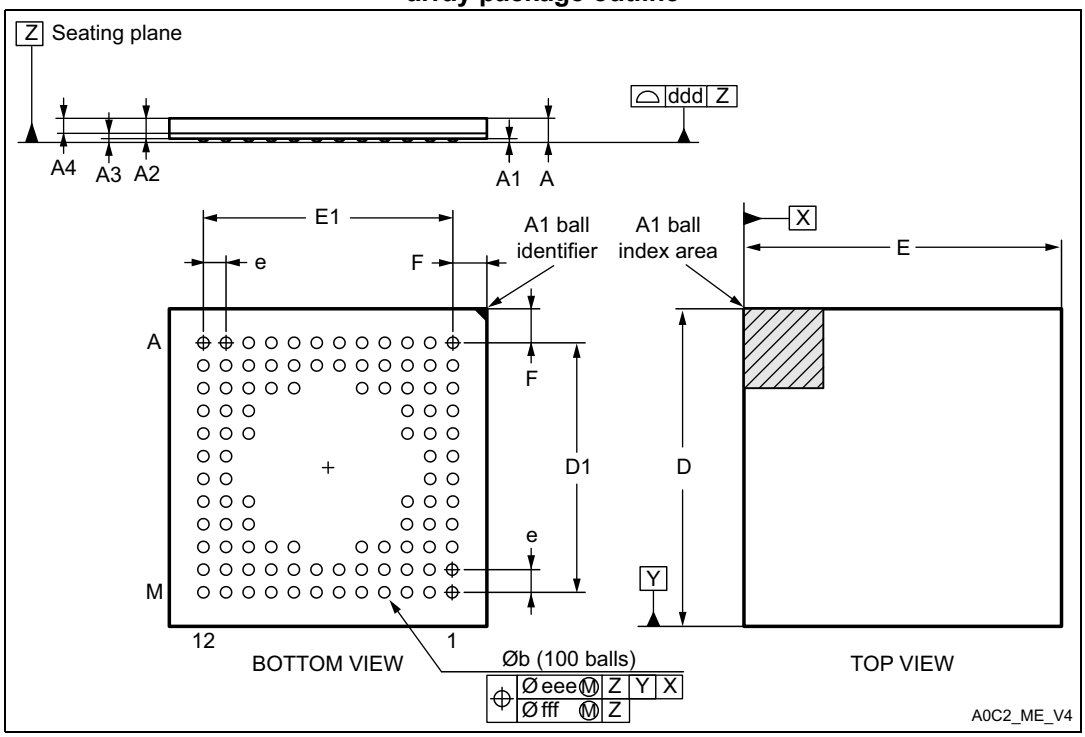


Table 54. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

6.5 UFBGA100 7x 7 mm, ultra fine pitch ball grid array package information

Figure 53. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 56. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

8 Revision history

Table 64. Document revision history

Date	Revision	Changes
01-jun-2007	1	Initial release.
20-Jul-2007	2	Flash memory size modified in *Note 9*, *Note 5*, *Note 7*, *Note 7* and BGA100 pins added to *Table 5: Medium-density STM32F103xx pin definitions*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* added. T_{HSE} changed to T_{LSE} in *Figure 23: Low-speed external clock source AC timing diagram*. V_{BAT} ranged modified in *Power supply schemes*. $t_{SU(LSE)}$ changed to $t_{SU(HSE)}$ in *Table 22: HSE 4-16 MHz oscillator characteristics*. $I_{DD(HSI)}$ max value added to *Table 24: HSI oscillator characteristics*. Sample size modified and machine model removed in *Electrostatic discharge (ESD)*. Number of parts modified and standard reference updated in *Static latch-up*. 25 °C and 85 °C conditions removed and class name modified in *Table 33: Electrical sensitivities*. R_{PU} and R_{PD} min and max values added to *Table 35: I/O static characteristics*. R_{PU} min and max values added to *Table 38: NRST pin characteristics*. *Figure 32: I2C bus AC waveforms and measurement circuit* and *Figure 31: Recommended NRST pin protection* corrected. Notes removed below *Table 9*, *Table 38*, *Table 44*. I_{DD} typical values changed in *Table 11: Maximum current consumption in Run and Sleep modes*. *Table 39: TIMx characteristics* modified. t_{STAB}, V_{REF+} value, t_{lat} and f_{TRIG} added to *Table 46: ADC characteristics*. In *Table :* , typical endurance and data retention for T_A = 85 °C added, data retention for T_A = 25 °C removed. V_{BG} changed to V_{REFINT} in *Table 12: Embedded internal reference voltage*. Document title changed. *Controller area network (CAN)* section modified. *Figure 14: Power supply scheme* modified. *Features on page 1* list optimized. Small text changes.

Table 64. Document revision history (continued)

Date	Revision	Changes
14-May-2013	15 (continued)	Updated *Figure 53: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 56: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data* Updated *Figure 47: LFBGA100 - 100-ball low-profile fine pitch ball grid array, 10 x10 mm, 0.8 mm pitch, package outline* and *Table 53: LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data* Updated *Figure 60: TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline* and *Table 59: TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data*
05-Aug-2013	16	Updated the reference for '$V_{ESD(CDM)}$' in *Table 32: ESD absolute maximum ratings* Corrected 'tf(IO)out' in *Figure 30: I/O AC characteristics definition* Updated *Table 52: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data*
21-Aug-2015	17	Updated *Table 3: STM32F103xx family* removing the note. Updated *Table 63: Ordering information scheme* removing the note. Updated *Section 6: Package information* and added *Section : Marking of engineering samples* for all packages. Updated I2C characteristics, added t_{SP} parameter and note 4 in *Table 40: I2C characteristics*. Updated *Figure 32: I2C bus AC waveforms and measurement circuit* swapping SCLL and SCLH. Updated *Figure 33: SPI timing diagram - slave mode and CPHA = 0*. Updated min/max value notes replacing 'Guaranteed by design, not tested in production" by "guaranteed by design". Updated min/max value notes replacing 'based on characterization, not tested in production" by "Guaranteed based on test during characterization". Updated *Table 19: Peripheral current consumption*.