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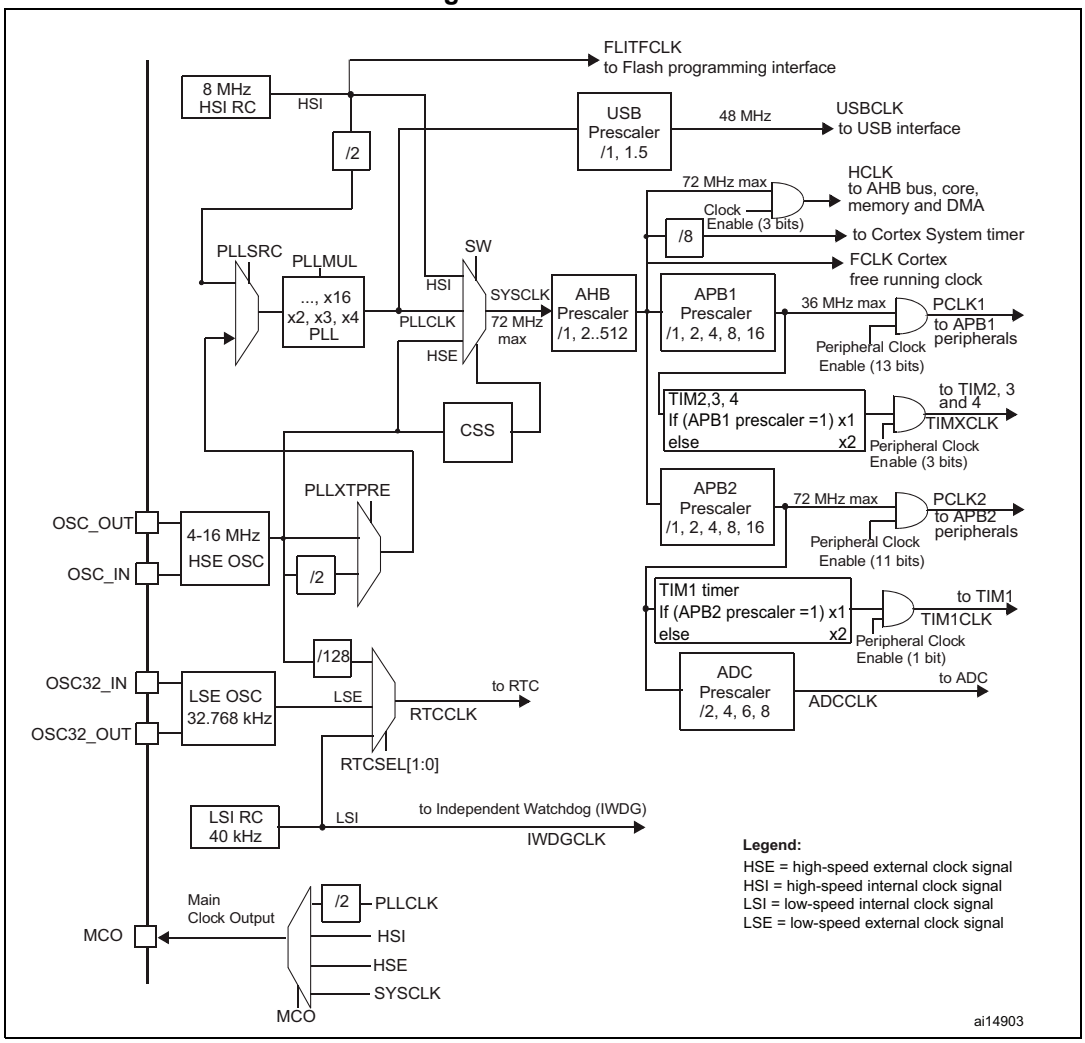
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103r8t7tr

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with USBCLK running at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

2.3.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.20 Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed.

2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

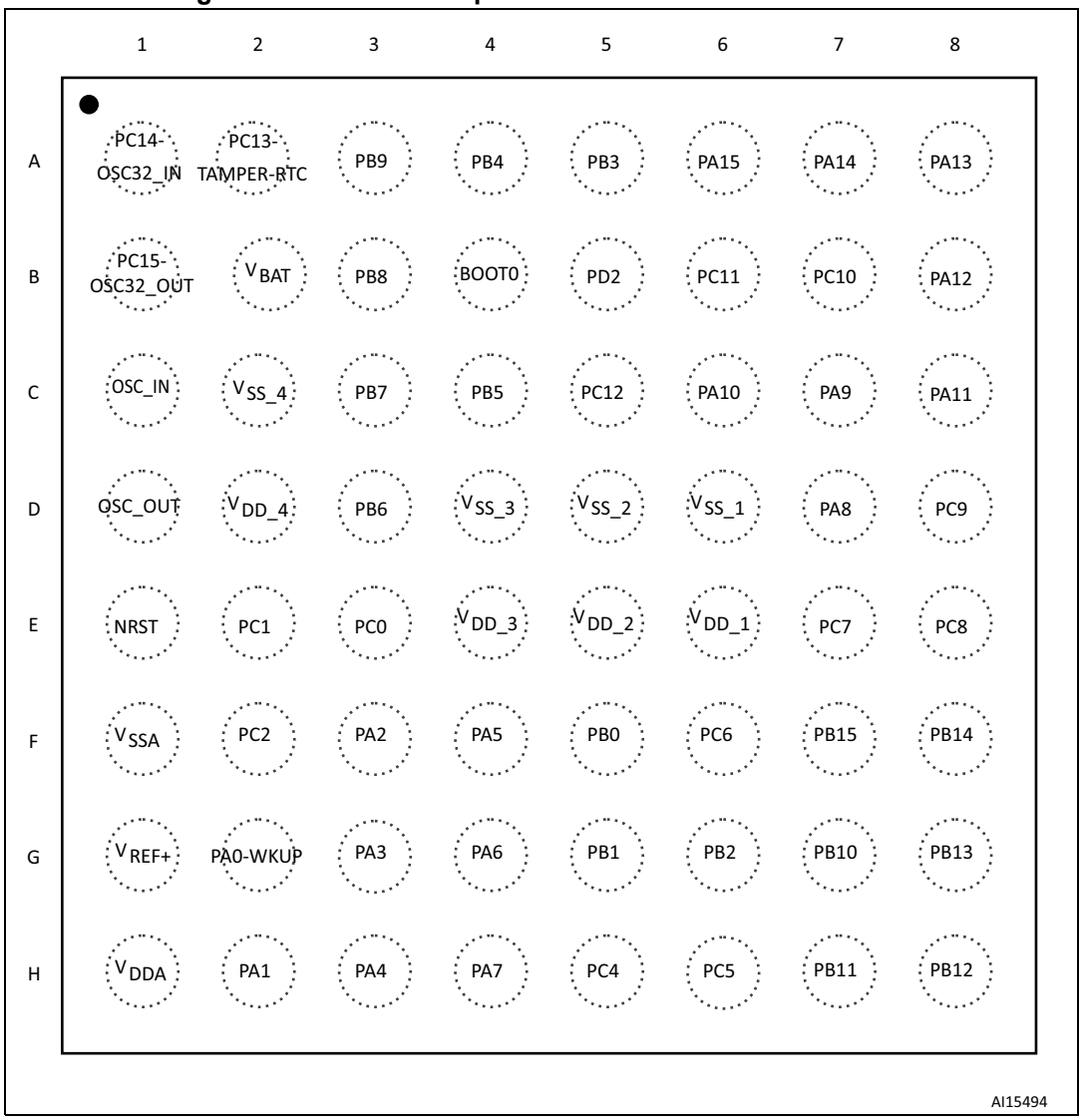
2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

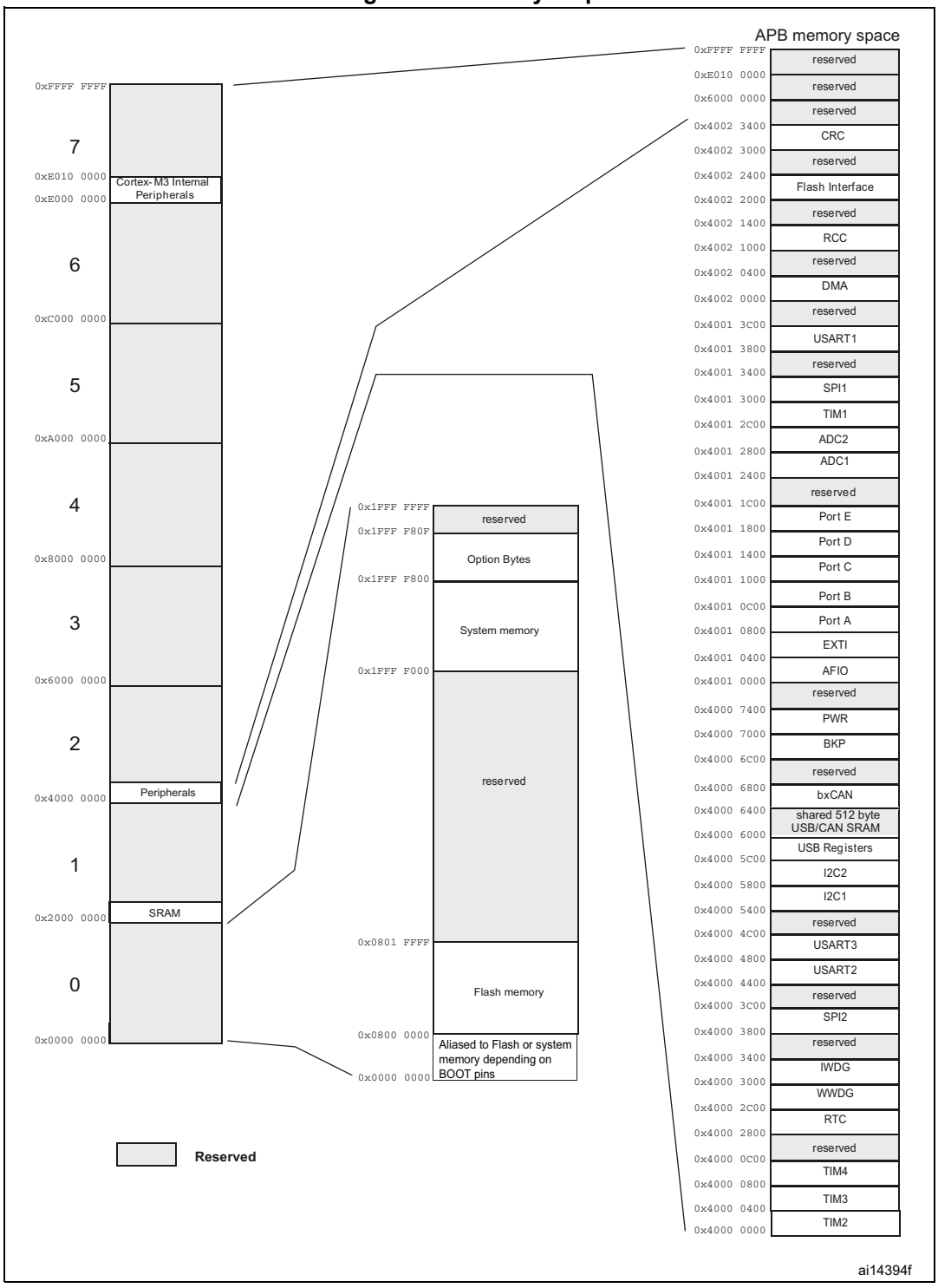
Figure 7. STM32F103xx performance line TFBGA64 ballout



4 Memory mapping

The memory map is shown in *Figure 11*.

Figure 11. Memory map



5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	200	370	µA
		Regulator in Low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	180	340	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9(2)	2.2	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed based on test during characterization.

Figure 18. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

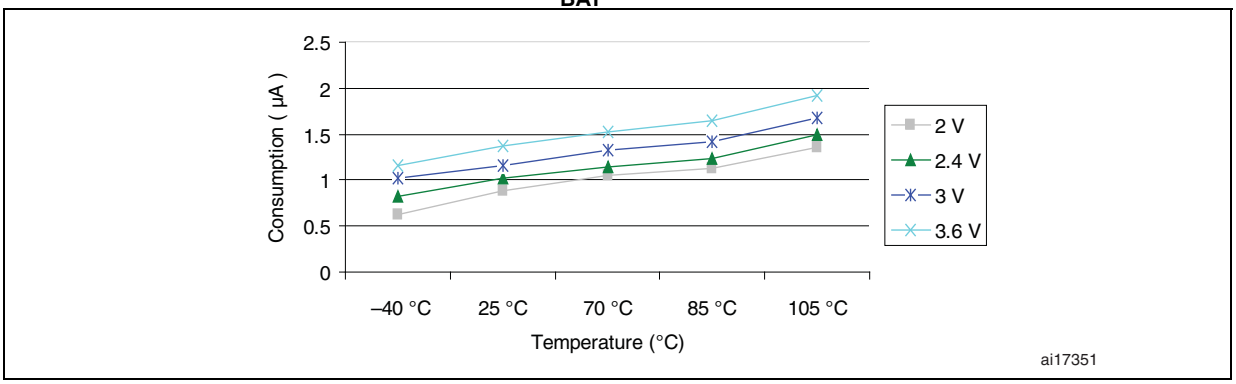


Table 28. Flash memory characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	-	-	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	-	-	Years
		1 kcycle(2) at T_A = 105 °C	10	-	-	
		10 kcycles(2) at T_A = 55 °C	20	-	-	

1. Guaranteed based on test during characterization.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 30*. They are based on the EMS levels and classes defined in application note AN1709.

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
		IO FT(3) input low level voltage	-	-	0.32*(V_{DD}-2V)+0.75 V(1)	
		All I/Os except BOOT0	-	-	0.35V_{DD}(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	0.41*(V_{DD}-2 V)+1.3 V(1)	-	-	
		IO FT(3) input high level voltage	0.42*(V_{DD}-2 V)+1 V(1)	-	-	
		All I/Os except BOOT0	0.65V_{DD}(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed based on test during characterization.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

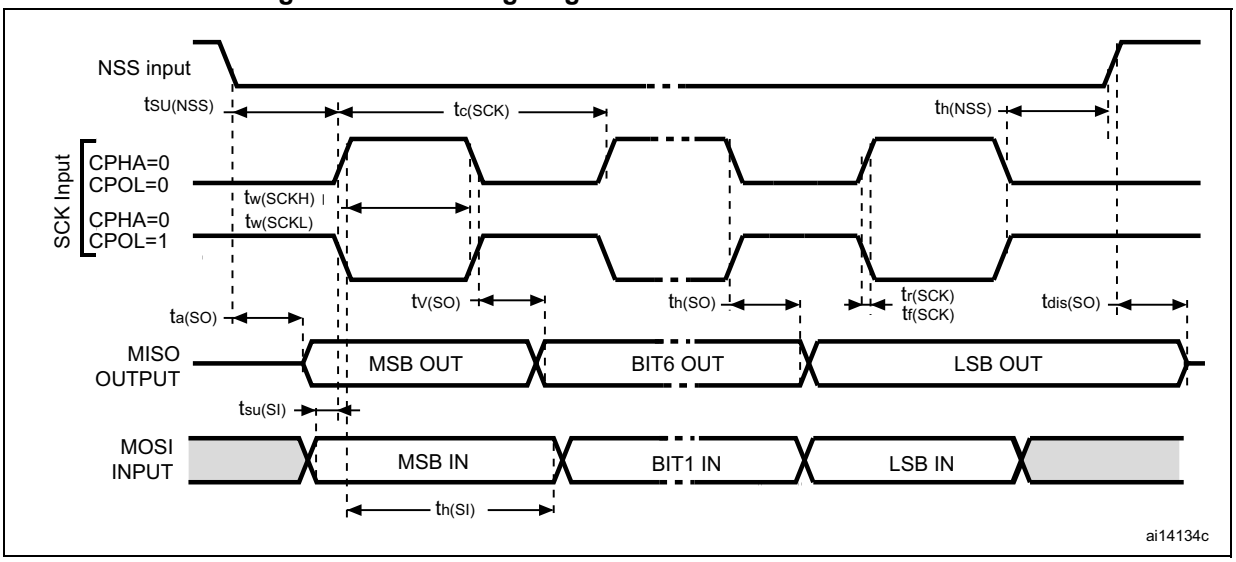
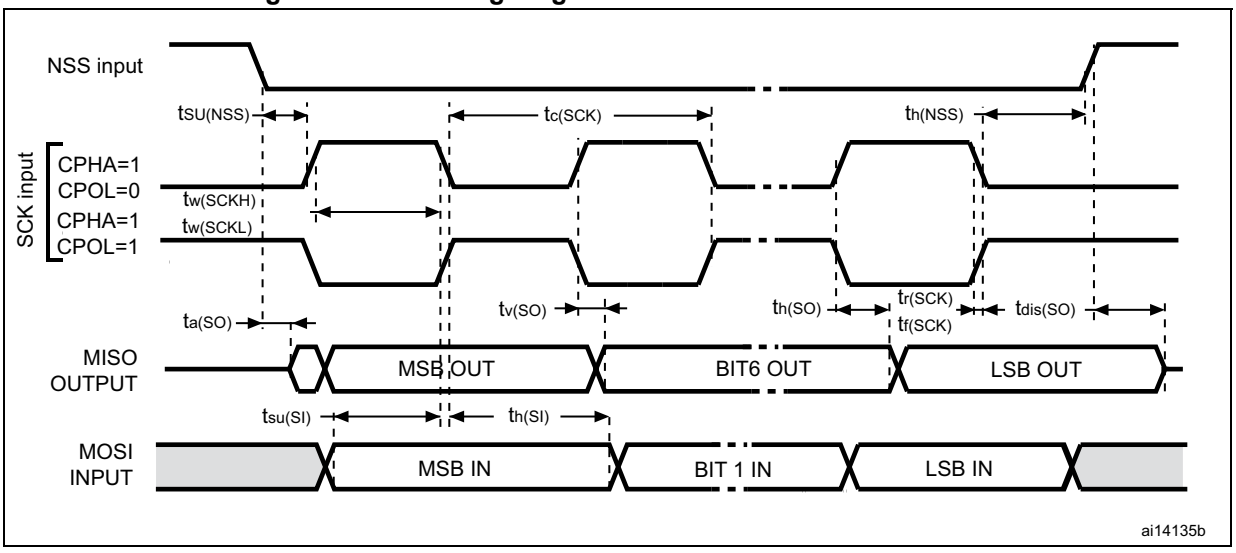
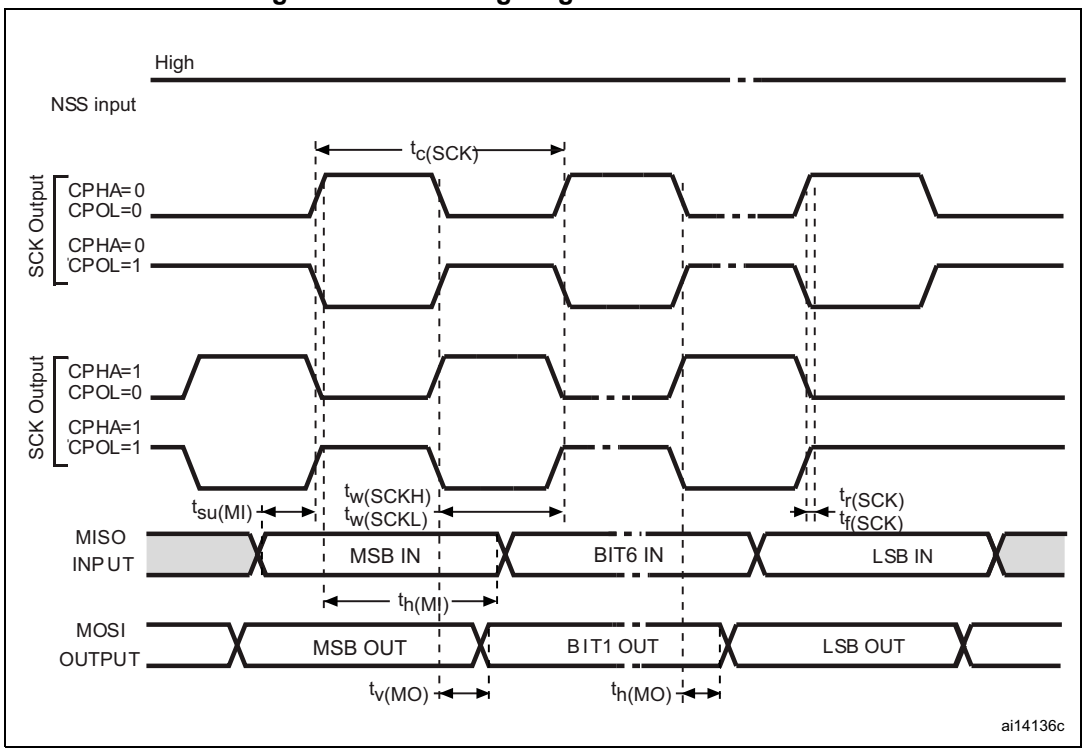


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 43. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 44. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers

Figure 36. USB timings: definition of data signal rise and fall time

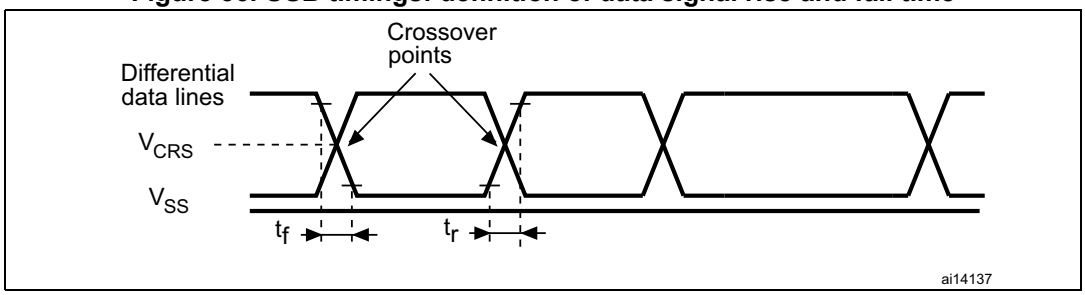


Table 45. USB: Full-speed electrical characteristics(1)

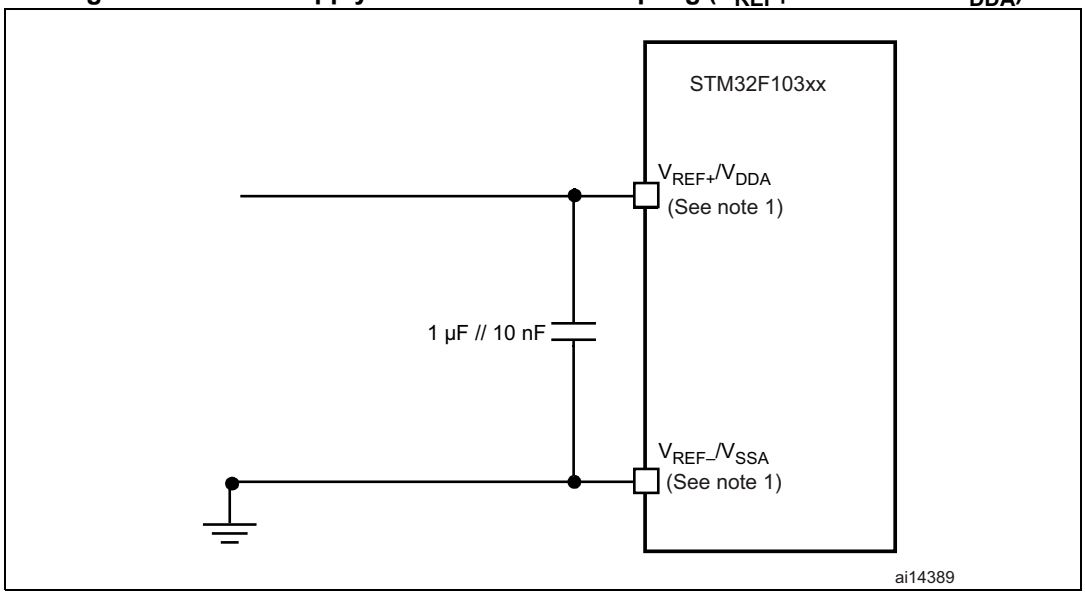
Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics					
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Section 7 (version 2.0).

5.3.17 CAN (controller area network) interface

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Figure 40. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

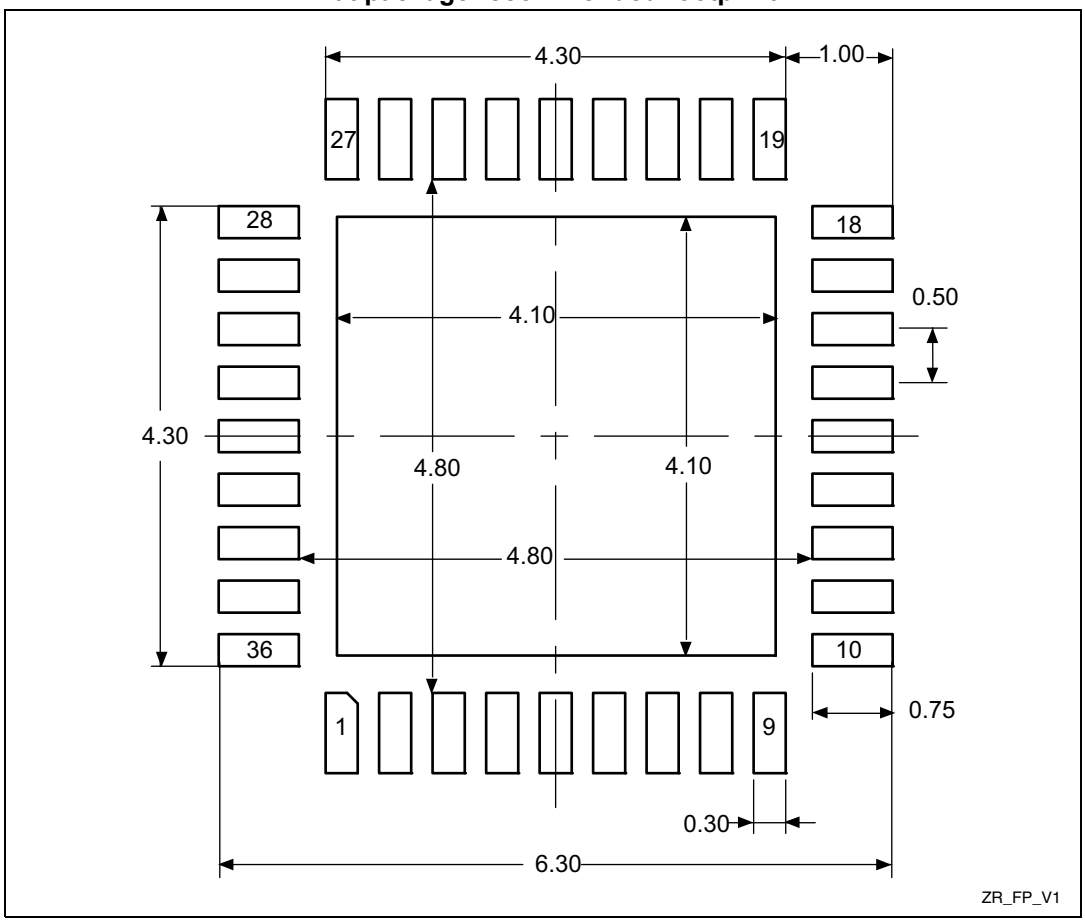
5.3.19 Temperature sensor characteristics

Table 50. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed based on test during characterization.
2. Guaranteed by design.
3. Shortest sampling time can be determined in the application by multiple iterations.

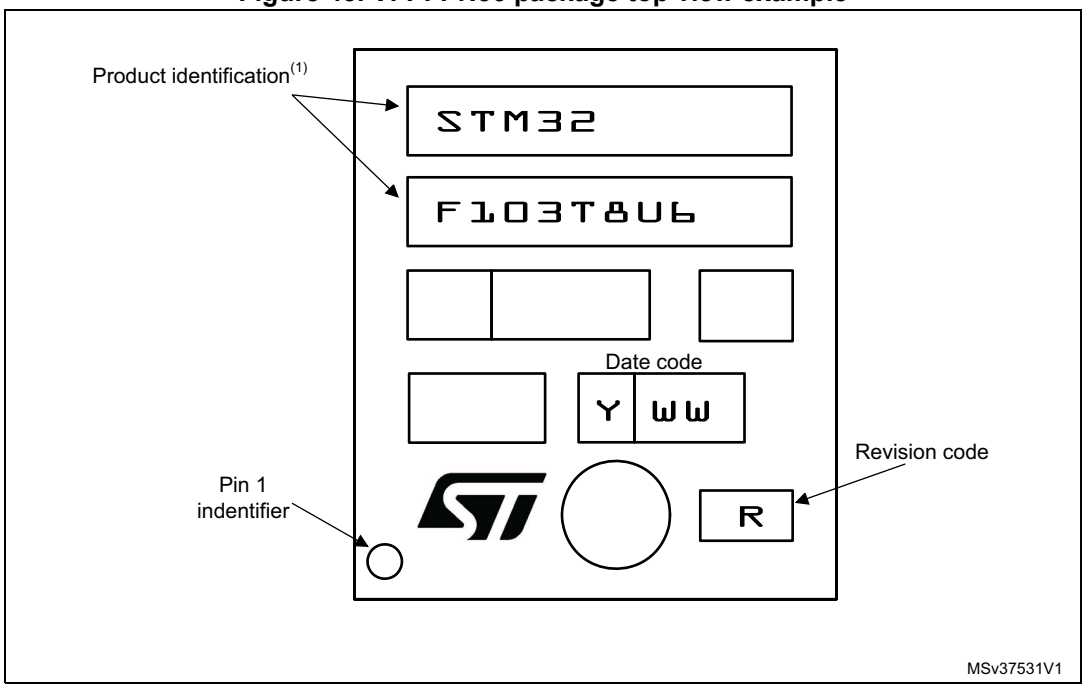
Figure 42. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

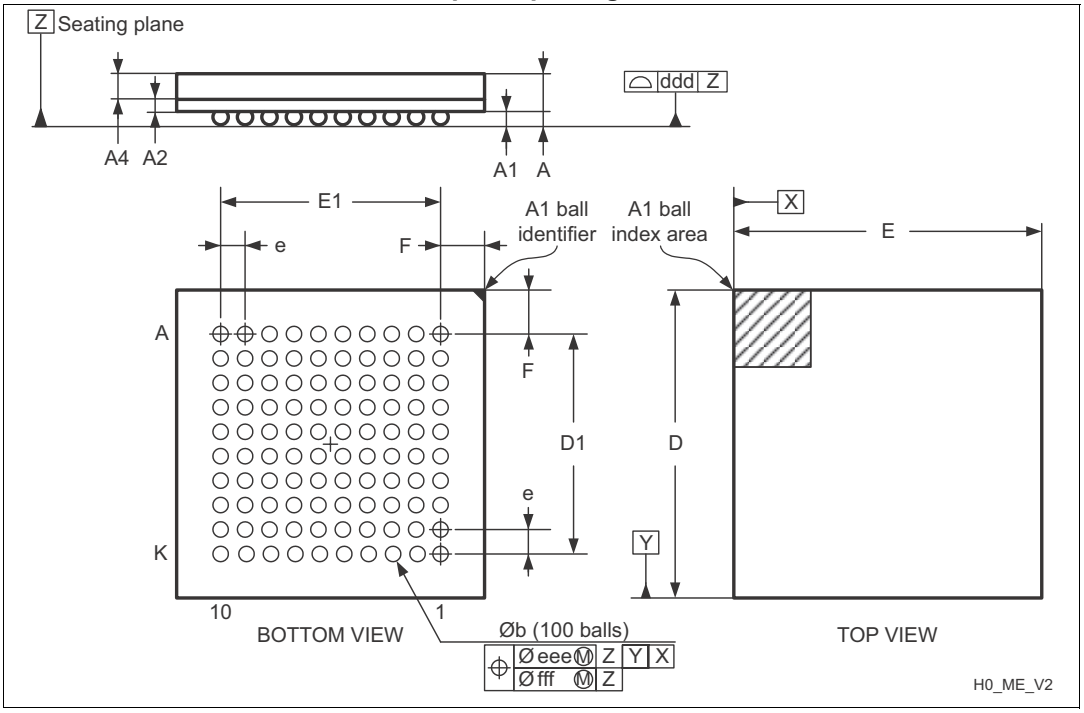
Figure 43. VFPFPN36 package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.3 LFBGA100 10 x 10 mm, low-profile fine pitch ball grid array package information

Figure 47. LFBGA100 - 100-ball low-profile fine pitch ball grid array, 10 x10 mm, 0.8 mm pitch, package outline



1. Drawing is not to scale.

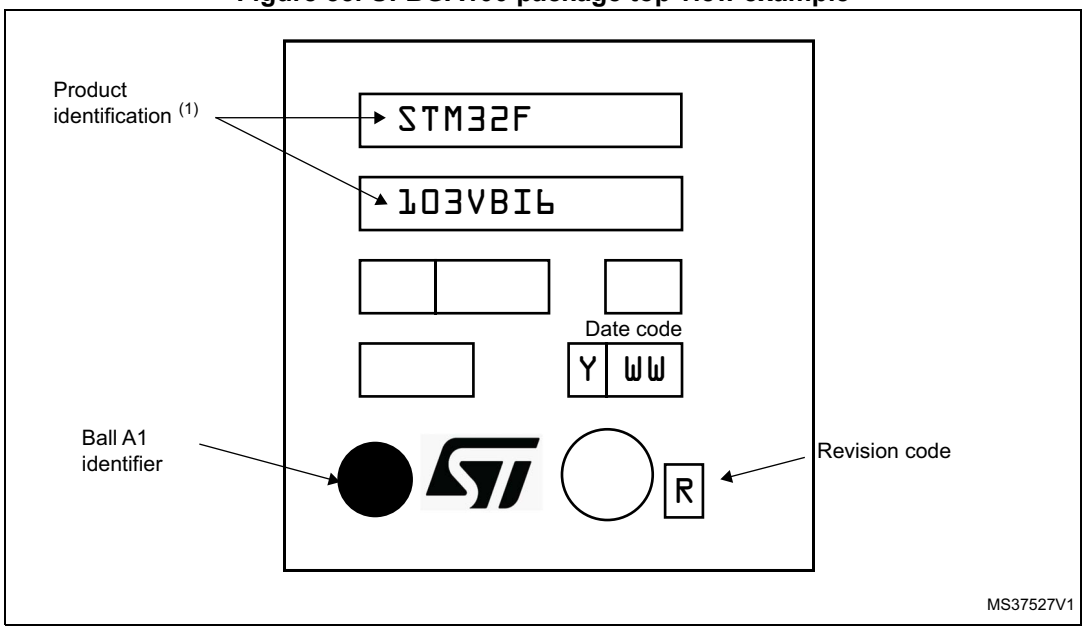
Table 53. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.700	-	-	0.0669
A1	0.270	-	-	0.0106	-	-
A2	-	0.300	-	-	0.0118	-
A4	-	-	0.800	-	-	0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	7.200	-	-	0.2835	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	1.400	-	-	0.0551	-
ddd	-	-	0.120	-	-	0.0047

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

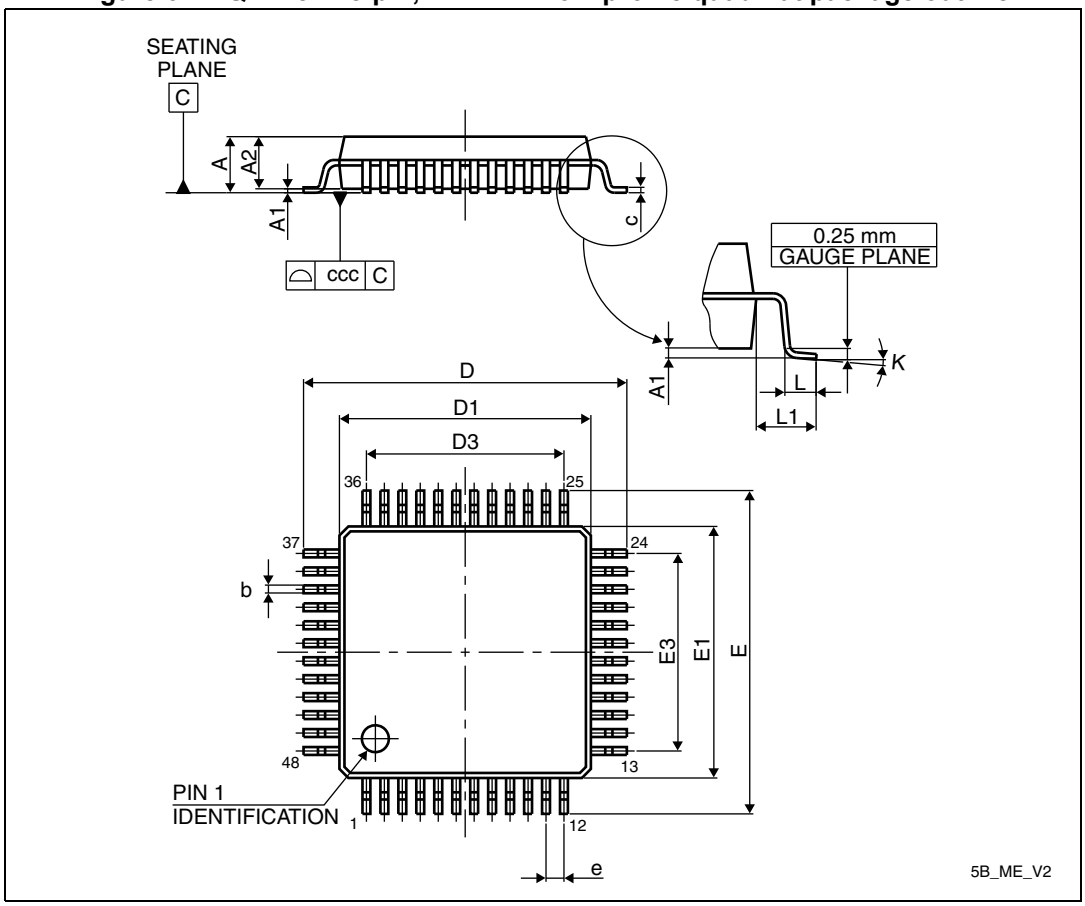
Figure 55. UFBGA100 package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.8 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 62. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 61. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

Table 64. Document revision history (continued)

Date	Revision	Changes
19-Apr-2011	13	Updated footnotes below *Table 6: Voltage characteristics on page 37* and *Table 7: Current characteristics on page 37* Updated tw min in *Table 20: High-speed external user clock characteristics on page 51* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 54* Added *Section 5.3.12: I/O current injection characteristics* Updated *Section 5.3.13: I/O port characteristics*
07-Dec-2012	14	Added UFBGA100 7 x 7 mm. Updated *Figure 59: LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline* to add pin 1 identification.
14-May-2013	15	Replaced VQFN48 package with UQFN48 in cover page packages, *Table 2: STM32F103xx medium-density device features and peripheral counts*, *Figure 9: STM32F103xx performance line UFQFPN48 pinout*, *Table 2: STM32F103xx medium-density device features and peripheral counts*, *Table 56: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, *Table 63: Ordering information scheme* and updated *Table 62: Package thermal characteristics* Added footnote for TFBGA ADC channels in *Table 2: STM32F103xx medium-density device features and peripheral counts* Updated 'All GPIOs are high current...' in *Section 2.3.21: GPIOs (general-purpose inputs/outputs)* Updated *Table 5: Medium-density STM32F103xx pin definitions* Corrected Sigma letter in *Section 5.1.1: Minimum and maximum values* Removed the first sentence in *Section 5.3.16: Communications interfaces* Added 'V_{IN}' in *Table 9: General operating conditions* Updated first sentence in *Output driving current* Added note *5.* in *Table 24: HSI oscillator characteristics* Updated 'V_{IL}' and 'V_{IH}' in *Table 35: I/O static characteristics* Added notes to *Figure 26: Standard I/O input characteristics - CMOS port*, *Figure 27: Standard I/O input characteristics - TTL port*, *Figure 28: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 29: 5 V tolerant I/O input characteristics - TTL port* Updated *Figure 32: I2C bus AC waveforms and measurement circuit* Updated note *2.* and *3.*,removed note "the device must internally..." in *Table 40: I2C characteristics* Updated title of *Table 41: SCL frequency (fPCLK1= 36 MHz.,VDD_I2C = 3.3 V)* Updated note *2.* in *Table 49: ADC accuracy*