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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-VFQFPN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103tbu6tr

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F103xx medium-density performance line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The devices operate from a 2.0 to 3.6 V power supply. They are available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

3 Pinouts and pin description

Figure 3. STM32F103xx performance line LFBGA100 ballout

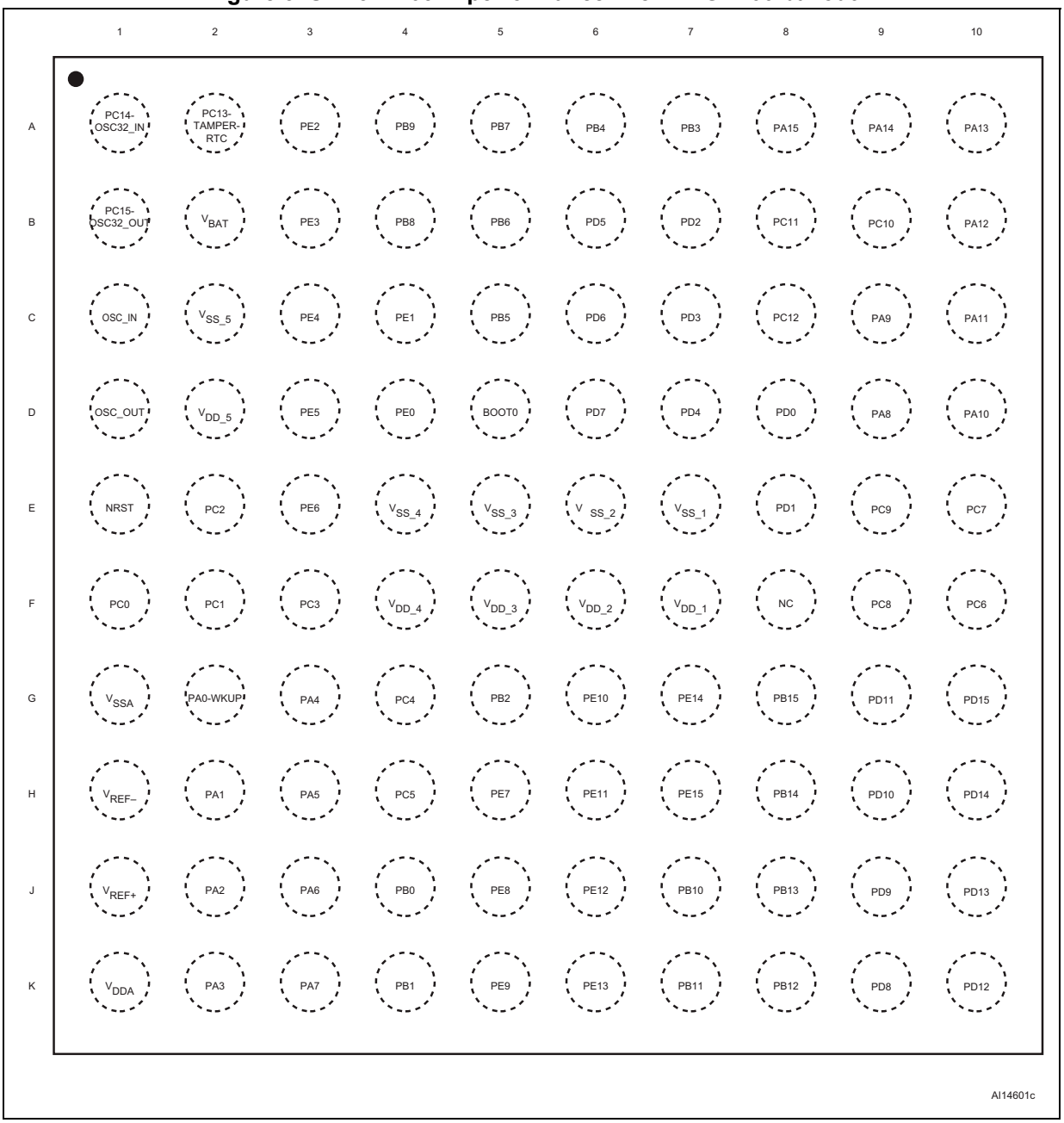


Figure 5. STM32F103xx performance line UFBGA100 pinout

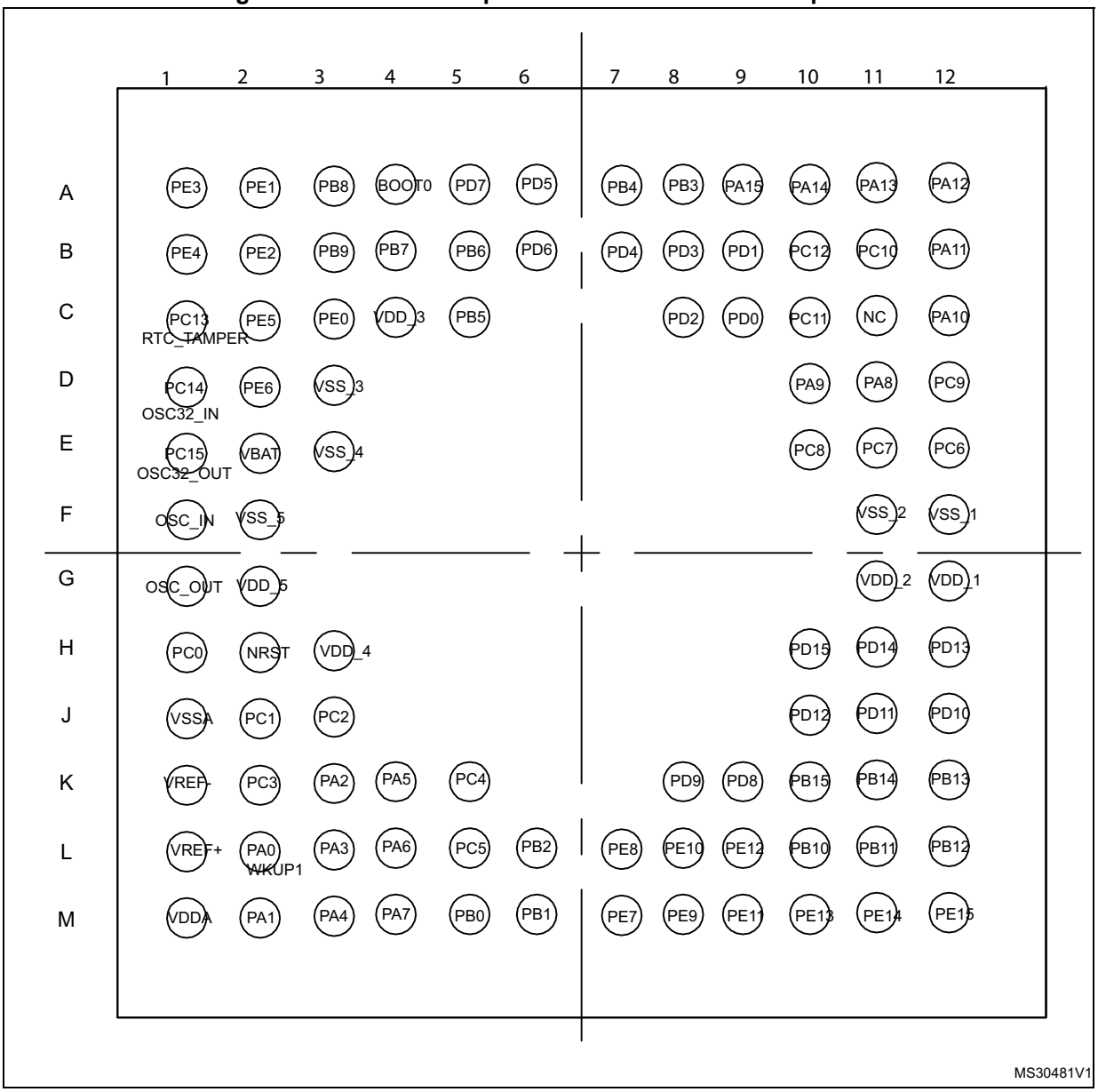


Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins							Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
H9	J12	-	-	-	57	-	PD10	I/O	FT	PD10	-	USART3_CK
G9	J11	-	-	-	58	-	PD11	I/O	FT	PD11	-	USART3_CTS
K10	J10	-	-	-	59	-	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
J10	H12	-	-	-	60	-	PD13	I/O	FT	PD13	-	TIM4_CH2
H10	H11	-	-	-	61	-	PD14	I/O	FT	PD14	-	TIM4_CH3
G10	H10	-	-	-	62	-	PD15	I/O	FT	PD15	-	TIM4_CH4
F10	E12	-	F6	37	63	-	PC6	I/O	FT	PC6	-	TIM3_CH1
E10	E11		E7	38	64	-	PC7	I/O	FT	PC7	-	TIM3_CH2
F9	E10		E8	39	65	-	PC8	I/O	FT	PC8	-	TIM3_CH3
E9	D12	-	D8	40	66	-	PC9	I/O	FT	PC9	-	TIM3_CH4
D9	D11	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(9)/ MCO	-
C9	D10	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX(9)/ TIM1_CH2(9)	-
D10	C12	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX(9)/ TIM1_CH3(9)	-
C10	B12	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(9)/ USBDM/ TIM1_CH4(9)	-
B10	A12	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX(9) /USBDP TIM1_ETR(9)	-
A10	A11	34	A8	46	72	25	PA13	I/O	FT	JTMS/SWDIO	-	PA13
F8	C11	-	-	-	73	-	Not connected					-
E6	F11	35	D5	47	74	26	V_{SS_2}	S	-	V_{SS_2}	-	-
F6	G11	36	E5	48	75	27	V_{DD_2}	S	-	V_{DD_2}	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

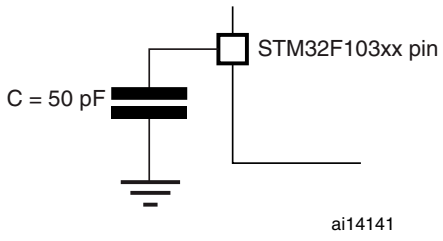


Figure 13. Pin input voltage

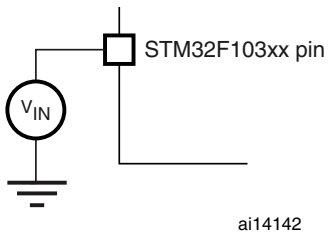


Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	36	
f_{PCLK2}	Internal APB2 clock frequency	-		0	72	
V_{DD}	Standard operating voltage	-		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)		2	3.6	
	Analog operating voltage (ADC used)			2.4	3.6	
V_{BAT}	Backup operating voltage	-		1.8	3.6	
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	V
		FT IO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LFBGA100		-	454	mW
		LQFP100		-	434	
		UFBGA100		-	339	
		TFBGA64		-	308	
		LQFP64		-	444	
		LQFP48		-	363	
		UFQFPN48		-	624	
		VFQFPN36		-	1000	

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	30	32	mA
			48 MHz	20	20.5	
			36 MHz	15.5	16	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	
		External clock(2), all peripherals disabled	72 MHz	7.5	8	
			48 MHz	6	6.5	
			36 MHz	5	5.5	
			24 MHz	4.5	5	
			16 MHz	4	4.5	
			8 MHz	3	4	

1. Based on characterization, tested in production at $V_{DD\ max}$, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1) (2) (continued)

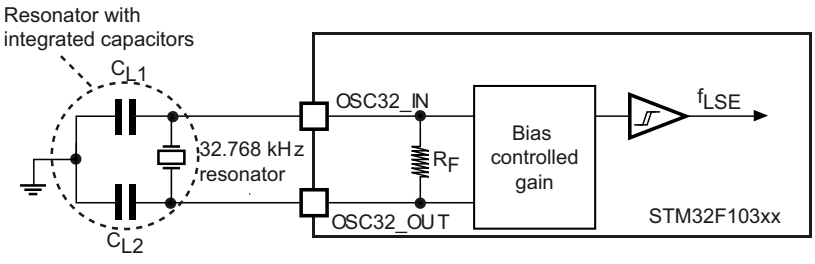
Symbol	Parameter	Conditions	-	Min	Typ	Max	Unit
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed based on test during characterization.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 25. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 34*

Table 34. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

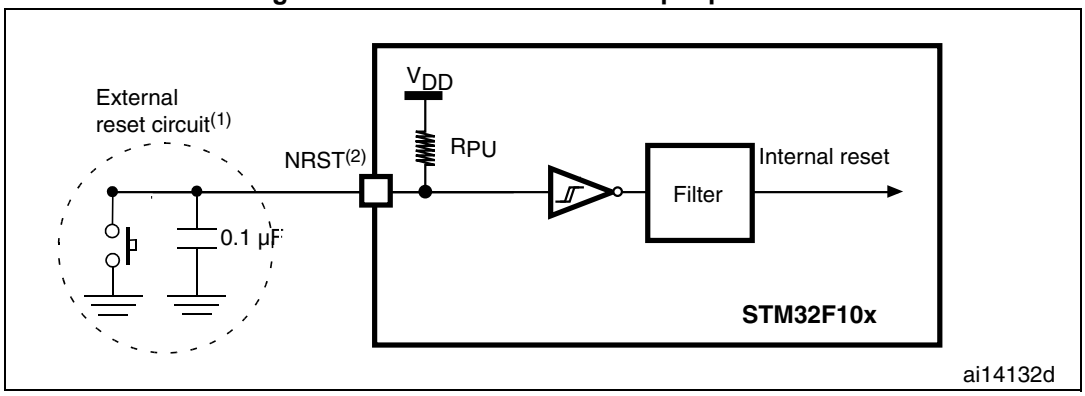
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2), I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed based on test during characterization.

Figure 31. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 38*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in *Table 39* are guaranteed by design.

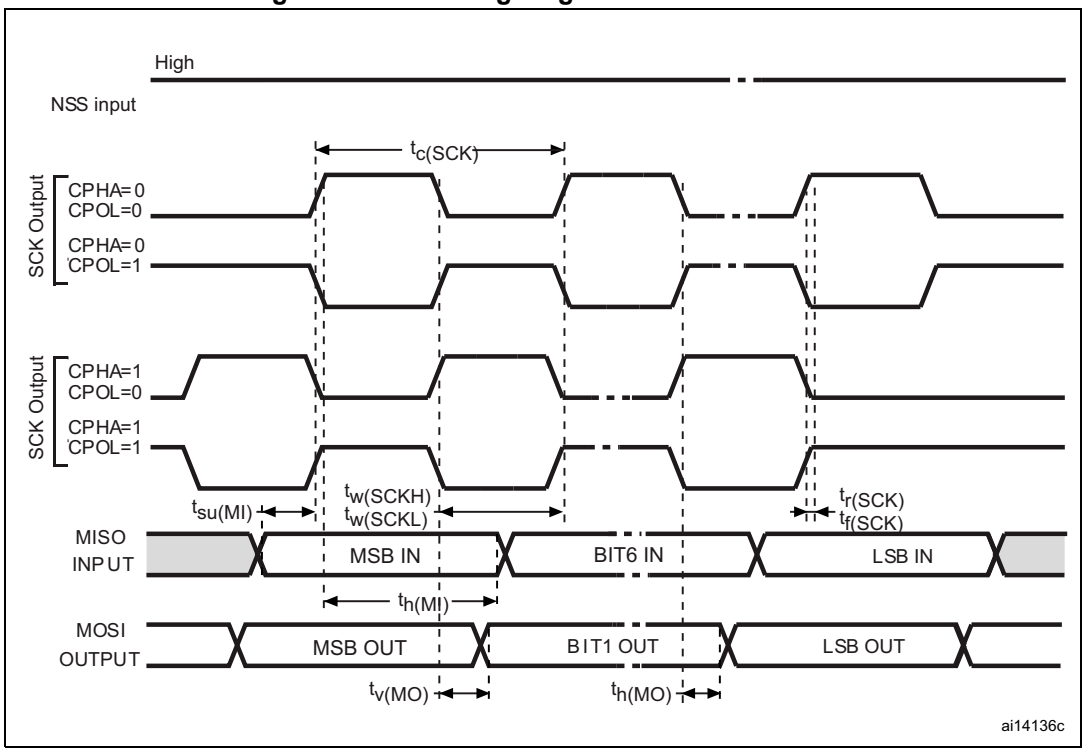
Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 39. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

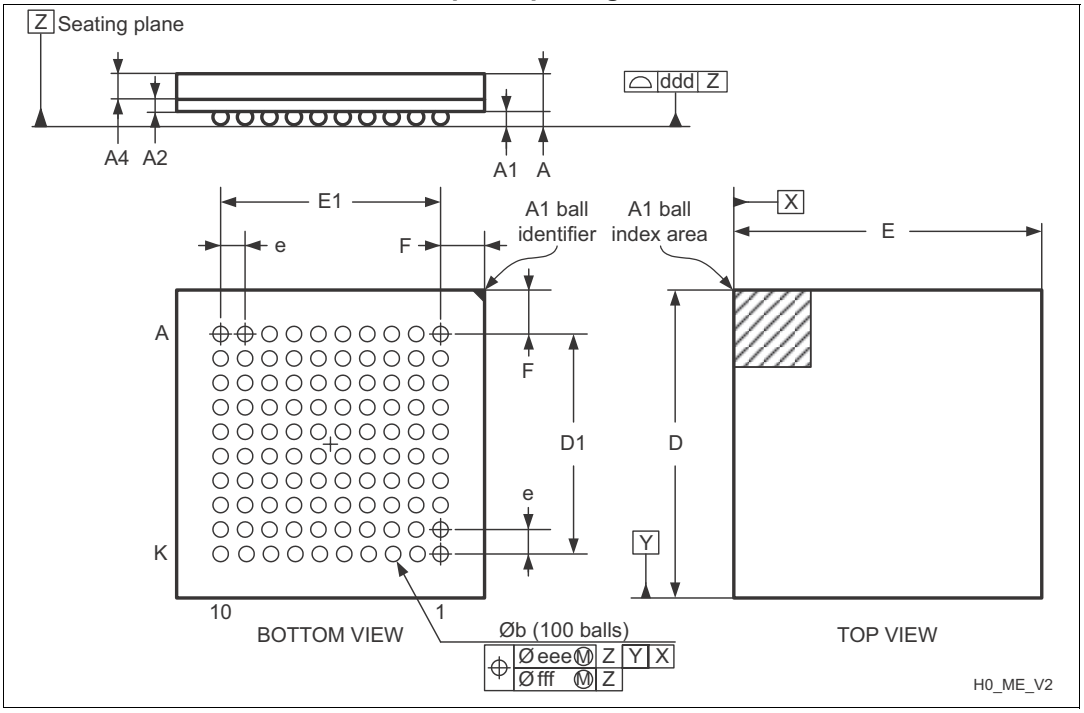
Table 43. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

6.3 LFBGA100 10 x 10 mm, low-profile fine pitch ball grid array package information

Figure 47. LFBGA100 - 100-ball low-profile fine pitch ball grid array, 10 x10 mm, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 53. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.700	-	-	0.0669
A1	0.270	-	-	0.0106	-	-
A2	-	0.300	-	-	0.0118	-
A4	-	-	0.800	-	-	0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	7.200	-	-	0.2835	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	1.400	-	-	0.0551	-
ddd	-	-	0.120	-	-	0.0047

Table 53. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. LFBGA100 – 100-ball low-profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint

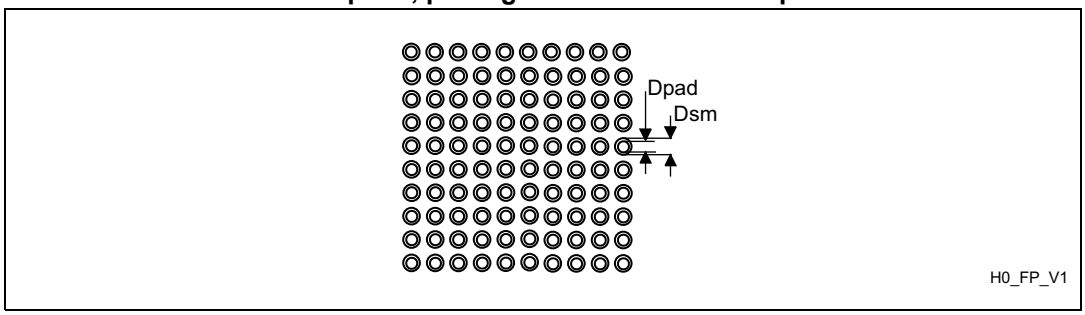


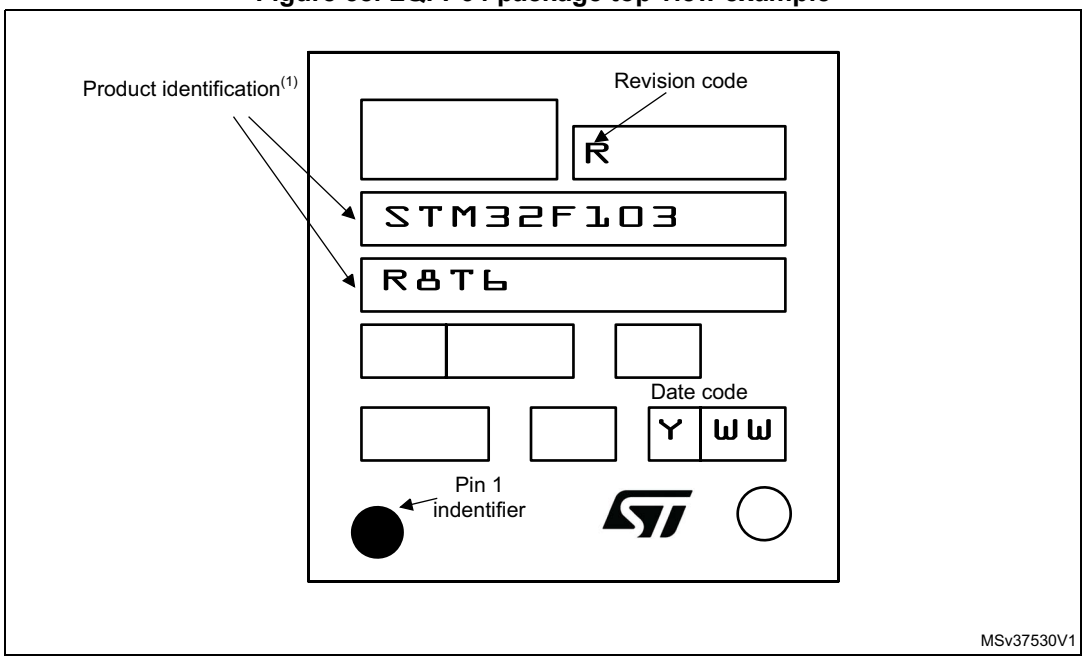
Table 54. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 58. LQFP64 package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 59. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 60. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package recommended footprint

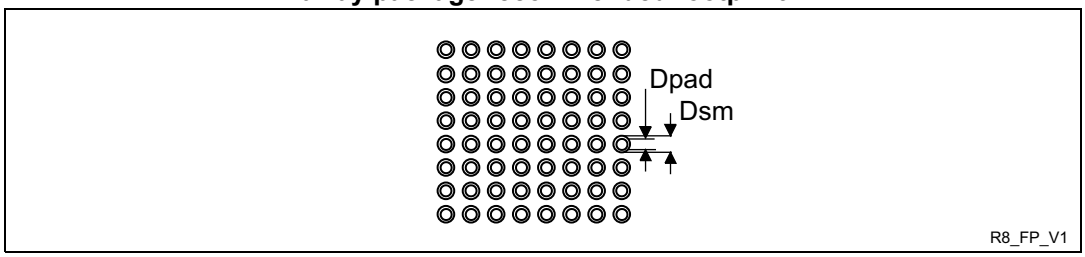


Table 60. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 1.125 mm
Pad trace width	0.100 mm

Using the values obtained in *Table 62* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 63: Ordering information scheme*).

Figure 65. LQFP100 P_D max vs. T_A

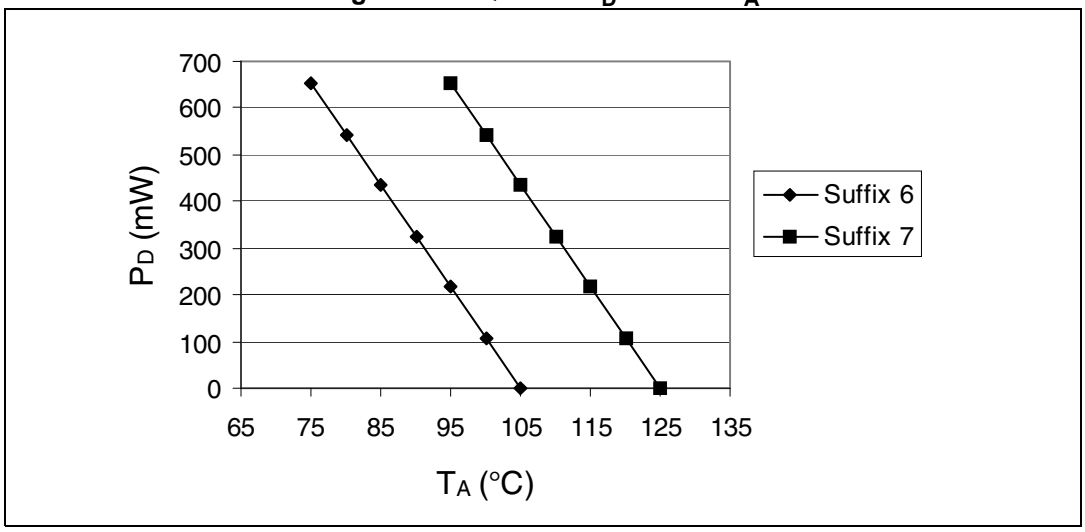


Table 64. Document revision history (continued)

Date	Revision	Changes
22-Nov-2007	4	Document status promoted from preliminary data to datasheet. The STM32F103xx is USB certified. Small text changes. *Power supply schemes on page 15* modified. Number of communication peripherals corrected for STM32F103Tx and number of GPIOs corrected for LQFP package in *Table 2: STM32F103xx medium-density device features and peripheral counts*. Main function and default alternate function modified for PC14 and PC15 in, *Note 6* added and Remap column added in *Table 5: Medium-density STM32F103xx pin definitions*. V_{DD}–V_{SS} ratings and *Note 1* modified in *Table 6: Voltage characteristics*, *Note 1* modified in *Table 7: Current characteristics*. *Note 1* and *Note 2* added in *Table 11: Embedded reset and power control block characteristics*. I_{DD} value at 72 MHz with peripherals enabled modified in *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM*. I_{DD} value at 72 MHz with peripherals enabled modified in *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 44*. I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum values added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. Note added in *Table 17 on page 48* and *Table 18 on page 49*. ADC1 and ADC2 consumption and notes modified in *Table 19: Peripheral current consumption*. $t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in *Table 22* and *Table 23*, respectively. Maximum values removed from *Table 26: Low-power mode wakeup timings*. t_{RET} conditions modified in *Table :* . *Figure 14: Power supply scheme* corrected. *Figure 20: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* added. Note removed below *Figure 33: SPI timing diagram - slave mode and CPHA = 0*. Note added below *Figure 34: SPI timing diagram - slave mode and CPHA = 1(1)*. Details on unused pins removed from *General input/output characteristics on page 62*. *Table 42: SPI characteristics* updated. *Table 43: USB startup time* added. V_{AIN}, $t_{lat\ and}$ t_{latr} modified, note added and I_{lkg} removed in *Table 46: ADC characteristics*. Test conditions modified and note added in *Table 49: ADC accuracy*. Note added below *Table 47* and *Table 50*. Inch values corrected in *Table 55: LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data*, *Table 58: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data* and *Table 60: LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data*. Θ_{JA}value for VFQFPN36 package added in *Table 62: Package thermal characteristics*. Order codes replaced by *Section 7: Ordering information scheme*. MCU ‘s operating conditions modified in *Typical current consumption on page 47*. Avg_Slope and V_{25} modified in *Table 50: TS characteristics*. *I2C interface characteristics on page 69* modified. Impedance specified in *A.4: Voltage glitch on ADC input 0 on page 81*.

Table 64. Document revision history (continued)

Date	Revision	Changes
19-Apr-2011	13	Updated footnotes below *Table 6: Voltage characteristics on page 37* and *Table 7: Current characteristics on page 37* Updated tw min in *Table 20: High-speed external user clock characteristics on page 51* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 54* Added *Section 5.3.12: I/O current injection characteristics* Updated *Section 5.3.13: I/O port characteristics*
07-Dec-2012	14	Added UFBGA100 7 x 7 mm. Updated *Figure 59: LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline* to add pin 1 identification.
14-May-2013	15	Replaced VQFN48 package with UQFN48 in cover page packages, *Table 2: STM32F103xx medium-density device features and peripheral counts*, *Figure 9: STM32F103xx performance line UFQFPN48 pinout*, *Table 2: STM32F103xx medium-density device features and peripheral counts*, *Table 56: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, *Table 63: Ordering information scheme* and updated *Table 62: Package thermal characteristics* Added footnote for TFBGA ADC channels in *Table 2: STM32F103xx medium-density device features and peripheral counts* Updated 'All GPIOs are high current...' in *Section 2.3.21: GPIOs (general-purpose inputs/outputs)* Updated *Table 5: Medium-density STM32F103xx pin definitions* Corrected Sigma letter in *Section 5.1.1: Minimum and maximum values* Removed the first sentence in *Section 5.3.16: Communications interfaces* Added 'V_{IN}' in *Table 9: General operating conditions* Updated first sentence in *Output driving current* Added note *5.* in *Table 24: HSI oscillator characteristics* Updated 'V_{IL}' and 'V_{IH}' in *Table 35: I/O static characteristics* Added notes to *Figure 26: Standard I/O input characteristics - CMOS port*, *Figure 27: Standard I/O input characteristics - TTL port*, *Figure 28: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 29: 5 V tolerant I/O input characteristics - TTL port* Updated *Figure 32: I2C bus AC waveforms and measurement circuit* Updated note *2.* and *3.*,removed note "the device must internally..." in *Table 40: I2C characteristics* Updated title of *Table 41: SCL frequency (fPCLK1= 36 MHz.,VDD_I2C = 3.3 V)* Updated note *2.* in *Table 49: ADC accuracy*