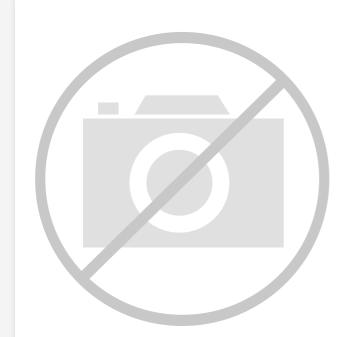
Epson Hectronics America Inc-Semiconductor Div - <u>S1C17W13F002100 Datasheet</u>



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	S1C17
Core Size	16-Bit
Speed	4.2MHz
Connectivity	I ² C, IrDA, SSI, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	-
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/epson/s1c17w13f002100

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

S1C17W12/W13 (rev1.1)



16-bit Single Chip Microcontroller

- Low voltage operation from 1.2 V with a single alkaline or silver oxide button battery.
- Ultra low standby power consumption (0.3 µA during HALT state in super economy mode)
- Equipped with an LCD driver capable of driving an 18–26 SEG × 4 COM LCD panel.
- Various kinds of serial interfaces (UART, SPI, I²C)

DESCRIPTIONS

The S1C17W12/W13 is a 16-bit MCU that features low-voltage operation from 1.2 V even though Flash memory is included. This IC has realized an excellent low power operation that is better than Seiko Epson's 4-bit MCUs by adopting a high-efficiency DC-DC converter that generates a constant voltage to drive internal circuits. It includes a real-time clock, a stopwatch, an LCD driver, and a PWM timer capable of being used to generate drive waveforms for a motor driver as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an LCD display.

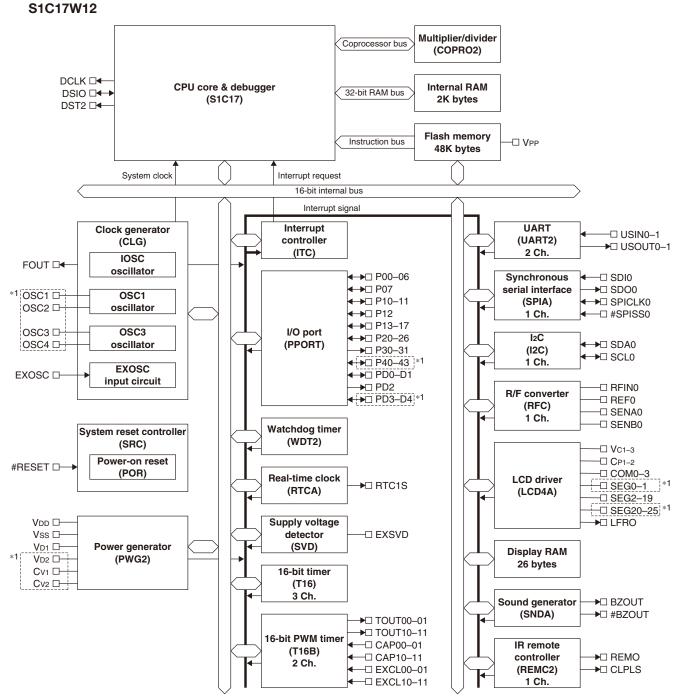
FEATURES

Model	S1C1	17W12	S1C17W13							
	SQFN7-48pin	Chip	TQFP12-48pin	SQFN7-48pin	QFP13-64pin or chip					
CPU										
CPU core	Seiko Epson origina	al 16-bit RISC CPU c	ore S1C17							
Other	On-chip debugger									
Embedded Flash memory										
Capacity	48K bytes (for both	instructions and dat	a)							
Erase/program count	1,000 times (min.) *	Programming by the	e debugging tool ICD	mini						
Other	Security function to	protect from reading	g/programming by IC	Dmini						
	On-board program	ming function using I	CDmini							
	* An external smoo	thing capacitor is rec	quired.							
Embedded RAM										
Capacity	2K bytes									
Embedded display RAM										
Capacity	26 bytes									
Clock generator (CLG)										
System clock source	4 sources (IOSC/OS	SC1/OSC3/EXOSC)								
System clock frequency	1.1 MHz (max.) VDD	= 1.2 to 1.6 V								
(operating frequency)	4.2 MHz (max.) VDD	= 1.6 to 3.6 V								
IOSC oscillator circuit	700 kHz (typ.) embe	edded oscillator								
(boot clock source)	23 µs (max.) starting	g time (time from car	ncelation of SLEEP st	ate to vector table r	ead by the CPU)					
OSC1 oscillator circuit	-	32.768 kHz (typ.) cr	ystal oscillator							
	32 kHz (typ.) embedded oscillator									
	-	Oscillation stop det	ection circuit include	d						
OSC3 oscillator circuit	-	4.2 MHz (max.)		-	4.2 MHz (max.)					
		crystal/ceramic osc	illator		crystal/ceramic oscillator					
	250, 384, 500 kHz,	1, 2, and 4 MHz-swi	tchable embedded o	scillator	1					
	_	2.1 MHz (max.)		_	2.1 MHz (max.)					
		CR oscillator (an ext	ernal R is required)		CR oscillator					
			, ,		(an external R is required)					
EXOSC clock input	4.2 MHz (max.) squ	are or sine wave inp	ut							
Other	Configurable syster	m clock division ratio								
	Configurable syster	m clock used at wake	e up from SLEEP sta	te						
	Operating clock frequency for the CPU and all peripheral circuits is selectable.									

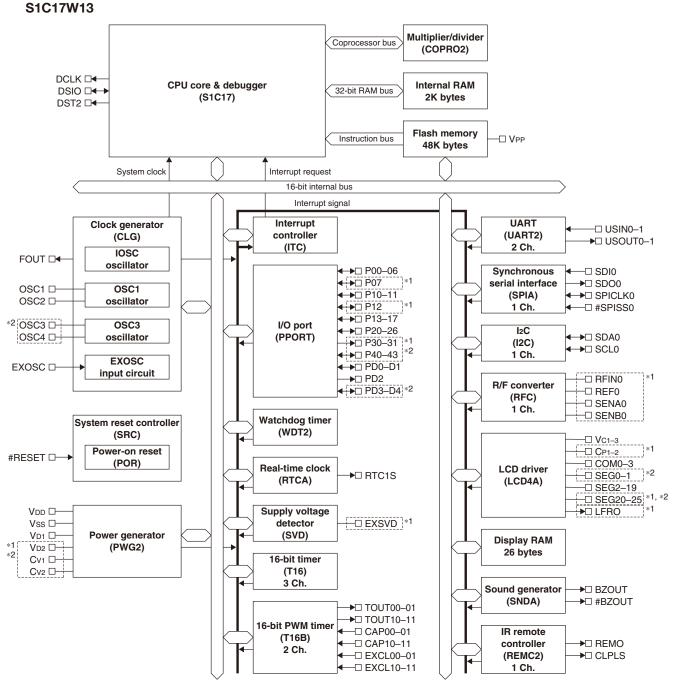
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rammable NMI. 1 Hz counter, s pretical regulation n and stopwaton annels prates the SPIA annels tt counter/captur A waveform ger ber of PWM our evels (1.2 to 3.6 mittent operation prates an internor annels	/reset generation cy second/minute/hour on function for 1-se ch functions master clock. ure function neration function tiput or capture input V)	/cle /day/day of the week cond correction ut ports: 2 ports/char	nel	HS						
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erates an interru annels		ng to the detection le	wolovaluation							
annels	upt or reset accord	ng to the detection le								
		-								
i-rate generato	2 channels									
Baud-rate generator included, IrDA1.0 supported Open drain output, signal polarity, and baud rate division ratio are configurable.										
	signal polarity, and	baud rate division ra	lo are configurable.							
1 channel										
2 to 16-bit variable data length The 16-bit timer (T16) can be used for the baud-rate generator in master mode.										
annel	of call be used for t	ine baud-rate genera	tor in master mode.							
d-rate generato	r included									
Hz to 16 kHz oi	utput frequencies									
Tempo: 16 tempos (30 to 480)										
lur may be spe	cified.									
annel										
imp drive wave	form can be genera	ted for an applicatio	n example.							
EG×	26 SEG ×	20 SEG \times	18 SEG ×	26 SEG \times						
COM (max.)	1–4 COM (max.)	1–4 COM (max.)	1–4 COM (max.)	1-4 COM (max.)						
vels		-								
	•									
ernal voltage ca	n be applied.)	supply	I(External voltage c	an be applied.)						
colletion ton -	with 04 bit count-		CP oppillation turns	with 04 bit counter						
	with 24-bit counters	5 -		with 24-bit counters						
annel			1 channel							
annel o two sensors	can be connected.)		1 channel (Up to two sensors	can be connected.)						
annel	can be connected.) ensors,		1 channel	s can be connected.) sensors,						
	shot output fur 128 Hz to ion: 7 notes/re io: 16 tempo ur may be spe unnel mp drive wave EG × COM (max.) vels ias power supp	tion: 7 notes/rests (Half note/rest f to: 16 tempos (30 to 480) ur may be specified. mp drive waveform can be genera EG × 26 SEG × COM (max.) 1–4 COM (max.)	shot output function : 128 Hz to 16 kHz \approx C3 to C6 tion: 7 notes/rests (Half note/rest to thirty-second note, note) tion: 7 notes/rests (Half note/rest to thirty-second note, note) tion: 7 notes/rests (Half note/rest to thirty-second note, note) tion: 7 notes/rests (Half note/rest to thirty-second note, note) tion: 16 tempos (30 to 480) tur may be specified. unnel mp drive waveform can be generated for an application EG × 26 SEG × 20M (max.) 1–4 COM (max.) turels – ias power supply included External power	shot output function : 128 Hz to 16 kHz \approx C3 to C6 tion: 7 notes/rests (Half note/rest to thirty-second note/rest) too: 16 tempos (30 to 480) ur may be specified. unnel mp drive waveform can be generated for an application example. EG × 26 SEG × 20 SEG × 18 SEG × COM (max.) 1–4 COM (max.) 1–4 COM (max.) 1–4 COM (max.) vels – 16 levels 13 bias power supply included						

Model	S1C1	7W12		S1C17W13							
	SQFN7-48pin	Chip	TQFP12-48pin	SQFN7-48pin	QFP13-64pin or chip						
Multiplier/divider (COPRO2)											
Arithmetic functions	16-bit × 16-bit mult	inlier									
	16-bit × 16-bit + 32-bit multiply and accumulation unit										
	32-bit ÷ 32-bit divid										
Reset											
#RESET pin	Reset when the res	et nin is set to low									
Power-on reset	Reset at power on.										
Key entry reset) to P01/P02/P03 ke	vs are pressed simul	taneously (can be e	nabled/disabled us-						
	ing a register).										
Watchdog timer reset	Reset when the wa	tchdog timer overflov	vs (can be enabled/o	disabled using a regi	ster).						
Supply voltage detector reset	Reset when the sup register).	set when the supply voltage detector detects the set voltage level (can be enabled/disabled using a ster).									
Interrupt											
Non-maskable interrupt	4 systems (Reset, a	ddress misaligned in	terrupt, debug, NMI								
Programmable external interrupt	1 system (8 levels)										
Programmable internal interrupt	18 systems		17 systems	18 systems							
	(8 levels)		(8 levels)	(8 levels)							
Power supply voltage											
VDD operating voltage	1.2 to 3.6 V										
VDD operating voltage for Flash programming	2.4 to 3.6 V (VPP = 7	7.5 V external power	supply is required.)								
VDD operating voltage for super	_	2.5 to 3.6 V	-		2.5 to 3.6 V						
economy mode		2.0 10 0.0 V			2.0 10 0.0 V						
Operating temperature											
Operating temperature range	-40 to 85 °C										
Current consumption (Typ. value)											
SLEEP mode	0.15 μA										
		= OFF, OSC3 = OFF									
HALT mode	1.5 µA	0.5 μA									
	OSC1 = 32 kHz	OSC1 = 32.768 kHz									
	(internal oscillator),										
	RTC = ON	RTC = ON									
	_	0.3 µA		_	0.3 μA						
		OSC1 = 32.768 kHz			OSC1 = 32.768 kHz						
		(crystal oscillator),			(crystal oscillator),						
		RTC = ON,			RTC = ON,						
		super economy			super economy						
		mode			mode						
RUN mode	5 µA	4 µA									
	OSC1 = 32 kHz	OSC1 = 32.768 kHz	1								
	(internal oscillator),	(crystal oscillator),									
	RTC = ON,	RTC = ON,									
	CPU = OSC1	CPU = OSC1			·						
	-	2 μΑ		-	2 μΑ						
		OSC1 = 32.768 kHz			OSC1 = 32.768 kHz						
		(crystal oscillator),			(crystal oscillator),						
		RTC = ON,			RTC = ON,						
		CPU = OSC1,			CPU = OSC1,						
		super economy			super economy						
		mode			mode						
	140 μA		1 00 700 kH /								
Chipping form	10503 = 1 MHz (cer	amic oscillator), OSC	1 = 32.768 KHZ (Crys	stal oscillator), RIC =	= ON, GPU $=$ OSC3						
Shipping form	SOENIZ 400:0 /1	h pitch: 0.5 mm)									
0	SQFN7-48pin (Lead										
2	Die form (Pad pitch	. ου μπι (min.))	OED12 64min /L cod	nitch: 0.5 mm)							
3		-	QFP13-64pin (Lead								
4		_	TQFP12-48pin (Lea	u pilon: 0.5 mm)							

BLOCK DIAGRAMS



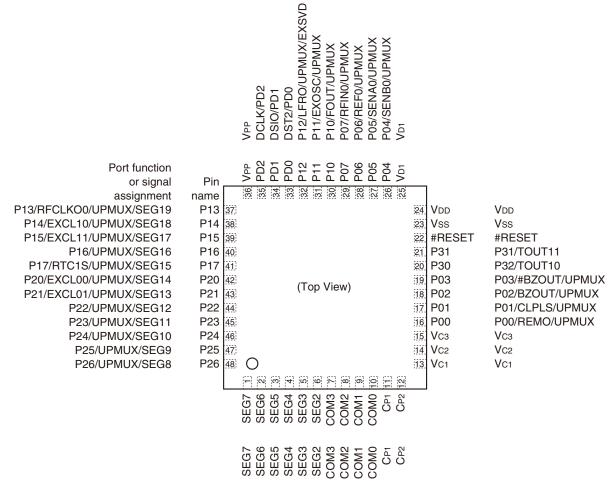
*1 These pins do not exist in the SQFN7-48pin package.



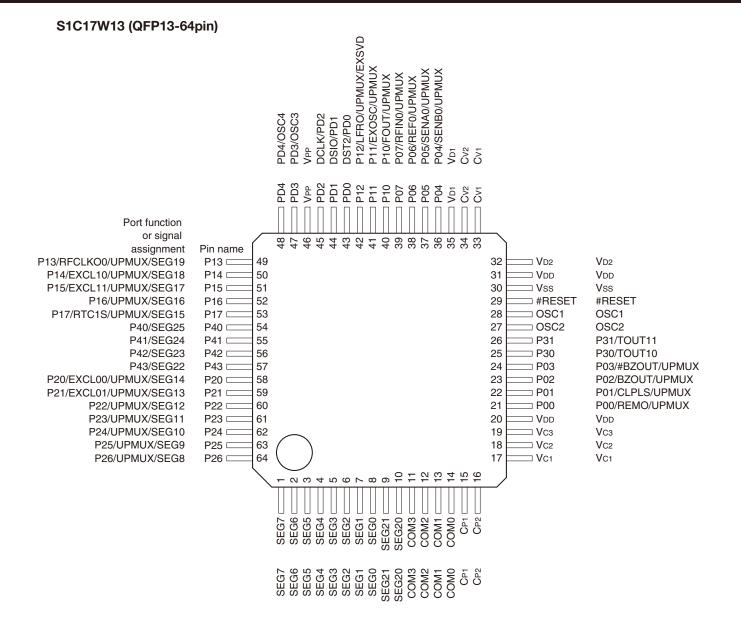
^{*1} These pins do not exist in the TQFP12-48pin package. *2 These pins do not exist in the SQFN7-48pin package.

PIN CONFIGURATION DIAGRAMS

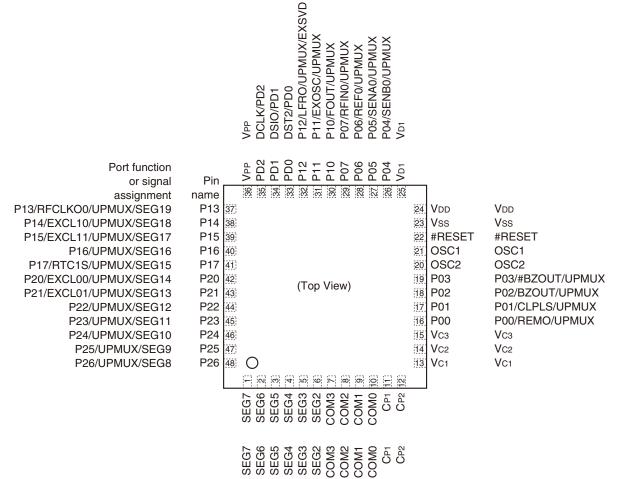
S1C17W12 (SQFN7-48pin)



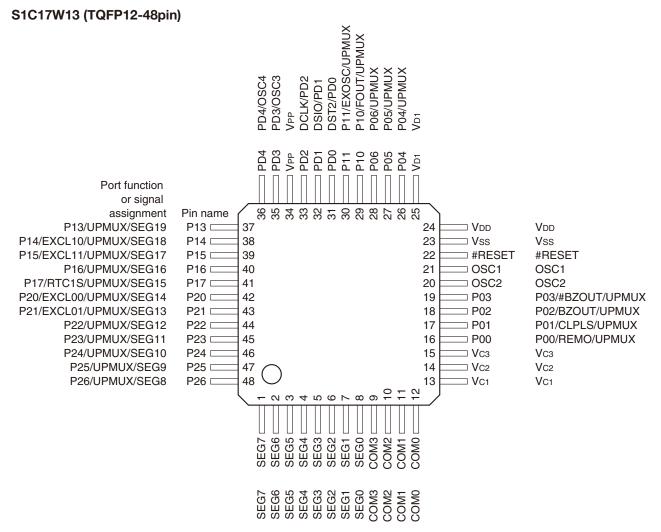
Note: The model in this package cannot be placed into super economy mode, as it does not have the VD2, CV1, and CV2 pins.



S1C17W13 (SQFN7-48pin)

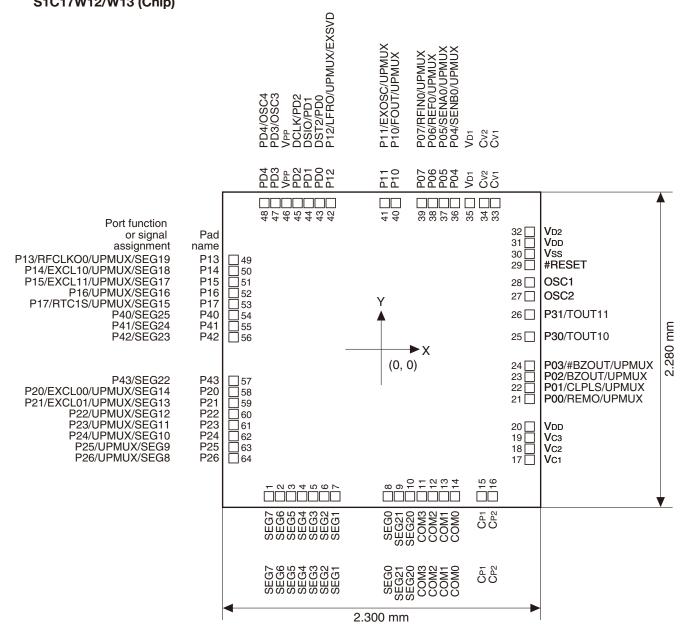


Note: The model in this package cannot be placed into super economy mode, as it does not have the VD2, Cv1, and Cv2 pins.



Note: The model in this package cannot be placed into super economy mode, as it does not have the VD2, Cv1, and Cv2 pins.

S1C17W12/W13 (Chip)



PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

	official field	a oontinato to acongit attornot
I/O:	I	= Input
	0	= Output
	I/O	= Input/output
	Р	= Power supply
	А	= Analog signal
	Hi-Z	= High impedance state
Initial state:	l (Pull-up)	= Input with pulled up
	l (Pull-down)) = Input with pulled down
	Hi-Z	= High impedance state
	O (H)	= High level output
	0 (L)	= Low level output
Tolerant fail-safe	structure:	
	1	= Over voltage tolerant fail

= Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter) The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}.

						W	12	, I	W13	\$
Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Chip	SQFN7-48pin	64pin/Chip	SQFN7-48pin	TQFP12-48pin
Vdd	Vdd	Р	-	-	Power supply (+)	1	1	1	1	\checkmark
Vss	Vss	Р	-	-	GND	1	\checkmark	\checkmark	\checkmark	\checkmark
Vpp	Vpp	Р	-	-	Power supply for Flash programming	1	1	1	<	\checkmark
VD1	VD1	Α	-	-	DC-DC converter output	1	1	1	1	1
VD2	VD2	Α	-	-	DC-DC converter stabilization capacitor connect pin	1	-	1	_	-
Cv1-2	Cv1-2	Α	-	-	DC-DC converter charge pump capacitor connect pins	1	-	1	_	-
Vc1-3	VC1-3	Р	-	-	LCD panel driver power supply	1	1	1	1	1
CP1-2	Ср1-2	Α	-	-	LCD power supply booster capacitor connect pins	1	1	1	1	-
OSC1	OSC1	Α	-	-	OSC1 oscillator circuit input	1	-	1	1	1
OSC2	OSC2	A	-	-	OSC1 oscillator circuit output		-	1	1	1
#RESET	#RESET	1	I (Pull-up)	-	Reset input	1	1	1	1	1
P00	P00	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	REMO	0			IR remote controller transmit data output	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	1	1	1
P01	P01	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	CLPLS	0	1		IR remote controller clear pulse output		1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	1	1	1
P02	P02	I/O	Hi-Z	1	/ I/O port		1	1	1	1
	BZOUT	0			Sound generator output	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
P03	P03	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	#BZOUT	0			Sound generator inverted output	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
P04	P04	I/O	Hi-Z	-	I/O port	1	1	1	1	1
	SENB0	Α			R/F converter Ch.0 sensor B oscillator pin	1	1	1	1	-
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
P05	P05	I/O	Hi-Z	-	I/O port		1	1	1	1
	SENA0	Α	1		I/O port R/F converter Ch.0 sensor A oscillator pin		1	1	1	-
	UPMUX	I/O]		User-selected I/O (universal port multiplexer)	1	1	1	1	1
P06	P06	I/O	Hi-Z	-	I/O port	1	1	1	1	1
	REF0	Α	1		R/F converter Ch.0 reference oscillator pin	1	1	1	1	-
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	1	1	1	1	1

						w	12	<u> </u>	W13	
Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Chip	SQFN7-48pin	64pin/Chip	SQFN7-48pin	TQFP12-48pin
P07	P07	I/O	Hi-Z	-	I/O port	1	1	1	1	-
	RFIN0	А			R/F converter Ch.0 oscillation input	1	1	1	1	-
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	-
P10	P10	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	FOUT	0			Clock external output	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
P11	P11	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	EXOSC	I			Clock generator external clock input	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
P12	P12	I/O	Hi-Z	1	I/O port	1	1	1	1	-
	LFRO	0			LCD frame signal monitor output	1	1	1	1	-
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	-
	EXSVD	Α			External power supply voltage detection input	1	1	1	1	-
P13	P13	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	RFCLKO0	0			R/F converter Ch.0 clock monitor output	1	1	1	1	_
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG19	Α			LCD segment output	1	1	1	1	1
P14	P14	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	EXCL10	Ι			16-bit PWM timer Ch.1 event counter input 0	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	\checkmark	1
	SEG18	А			LCD segment output	1	1	1	\checkmark	1
P15	P15	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG17	Α			LCD segment output	1	1	1	1	1
P16	P16	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG16	А			LCD segment output	1	1	1	1	1
P17	P17	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	RTC1S	0			Real-time clock 1-second cycle pulse output	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG15	Α			LCD segment output	1	1	1	1	1
P20	P20	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	EXCL00	Ι			16-bit PWM timer Ch.0 event counter input 0	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG14	Α			LCD segment output	1	1	1	1	1
P21	P21	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	EXCL01	Ι			16-bit PWM timer Ch.0 event counter input 1	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG13	Α			LCD segment output	1	1	1	1	1
P22	P22	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG12	А			LCD segment output	1	1	1	1	1
P23	P23	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG11	Α			LCD segment output	1	1	1	1	1
P24	P24	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG10	А			LCD segment output	1	1	1	1	1
P25	P25	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG9	Α			LCD segment output	1	1	1	1	1
P26	P26	I/O	Hi-Z	1	I/O port	1	1	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	1	1
	SEG8	Α			LCD segment output	1	1	1	1	1
P30	P30	0	Hi-Z	-	LED drive port		1	1	-	-
	TOUT10	0			16-bit PWM timer Ch.1 PWM output 0		1	1	_	-

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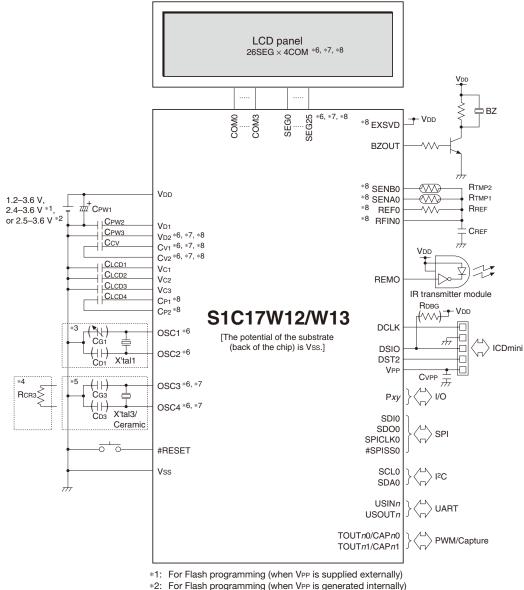
						W	12	1	W13	;
Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	Chip	SQFN7-48pin	64pin/Chip	SQFN7-48pin	TQFP12-48pin
P31	P31	0	Hi-Z	-	LED drive port	1	1	1	-	_
	TOUT11	0			16-bit PWM timer Ch.1 PWM output 1	1	1	1	-	_
P40	P40	I/O	Hi-Z	1	I/O port	1	-	1	-	-
	SEG25	A			LCD segment output	1	-	1	-	-
P41	P41	I/O	Hi-Z	1	I/O port	1	-	1	-	_
	SEG24	A			LCD segment output	1	-	1	-	-
P42	P42	I/O	Hi-Z	1	I/O port	1	-	\checkmark	-	-
	SEG23	Α			LCD segment output	1	-	1	-	_
P43	P43	I/O	Hi-Z	1	I/O port	1	-	1	-	-
	SEG22	Α			LCD segment output		-	1	-	_
PD0	DST2	0	O (L)	1	On-chip debugger status output	1	1	<	1	1
	PD0	I/O			I/O port	1	1	<	1	1
PD1	DSIO	I/O	I (Pull-up)	1	On-chip debugger data input/output	1	1	<	1	1
	PD1	I/O			I/O port	1	1	1	1	1
PD2	DCLK	0	O (H)	-	On-chip debugger clock output	1	1	1	1	1
	PD2	0			Output port	1	1	1	1	1
PD3	PD3	I/O	Hi-Z	-	I/O port	1	-	1	-	1
	OSC3	Α	1		OSC3 oscillator circuit input	1	-	1	-	1
PD4	PD4	I/O	Hi-Z	-	I/O port	1	-	1	-	1
	OSC4	Α			OSC3 oscillator circuit output	1	-	1	-	1
COM0-3	COM0-3	Α	Hi-Z	-	LCD common output	1	1	1	\checkmark	1
SEG0-1	SEG0-1	Α	Hi-Z	-	LCD segment output	1	-	\checkmark	-	1
SEG2-7	SEG2-7	Α	Hi-Z	-	LCD segment output	1	1	\checkmark	1	1
SEG20-21	SEG20-21	Α	Hi-Z	-	LCD segment output	1	-	1	_	_

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
Synchronous serial interface (SPIA)	SDIn		<i>n</i> = 0	SPIA Ch.n data input
	SDOn	0		SPIA Ch.n data output
	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
I ² C (I2C)	SCLn	I/O	<i>n</i> = 0	I2C Ch.n clock input/output
	SDAn	I/O		I2C Ch.n data input/output
UART (UART2)	USINn	I	<i>n</i> = 0, 1	UART2 Ch.n data input
	USOUTn	0		UART2 Ch.n data output
16-bit PWM timer (T16B)	TOUTn0/CAPn0	I/O	<i>n</i> = 0, 1	T16B Ch.n PWM output/capture input 0
	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1

BASIC EXTERNAL CONNECTION DIAGRAM



*3: When the OSC1 crystal oscillator is used (except for the S1C17M20/M23 (24-pin package))

*4: When the OSC3 crystal/ceramic oscillator is used (except for the S1C17M20/M23 (24-pin package))

*5: When the R/F converter is used (available in the S1C17M22/M25)

(): Do not mount components if unnecessary.

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