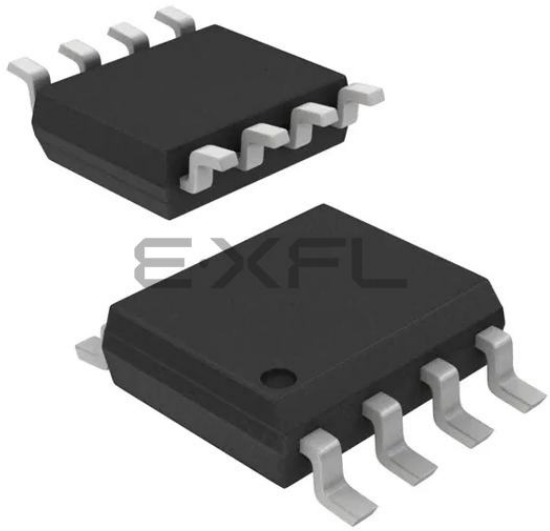

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Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	WDT
Number of I/O	6
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny11l-2su

Sleep Modes

Sleep Modes for the ATtiny11

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. The SM bit in the MCUCR register selects which sleep mode (Idle or Power-down) will be activated by the SLEEP instruction. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine, and resumes execution from the instruction following SLEEP. On wake-up from Power Down Mode on pin change, two instruction cycles are executed before the pin change interrupt flag is updated. During these cycles, the prosessor executes intructions, but the interrupt condition is not readable, and the interrupt routine has not startet yet. The contents of the register file and I/O memory are unaltered. If a reset occurs during Sleep Mode, the MCU wakes up and executes from the Reset vector.

Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle Mode, stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and Watchdog Reset. If wake-up from the Analog Comparator interrupt is not required, the analog comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status register – ACSR. This will reduce power consumption in Idle Mode. When the MCU wakes up from Idle mode, the CPU starts program execution immediately.

Power-down Mode

When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power-down Mode. In this mode, the external oscillator is stopped, while the external interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a watchdog reset (if enabled), an external level interrupt (INT0), or an pin change interrupt can wake up the MCU.

Note that if a level-triggered or pin change interrupt is used for wake-up from power-down, the changed level must be held for a time longer than the reset delay period of t_{TOUT}. Otherwise, the MCU will fail to wake up.

Sleep Modes for the ATtiny12

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. The SM bit in the MCUCR register selects which sleep mode (Idle or Power-down) will be activated by the SLEEP instruction. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes. The CPU is then halted for four cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the register file and I/O memory are unaltered. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset vector.

Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle Mode stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and Watchdog Reset. If wake-up from the Analog Comparator interrupt is not required, the analog comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register – ACSR. This will reduce power consumption in Idle Mode.

Power-down Mode

When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power-down Mode. In this mode, the external oscillator is stopped, while the external interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a watchdog

System Control and Reset

Reset Sources

The ATtiny11/12 provides three or four sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the power-on reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.
- Brown-out Reset. The MCU is reset when the supply voltage V_{CC} falls below a certain voltage (ATtiny12 only).

During reset, all I/O registers are then set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP – relative jump – instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 15 shows the reset logic for the ATtiny11. Figure 16 shows the reset logic for the ATtiny12. Table 7 defines the electrical parameters of the reset circuitry for ATtiny11. Table 9 shows the parameters of the reset circuitry for ATtiny12.

Figure 15. Reset Logic for the ATtiny11

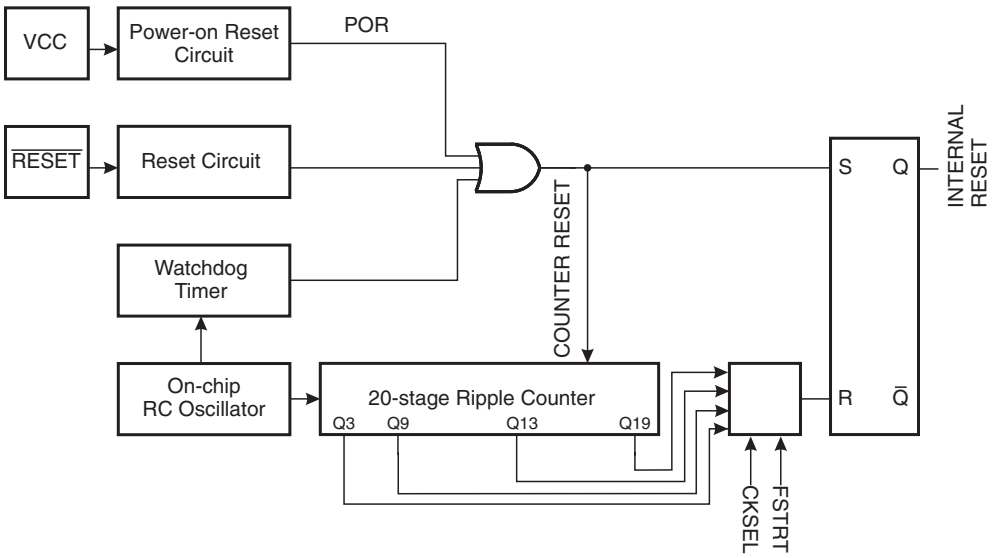


Table 7. Reset Characteristics for the ATtiny11

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}[1]	Power-on Reset Threshold Voltage (rising)	1.0	1.4	1.8	V
	Power-on Reset Threshold Voltage (falling)	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Pin Change Interrupt

The pin change interrupt is triggered by any change on any input or I/O pin. Change on pins PB2..0 will always cause an interrupt. Change on pins PB5..3 will cause an interrupt if the pin is configured as input or I/O, as described in the section “Pin Descriptions” on page 5. Observe that, if enabled, the interrupt will trigger even if the changing pin is configured as an output. This feature provides a way of generating a software interrupt. Also observe that the pin change interrupt will trigger even if the pin activity triggers another interrupt, for example, the external interrupt. This implies that one external event might cause several interrupts.

The values on the pins are sampled before detecting edges. If pin change interrupt is enabled, pulses that last longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt.

Register Description

MCU Control Register – MCUCR

The MCU Control Register contains control bits for general MCU functions.

Bit	7	6	5	4	3	2	1	0	
$35	-	(PUD)	SE	SM	-	-	ISC01	ISC00	MCUCR
Read/Write	R	R(/W)	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Note: The Pull-up Disable (PUD) bit is only available in ATtiny12.

- **Bit 7 - Res: Reserved Bit**

This bit is a reserved bit in the ATtiny11/12 and always reads as zero.

- **Bit 6 - Res: Reserved Bit in ATtiny11**

This bit is a reserved bit in the ATtiny11 and always reads as zero.

- **Bit 6 - PUD: Pull-up Disable in ATtiny12**

Setting this bit, disables all pull-ups on port B. If this bit is cleared, the pull-ups can be individually enabled as described in section “I/O Port B” on page 36.

- **Bit 5 - SE: Sleep Enable**

The SE bit must be set (one) to make the MCU enter the Sleep Mode when the SLEEP instruction is executed. To avoid the MCU entering the Sleep Mode unless it is the programmer’s purpose, it is recommended to set the Sleep Enable SE bit just before the execution of the SLEEP instruction.

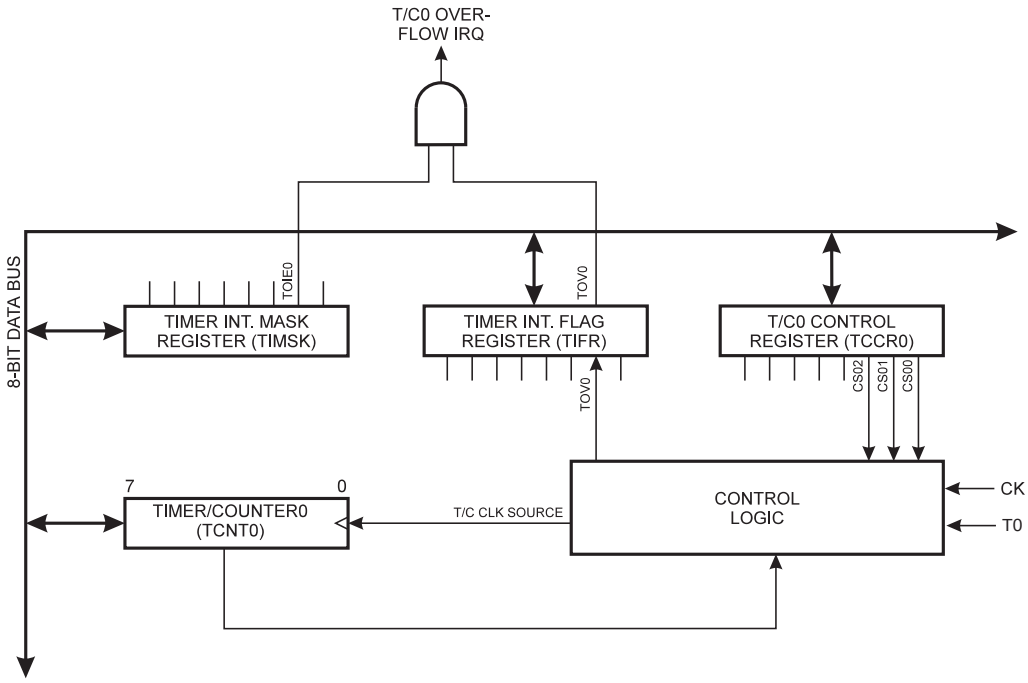
- **Bit 4 - SM: Sleep Mode**

This bit selects between the two available sleep modes. When SM is cleared (zero), Idle Mode is selected as Sleep Mode. When SM is set (one), Power-down Mode is selected as Sleep Mode. For details, refer to the paragraph “Sleep Modes” below.

- **Bits 3, 2 - Res: Reserved Bits**

These bits are reserved bits in the ATtiny11/12 and always read as zero.

Figure 23. Timer/Counter0 Block Diagram

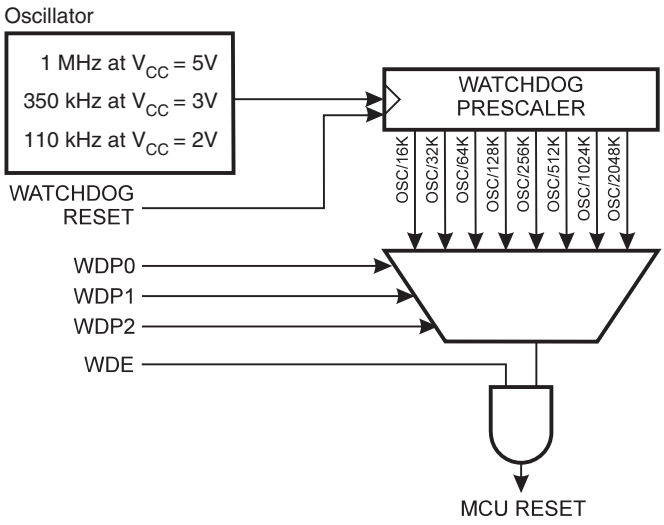


Watchdog Timer

The Watchdog Timer is clocked from a separate on-chip oscillator. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted as shown in Table 19. See characterization data for typical values at other V_{CC} levels. The WDR – Watchdog Reset – instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the ATtiny11/12 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 28.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 24. Watchdog Timer



Register Description

Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0	
$21	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..5 - Res: Reserved Bits**

These bits are reserved bits in the ATtiny11/12 and will always read as zero.

- **Bit 4 - WDTOE: Watchdog Turn-off Enable**

This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a watchdog disable procedure.

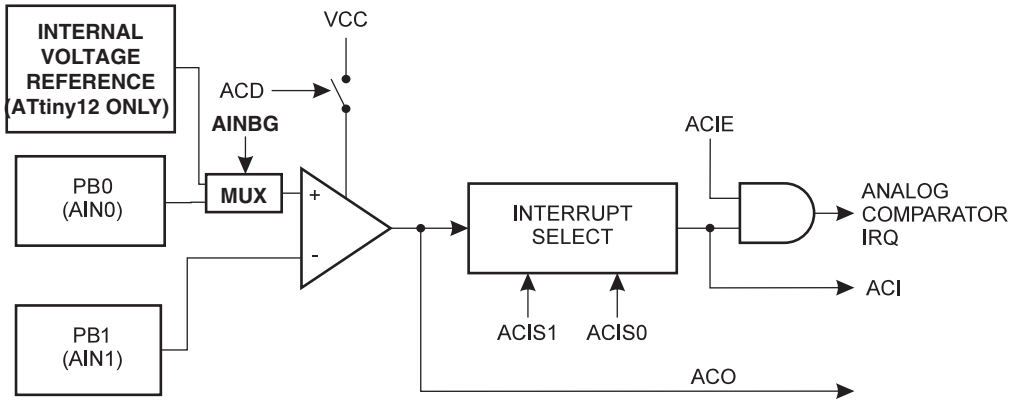
- **Bit 3 - WDE: Watchdog Enable**

When the WDE is set (one) the Watchdog Timer is enabled, and if the WDE is cleared (zero) the Watchdog Timer function is disabled. WDE can be cleared only when the WDTOE bit is set(one). To disable an enabled watchdog timer, the following procedure must be followed:

Analog Comparator

The Analog Comparator compares the input values on the positive input PB0 (AIN0) and negative input PB1 (AIN1). When the voltage on the positive input PB0 (AIN0) is higher than the voltage on the negative input PB1 (AIN1), the Analog Comparator Output (ACO) is set (one). The comparator's output can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 25.

Figure 25. Analog Comparator Block Diagram.



Register Description

Analog Comparator Control and Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
$08	ACD	(AINBG)	ACO	ACI	ACIE	-	ACIS1	ACIS0	ACSR
Read/Write	R/W	R(/W)	R	R/W	R/W	R	R/W	R/W	
Initial Value	0	0	X	0	0	0	0	0	

Note: AINBG is only available in ATtiny12.

- **Bit 7 - ACD: Analog Comparator Disable**

When this bit is set (one), the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- **Bit 6 - AINBG: Analog Comparator Bandgap Select in ATtiny12**

In ATtiny12, when this bit is set, a fixed bandgap voltage of 1.22 ± 0.05V replaces the normal input to the positive input (AIN0) of the comparator. When this bit is cleared, the normal input pin PB0 is applied to the positive input of the comparator.

- **Bit 6- Res: Reserved Bit in ATtiny11**

This bit is a reserved bit in the ATtiny11 and will always read as zero.

- **Bit 5 - ACO: Analog Comparator Output**

ACO is directly connected to the comparator output.

High-voltage Serial Programming Algorithm

To program and verify the ATtiny11/12 in the High-voltage Serial Programming mode, the following sequence is recommended (See instruction formats in Table 23):

1. Power-up sequence: Apply 4.5 - 5.5V between V_{CC} and GND. Set PB5 and PB0 to “0” and wait at least 100 ns. Toggle PB3 at least four times with minimum 100 ns pulse-width. Set PB3 to “0”. Wait at least 100 ns. Apply 12V to PB5 and wait at least 100 ns before changing PB0. Wait 8 µs before giving any instructions.
2. The Flash array is programmed one byte at a time by supplying first the address, then the low and high data byte. The write instruction is self-timed, wait until the PB2 (RDY/$\overline{\text{BSY}}$) pin goes high.
3. The EEPROM array (ATtiny12 only) is programmed one byte at a time by supplying first the address, then the data byte. The write instruction is self-timed, wait until the PB2 (RDY/$\overline{\text{BSY}}$) pin goes high.
4. Any memory location can be verified by using the Read instruction which returns the contents at the selected address at serial output PB2.
5. Power-off sequence:Set PB3 to “0”.
   Set PB5 to “1”.
   Turn V_{CC} power off.

When writing or reading serial data to the ATtiny11/12, data is clocked on the rising edge of the serial clock, see Figure 27, Figure 28 and Table 24 for details.

Table 23. High-voltage Serial Programming Instruction Set for ATtiny11/12 (Continued)

Instruction		Instruction Format				Operation Remarks
		Instr.1	Instr.2	Instr.3	Instr.4	
Read EEPROM byte (ATtiny12)	PB0 PB1 PB2	0_0000_0000_00 0_0110_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 **o_oooo_ooo**x_xx			Repeat Instr.2 for each new address
Write Fuse bits (ATtiny11)	PB0 PB1 PB2	0_0100_0000_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_000**7_6543**_00 0_0010_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_0100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 x_xxxx_xxxx_xx	Wait t_{WLWH_PFB} after Instr.3 for the Write fuse bits cycle to finish. Write **7** - **3** = “0” to program the fuse bit.
Write Fuse bits (ATtiny12)	PB0 PB1 PB2	0_0100_0000_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_**CBA9_8543**_00 0_0010_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_0100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 x_xxxx_xxxx_xx	Wait after Instr.4 until PB2 goes high. Write **C** - **A**, **9, 8,** 5 - **3** = “0” to program the fuse bit.
Write Lock bits	PB0 PB1 PB2	0_0010_0000_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_0210_00 0_0010_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_0100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 0_0000_0000_00	Wait after Instr.4 until PB2 goes high. Write ***2***, ***1*** = “0” to program the lock bit.
Read Fuse bits (ATtiny11)	PB0 PB1 PB2	0_0000_0100_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 x_xx**76_543**x_xx		Reading **7** - **3** = “0” means the fuse bit is programmed.
Read Fuse bits (ATtiny12)	PB0 PB1 PB2	0_0000_0100_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 **C_BA98_543**x_xx		Reading **C** - **A**, **9**, **8**, **5** - **3** = “0” means the fuse bit is programmed.
Read Lock bits	PB0 PB1 PB2	0_0000_0100_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0111_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0111_1100_00 x_xxxx_***21***xx_xx		Reading ***2***, ***1*** = “0” means the lock bit is programmed.
Read Signature Bytes	PB0 PB1 PB2	0_0000_1000_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_00**bb**_00 0_0000_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0110_1100_00 **o_oooo_ooo**x_xx	Repeat Instr.2 - Instr.4 for each signature byte address
Read Calibration Byte (ATtiny12)	PB0 PB1 PB2	0_0000_1000_00 0_0100_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0000_1100_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0111_1000_00 x_xxxx_xxxx_xx	0_0000_0000_00 0_0111_1100_00 **o_oooo_ooo**x_xx	

Note: **a** = address high bits
b = address low bits
i = data in
o = data out
x = don’t care
1 = Lock Bit1
2 = Lock Bit2
3 = CKSEL0 Fuse
4 = CKSEL1 Fuse
5 = CKSEL2 Fuse
9, **6** = RSTDISBL Fuse
7 = FSTRT Fuse
8 = CKSEL3 Fuse
A = SPIEN Fuse
B = BODEN Fuse
C = BODLEVEL Fuse

Low-voltage Serial Programming Characteristics

Figure 31. Low-voltage Serial Programming Timing

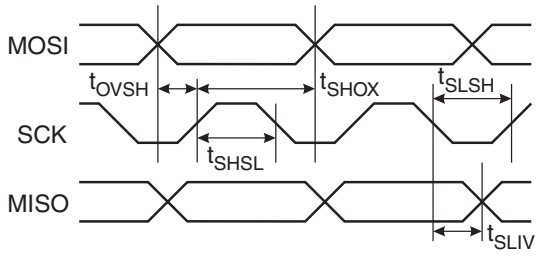


Table 26. Low-voltage Serial Programming Characteristics T_A = -40°C to 85°C, V_{CC} = 2.2 - 5.5V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.2 - 2.7V)	0		1	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.2 - 2.7V)	1000			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.7 - 4.0V)	0		4	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.7 - 4.0V)	250			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 4.0 - 5.5V)	0		8	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.0 - 5.5V)	125			ns
t_{SHSL}	SCK Pulse Width High	2 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns

Table 27. Minimum Wait Delay after the Chip Erase Instruction

Symbol	Minimum Wait Delay
t_{WD_ERASE}	6.8 ms

Table 28. Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	Minimum Wait Delay
t_{WD_FLASH}	3.4 ms
t_{WD_EEPROM}	6.8 ms

DC Characteristics – Preliminary Data (Continued)

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V for ATtiny11, V_{CC} = 1.8V to 5.5V for ATtiny12 (Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Active 1 MHz, V_{CC} = 3V (ATtiny12V)			1.0	mA
		Active 2 MHz, V_{CC} = 3V (ATtiny11L)			2.0	mA
		Active 4 MHz, V_{CC} = 3V (ATtiny12L)			2.5	mA
		Active 6 MHz, V_{CC} = 5V (ATtiny11)			10	mA
		Active 8 MHz, V_{CC} = 5V (ATtiny12)			10	mA
		Idle 1 MHz, V_{CC} = 3V (ATtiny12V)			0.4	mA
		Idle 2 MHz, V_{CC} = 3V (ATtiny11L)			0.5	mA
		Idle 4 MHz, V_{CC} = 3V (ATtiny12L)			1.0	mA
		Idle 6 MHz, V_{CC} = 5V (ATtiny11)			2.0	mA
		Idle 8 MHz, V_{CC} = 5V (ATtiny12)			3.5	mA
		Power Down[5], V_{CC} = 3V, WDT enabled		9.0	15	µA
		Power Down[5], V_{CC} = 3V. WDT disabled (ATtiny12)		<1	2	µA
		Power Down[5], V_{CC} = 3V. WDT disabled (ATtiny11)		<1	5	µA
V_{ACIO}	Analog Comparator Input Offset Voltage	V_{CC} = 5V V_{IN} = V_{CC}/2			40	mV
I_{ACLK}	Analog Comparator Input Leakage Current	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
T_{ACPD}	Analog Comparator Propagation Delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low.
2. "Min" means the lowest value where the pin is guaranteed to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all I_{OL}, for all ports, should not exceed 100 mA.
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
4. Although each I/O port can source more than the test conditions (3 mA at V_{CC} = 5V, 1.5 mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all I_{OH}, for all ports, should not exceed 100 mA.
   If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. Minimum V_{CC} for Power-down is 1.5V. (On ATtiny12: only with BOD disabled)

Figure 34. Active Supply Current vs. V_{CC}

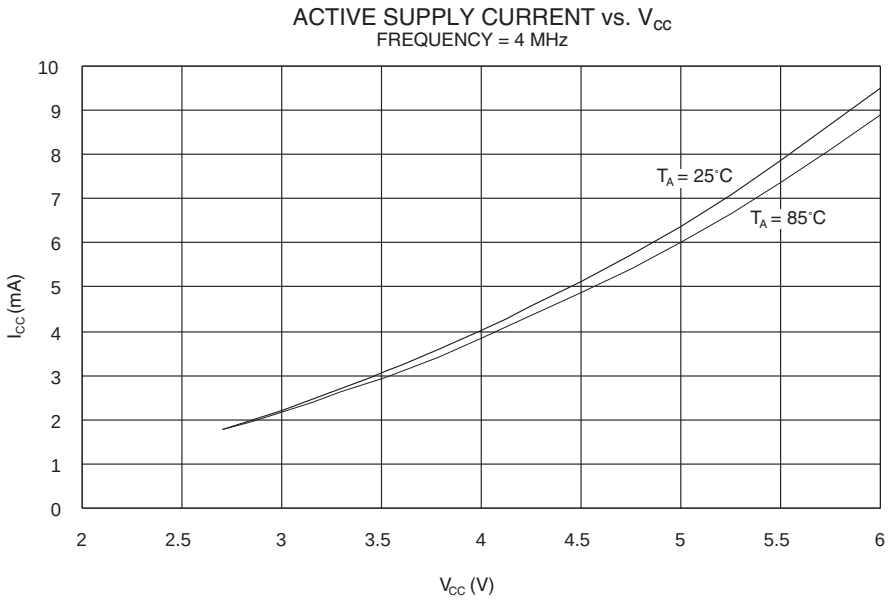


Figure 35. Active Supply Current vs. V_{CC}, Device Clocked by Internal Oscillator

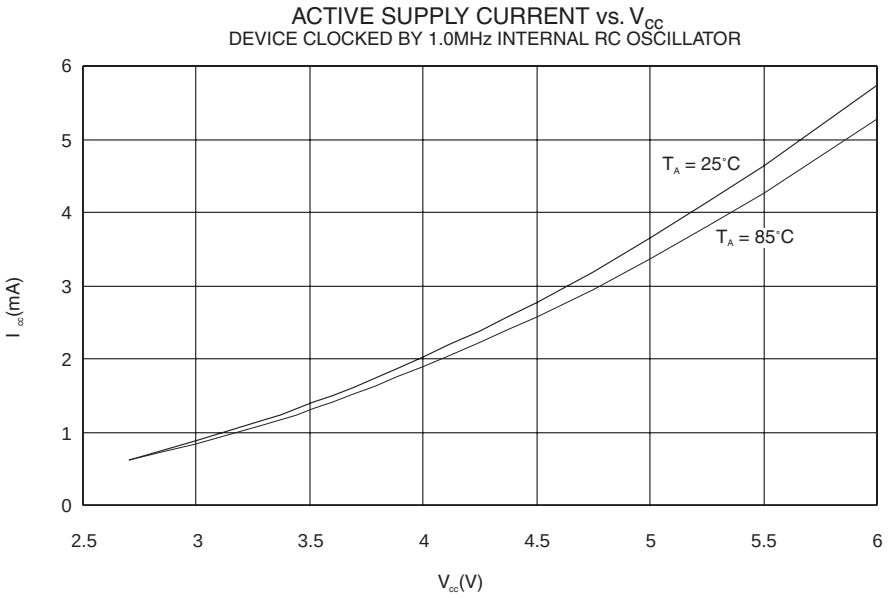


Figure 36. Active Supply Current vs. V_{CC}, Device Clocked by External 32kHz Crystal

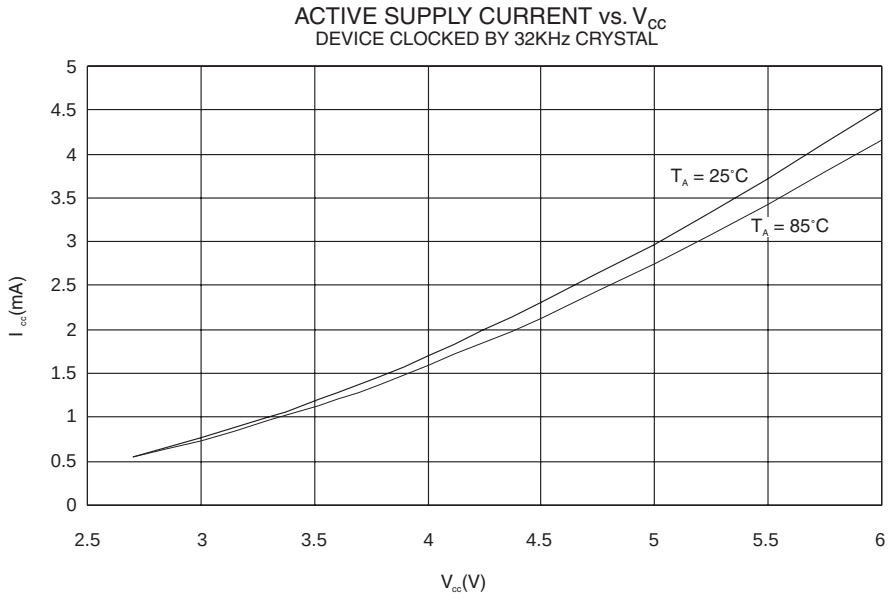


Figure 37. Idle Supply Current vs. Frequency

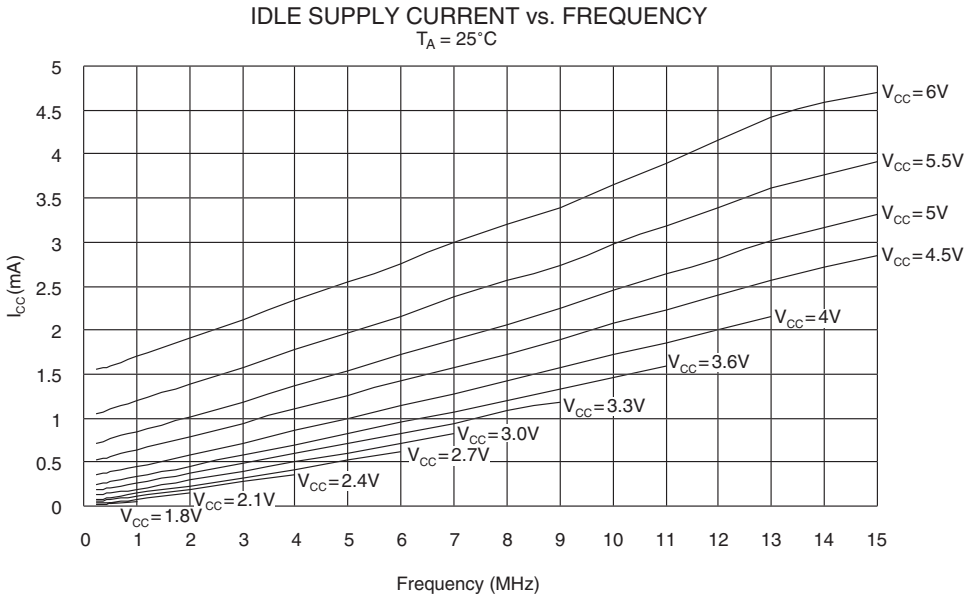


Figure 40. Idle Supply Current vs. V_{CC}, Device Clocked by External 32kHz Crystal

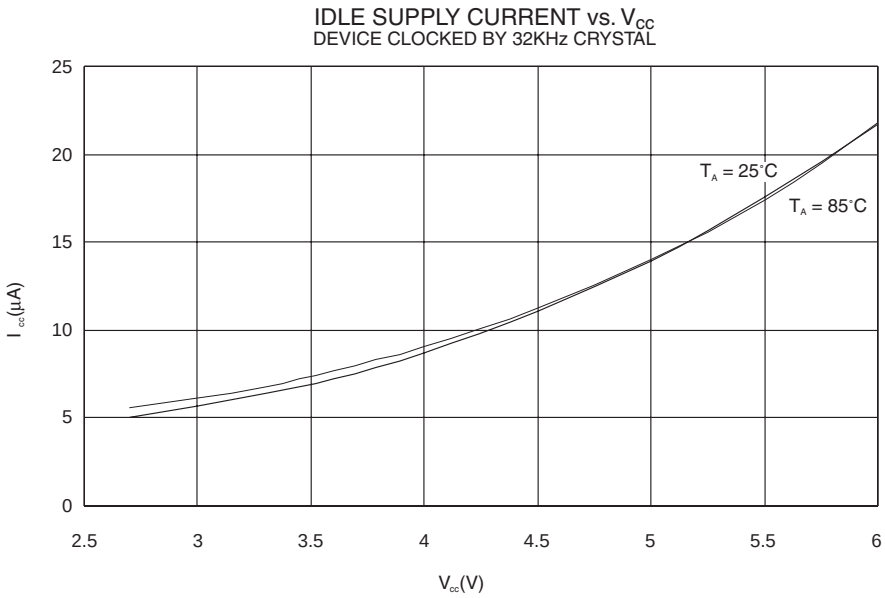
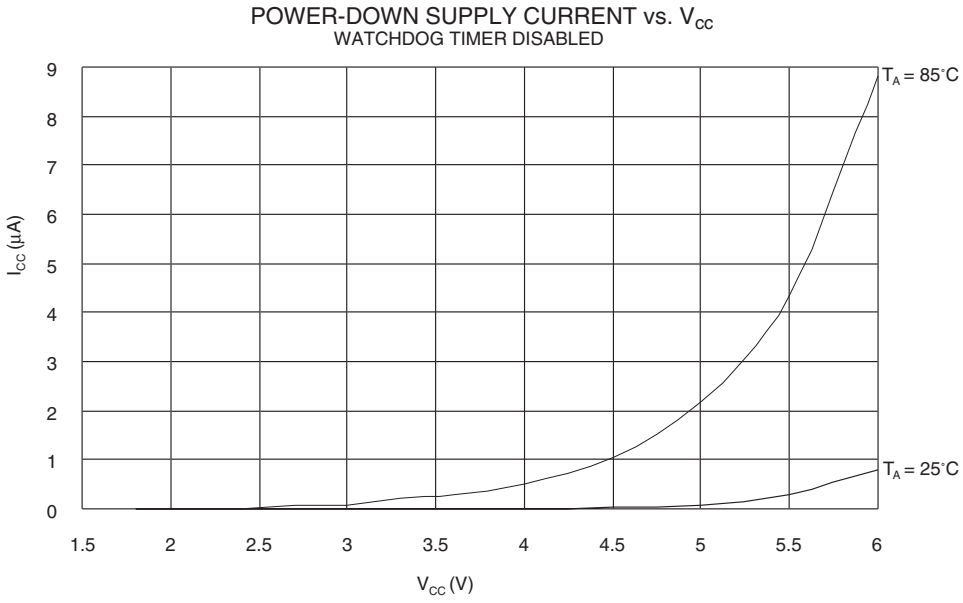


Figure 41. Power-down Supply Current vs. V_{CC}



Analog comparator offset voltage is measured as absolute offset.

Figure 44. Analog Comparator Offset Voltage vs. Common Mode Voltage

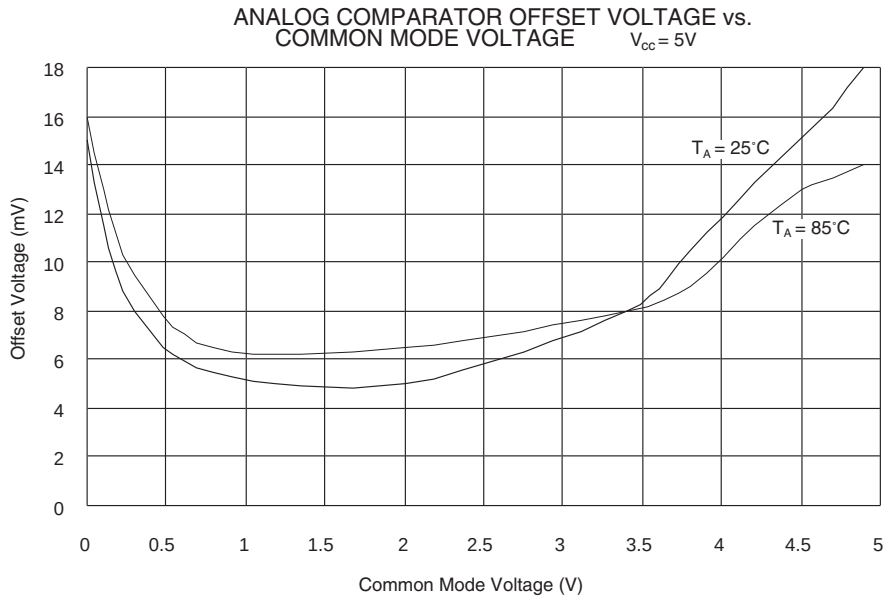


Figure 45. Analog Comparator Offset Voltage vs. Common Mode Voltage

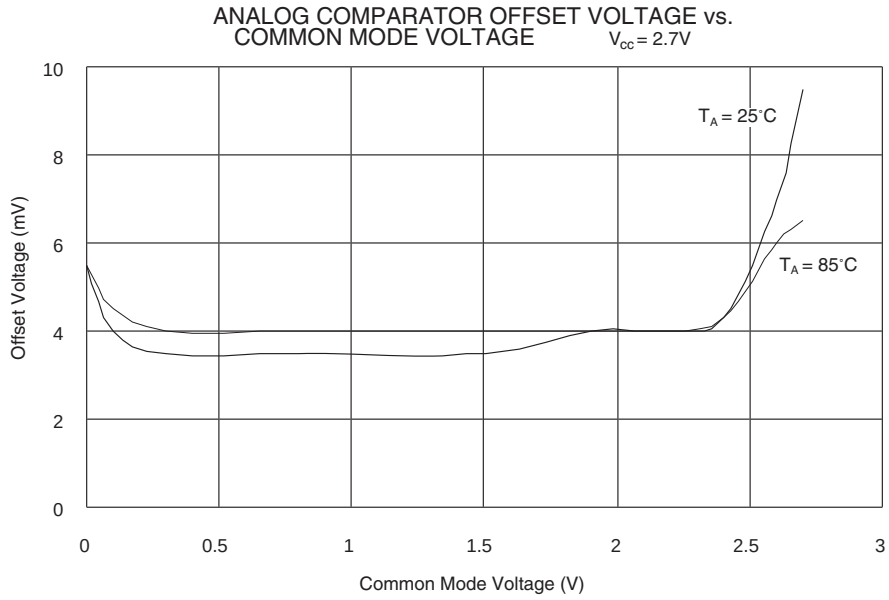


Figure 54. I/O Pin Input Threshold Voltage vs. V_{CC}

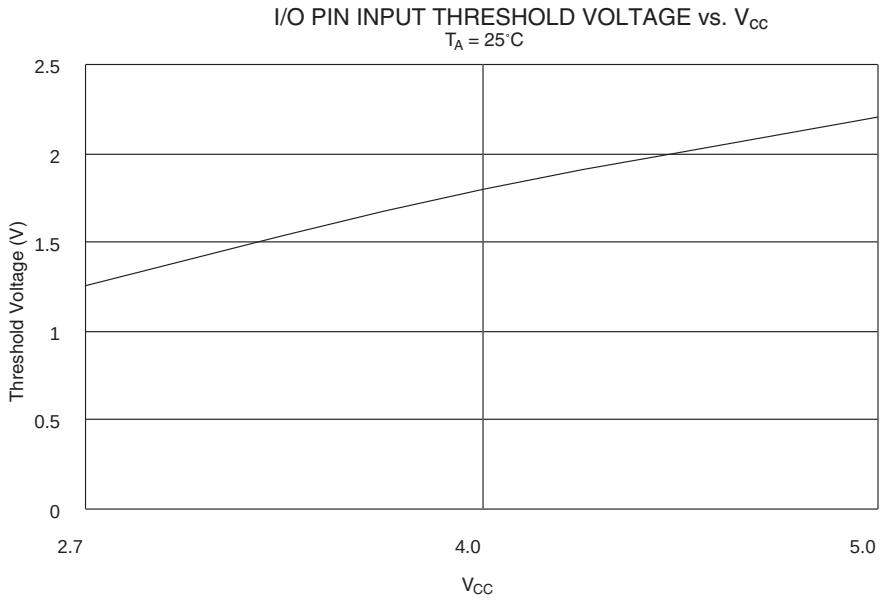


Figure 55. I/O Pin Input Hysteresis vs. V_{CC}

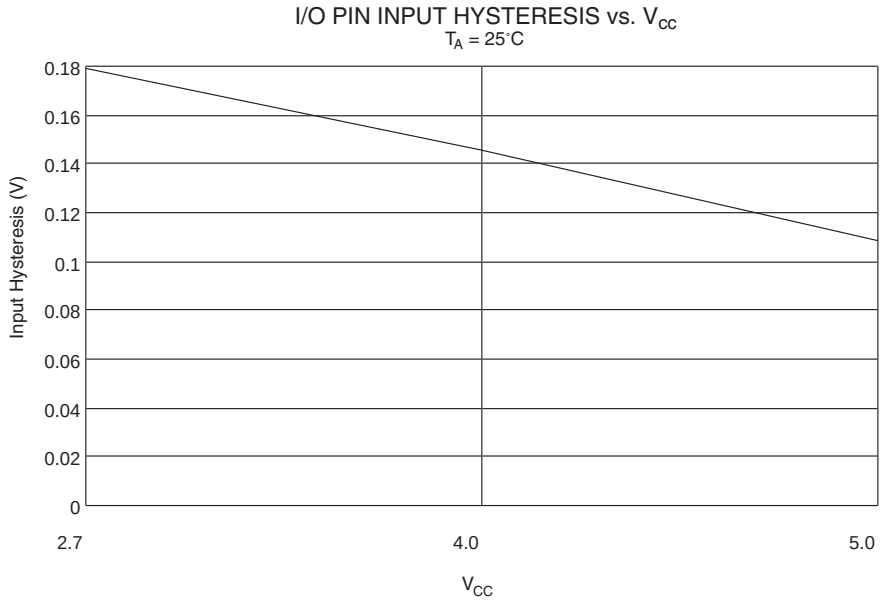


Figure 57. Active Supply Current vs. V_{CC}, Device Clocked by External 32kHz Crystal

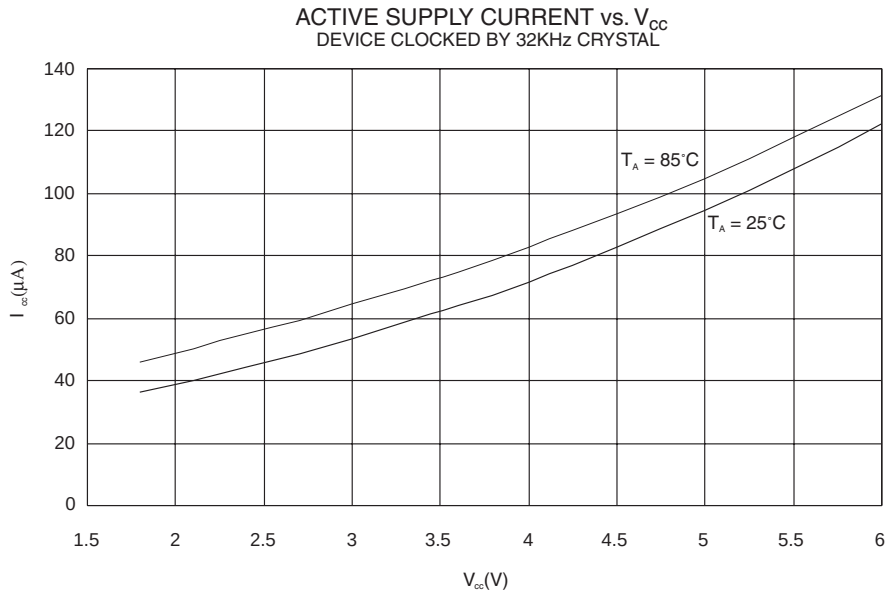


Figure 58. Idle Supply Current vs. V_{CC}, Device Clocked by Internal Oscillator

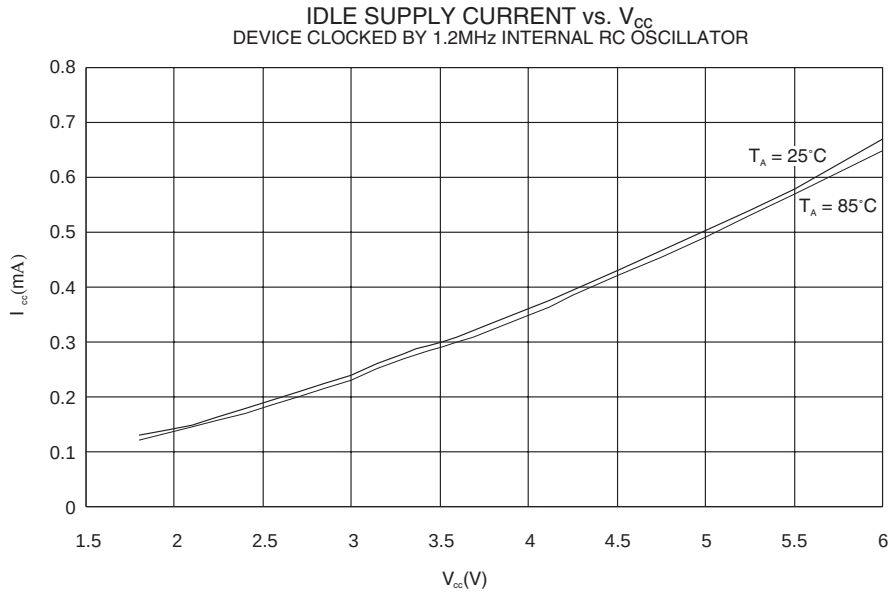


Figure 67. I/O Pin Sink Current vs. Output Voltage (V_{CC} = 5V)

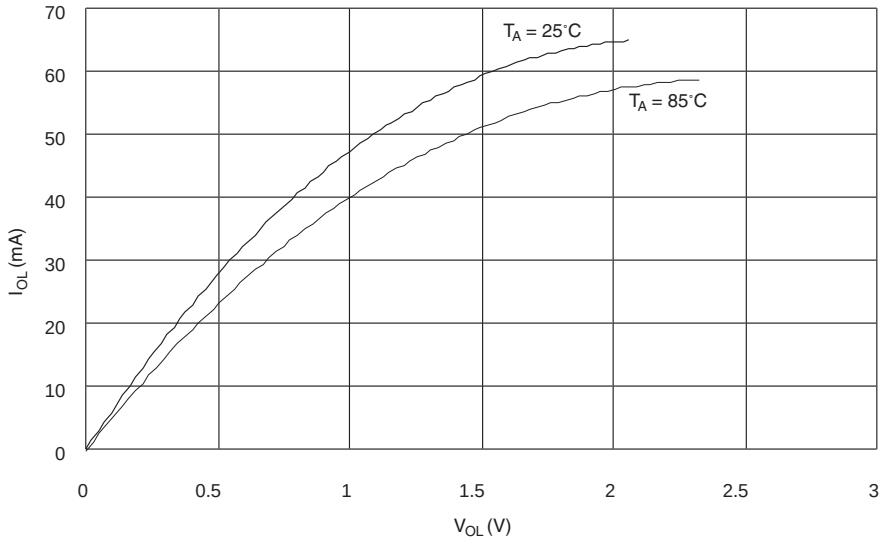
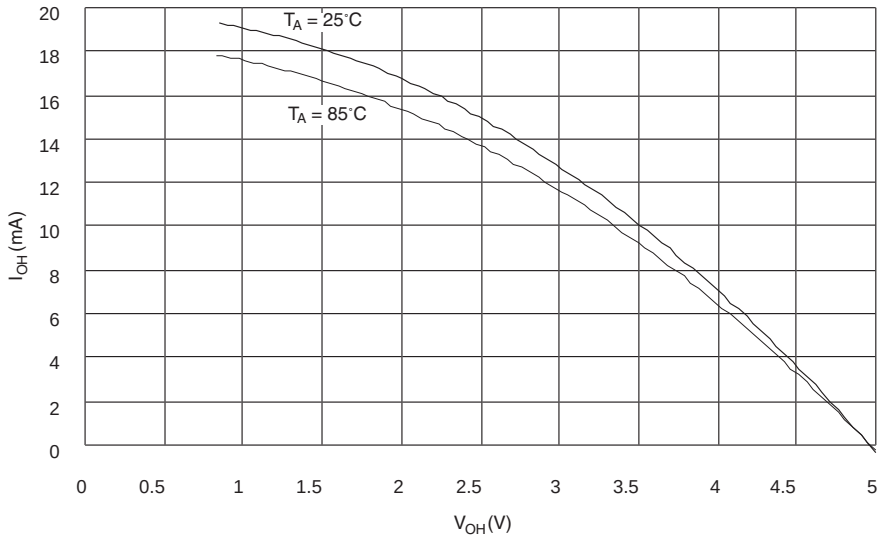
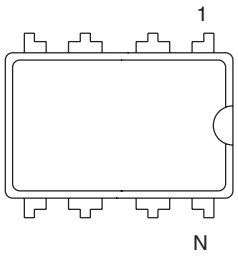


Figure 68. I/O Pin Source Current vs. Output Voltage (V_{CC} = 5V)

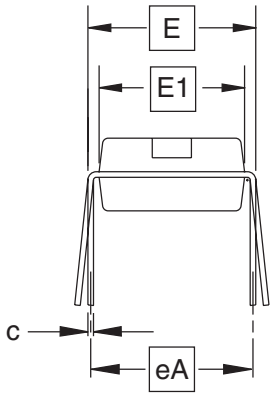


Packaging Information

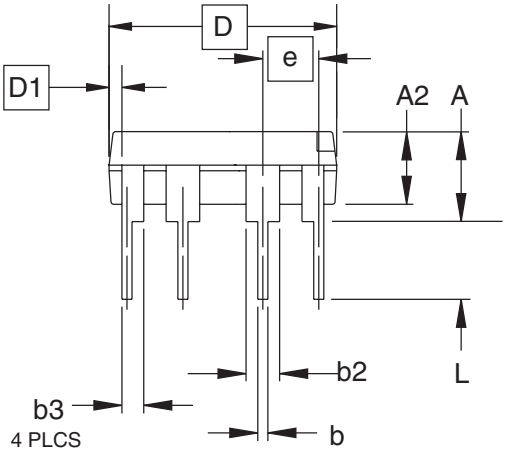
8P3



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

Datasheet Revision History

Please note that the page numbers listed in this section are refering to this document. The revision numbers are referring to the document revision.

Rev. 1006F-06/07

1. **“Not recommended for new design”.**

Rev. 1006E-07/06

1. **Updated chapter layout.**
2. **Updated Power-down in “Sleep Modes for the ATtiny11” on page 20.**
3. **Updated Power-down in “Sleep Modes for the ATtiny12” on page 20.**
4. **Updated Table 16 on page 36.**
5. **Updated “Calibration Byte in ATtiny12” on page 49.**
6. **Updated “Ordering Information” on page 87.**
7. **Updated “Packaging Information” on page 89.**

Rev. 1006D-07/03

1. **Updated V_{BOT} values in Table 9 on page 24.**

Rev. 1006C-09/01

1. **N/A**