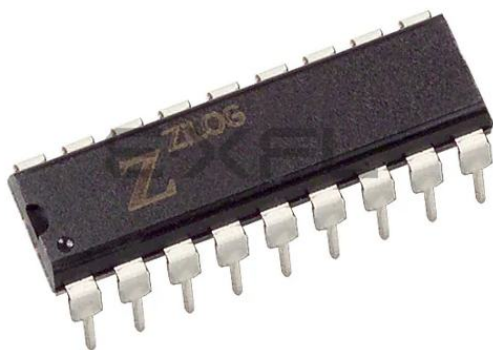




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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c0208pscr4380

GENERAL DESCRIPTION (Continued)

cations. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

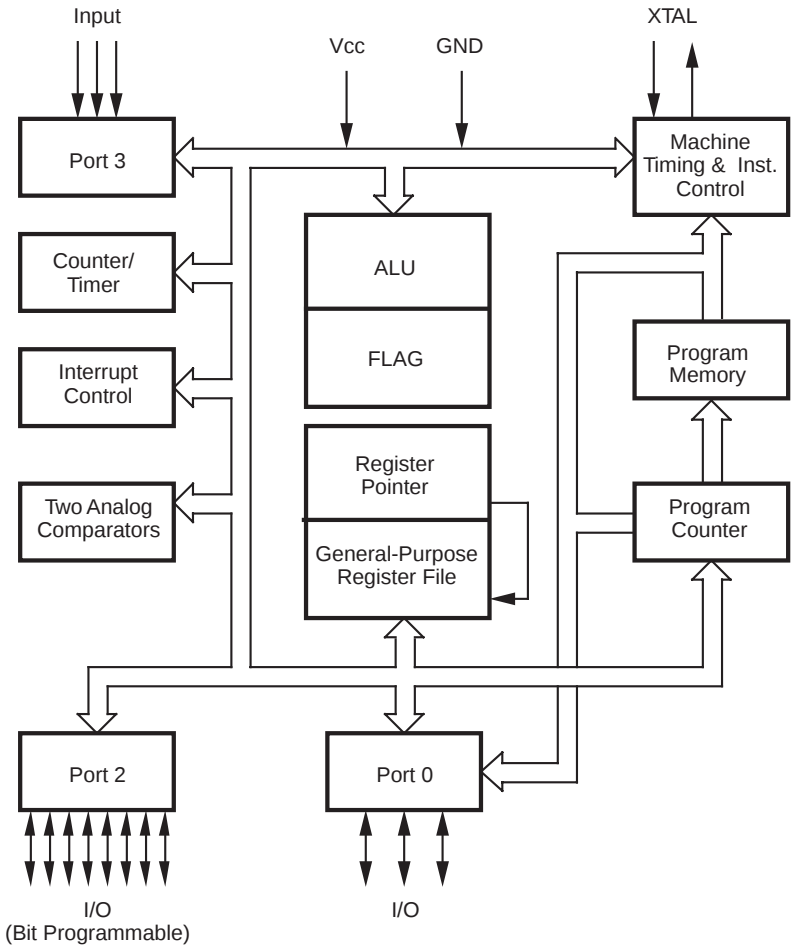


Figure 1. Z86C02/E02/L02 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

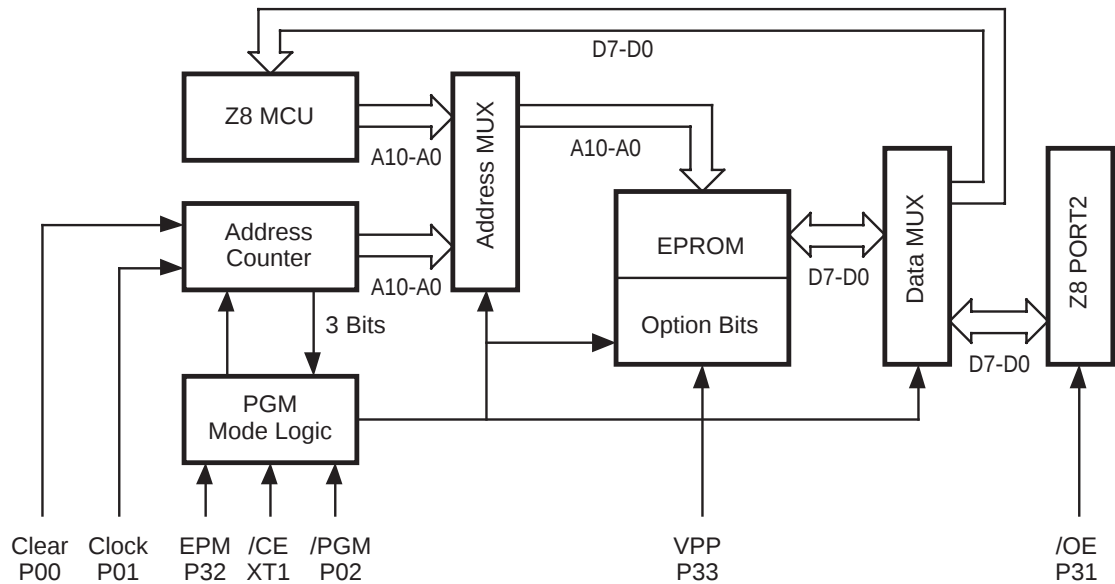


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTIONS

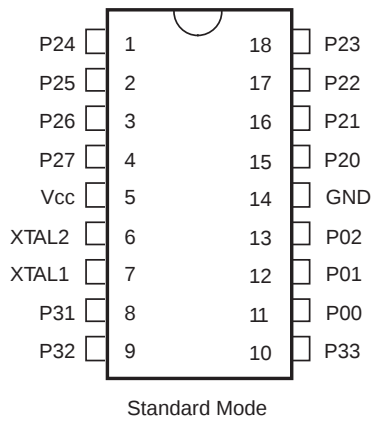


Figure 3. 18-Pin Standard Mode Configuration

Table 1. 18-Pin Standard Mode Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V _{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	-40	+105	C
Storage Temperature	-65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	-0.7	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2] (Z86C02/L02)	-0.7	$V_{DD}+1$	V
Voltage on Pin 7,8,9,10 with Respect to V_{SS} [Note 2] (Z86E02)	-0.7	$V_{DD}+1$	V
Total Power Dissipation		462	mW
Maximum Allowed Current out of V_{SS}		300	mA
Maximum Allowed Current into V_{DD}		270	mA
Maximum Allowed Current into an Input Pin [Note 3]	-600	+600	μ A
Maximum Allowed Current into an Open-Drain Pin [Note 4]	-600	+600	μ A
Maximum Allowed Output Current Sunk by Any I/O Pin		20	mA
Maximum Allowed Output Current Sourced by Any I/O Pin		20	mA
Maximum Allowed Output Current Sunk by Port 2, Port 0		80	mA
Maximum Allowed Output Current Sourced by Port 2, Port 0		80	mA

Notes:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

1. This applies to all pins except where otherwise noted.
2. Maximum current into pin must be $\pm 600\mu\text{A}$. There is no input protection diode from pin to V_{DD} .
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 6).

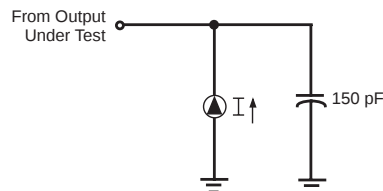


Figure 6. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0 \text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC CHARACTERISTICS

Z86C02

Sym. Parameter	V _{CC} [4]	T _A = 40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
		Min	Max				
I _{CC} Supply Current	3.0V		3.5	1.5	mA	@ 2 MHz	[5,6,7]
	5.5V		7.0	3.8	mA	@ 2 MHz	[5,6,7]
	3.0V		8.0	3.0	mA	@ 8 MHz	[5,6,7]
	5.5V		11.0	4.4	mA	@ 8 MHz	[5,6,7]
I _{CC1} Standby Current (Halt Mode)	3.0V		2.5	0.7	mA	@ 2 MHz	[5,6,7]
	5.5V		4.0	2.5	mA	@ 2 MHz	[5,6,7]
	3.0V		4.0	1.0	mA	@ 8 MHz	[5,6,7]
	5.5V		5.0	3.0	mA	@ 8 MHz	[5,6,7]
I _{CC} Supply Current (Low Noise Mode)	3.0V		3.5	1.5	mA	@ 1 MHz	[5,6,7]
	5.5V		7.0	3.8	mA	@ 1 MHz	[5,6,7]
	3.0V		5.8	2.5	mA	@ 2 MHz	[5,6,7]
	5.5V		9.0	4.0	mA	@ 2 MHz	[5,6,7]
	3.0V		8.0	3.0	mA	@ 4 MHz	[5,6,7]
	5.5V		11.0	4.4	mA	@ 4 MHz	[5,6,7]
I _{CC1} Standby Current (Low Noise Halt Mode)	3.0V		2.5	0.7	mA	@ 1 MHz	[6,7,8]
	5.5V		4.0	2.5	mA	@ 1 MHz	[6,7,8]
	3.0V		3.0	0.9	mA	@ 2 MHz	[6,7,8]
	5.5V		4.5	2.8	mA	@ 2 MHz	[6,7,8]
	3.0V		4.0	1.0	mA	@ 4 MHz	[6,7,8]
	5.5V		5.0	3.0	mA	@ 4 MHz	[6,7,8]
I _{CC2} Standby Current (Stop Mode)	3.0V		10	1.0	μA		[6,7,8,9]
	3.0V		20	1.0	μA		[6,7,8,10]
	5.5V		10	1.0	μA		[6,7,8,9]
	5.5V		20	1.0	μA		[6,7,8,10]
I _{ALL} Auto Latch Low Current	3.0V		12	3.0	μA	0V < V _{IN} < V _{CC}	
	5.5V		32	16	μA	0V < V _{IN} < V _{CC}	
I _{ALH} Auto Latch High Current	3.0V		-8	-1.5	μA	0V < V _{IN} < V _{CC}	
	5.5V		-16	-8.0	μA	0V < V _{IN} < V _{CC}	

Notes:

1. Port 0, 2, and 3 only.
2. V_{SS} = 0V = GND.
3. The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature.
4. V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
5. Standard mode (not Low EMI mode).
6. Inputs at V_{CC} or V_{SS}, outputs unloaded.
7. Halt mode and Low EMI mode.
8. WDT not running.
9. T_A = 0°C to 70°C.
10. T_A = 40°C to 105°C.

Sym	Parameter	V _{CC} [4]	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC}	Supply Current	2.0V		3.3		mA	@ 2 MHz	[5,6]
		3.9V		6.8		mA	@ 2 MHz	[5,6]
		2.0V		6.0		mA	@ 8 MHz	[5,6]
		3.9V		9.0		mA	@ 8 MHz	[5,6]
I _{CC1}	Standby Current (Halt Mode)	2.0V		2.3		mA	@ 2 MHz	[5,6,7]
		3.9V		3.8		mA	@ 2 MHz	[5,6,7]
		2.0V		3.8		mA	@ 8 MHz	[5,6,7]
		3.9V		4.8		mA	@ 8 MHz	[5,6,7]
I _{CC2}	Standby Current (Stop Mode)	2.0V		10	1.0	μA		[6,7]
		3.9V		10	1.0	μA		[6,7]
I _{ALL}	Auto Latch Low Current	2.0V		12	3.0	μA	0V < V _{IN} < V _{CC}	
		3.9V		32	16	μA	0V < V _{IN} < V _{CC}	
I _{ALH}	Auto Latch High Current	2.0V		-8	-1.5	μA	0V < V _{IN} < V _{CC}	
		3.9V		-16	-8.0	μA		

Notes:

1. Port 0, 2, and 3 only
2. V_{SS} = 0V = GND. The device operates down to V_{LV}. The minimum operational V_{CC} is determined by the value of the voltage V_{LV} at the ambient temperature.
3. V_{CC} = 2.0V to 3.9V, typical values measured at V_{CC} = 3.3 V.
4. Standard Mode (not Low EMI mode).
5. Inputs at V_{CC} or V_{SS}, outputs are unloaded.
6. WDT is not running.

		$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$					
		$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			Typical		
Sym.	Parameter	V_{CC} [4]	Min	Max	@ 25°C	Units	Conditions
I_{CC}	Supply Current	4.5V		9.0	3.8	mA	@ 2 MHz
		5.5V		9.0	3.8	mA	@ 2 MHz
		4.5V		15.0	4.4	mA	@ 8 MHz
		5.5V		15.0	4.4	mA	@ 1 MHz
I_{CC1}	Standby Current (HALT mode)	4.5V		4.0	2.5	mA	@ 2 MHz
		5.5V		4.0	2.5	mA	@ 2 MHz
		4.5V		5.0	3.0	mA	@ 4 MHz
		5.5V		5.0	3.0	mA	@ 4 MHz
I_{CC}	Supply Current (Low Noise Mode)	4.5V		9.0	3.8	mA	
		5.5V		9.0	3.8	mA	
		4.5V		11.0	4.0	mA	@ 2 MHz
		5.5V		11.0	4.0	mA	@ 2 MHz
		4.5V		15.0	4.4	mA	@ 4 MHz
		5.5V		15.0	4.4	mA	@ 4 MHz
I_{CC1}	Standby Current (Low Noise Halt Mode)	4.5V		4.0	2.5	mA	@ 1 MHz
		5.5V		4.0	2.5	mA	@ 1 MHz
		4.5V		4.5	2.7	mA	@ 2 MHz
		5.5V		4.5	2.7	mA	@ 2 MHz
		4.5V		5.0	3.0	mA	@ 4 MHz
		5.5V		5.0	3.0	mA	@ 4 MHz
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	1.0	μA	
		4.5V		20	1.0	μA	
		5.5V		10	1.0	μA	
		5.5V		20	1.0	μA	
I_{ALL}	Auto Latch Low Current	4.5V		32	16	μA	$0V < V_{IN} < V_{CC}$
		5.5V		32	16	μA	$0V < V_{IN} < V_{CC}$
ALH	Auto Latch High	4.5V		-16	-8.0	μA	$0V < V_{IN} < V_{CC}$
		5.5V		-16	-8.0	μA	$0V < V_{IN} < V_{CC}$

Notes:

1. Port 0, 2, and 3 only.
2. $V_{SS} = 0V = \text{GND}$.
3. The device operates down to V_{LV} of the specified frequency for V_{LV} . The minimum operational V_{CC} is determined by the value of the voltage V_{LV} at the ambient temperature.
4. The V_{LV} increases as the temperature decreases.
5. $V_{CC} = 4.5V$ to $5.5V$, typical values measured at $V_{CC} = 5.0V$.
6. Standard mode (not Low EMI mode).
7. Inputs at V_{CC} or V_{SS} , outputs unloaded.
8. WDT not running.
9. Halt mode and Low EMI mode.
10. $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$. $T_A = -40^{\circ}\text{C to } 105^{\circ}\text{C}$.

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software

control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 9).

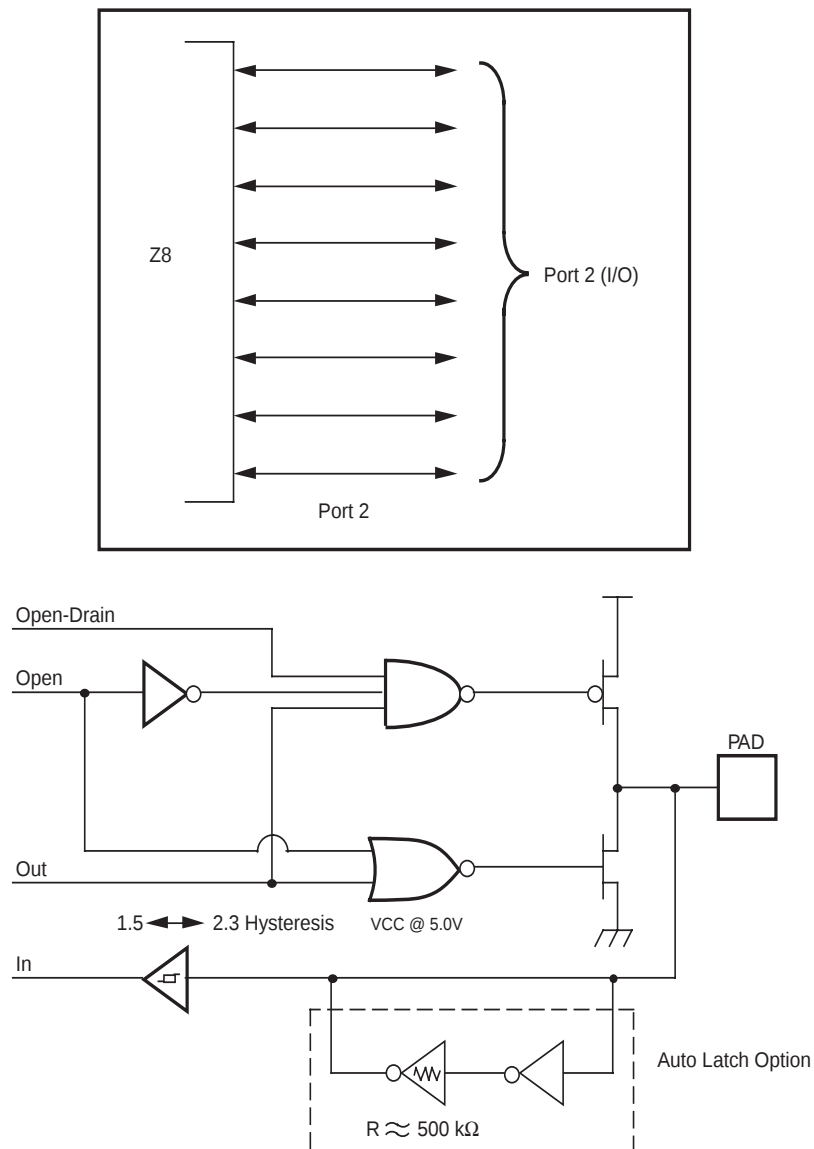


Figure 9. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3, P33-P31. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal T_{IN} (Figure 10).

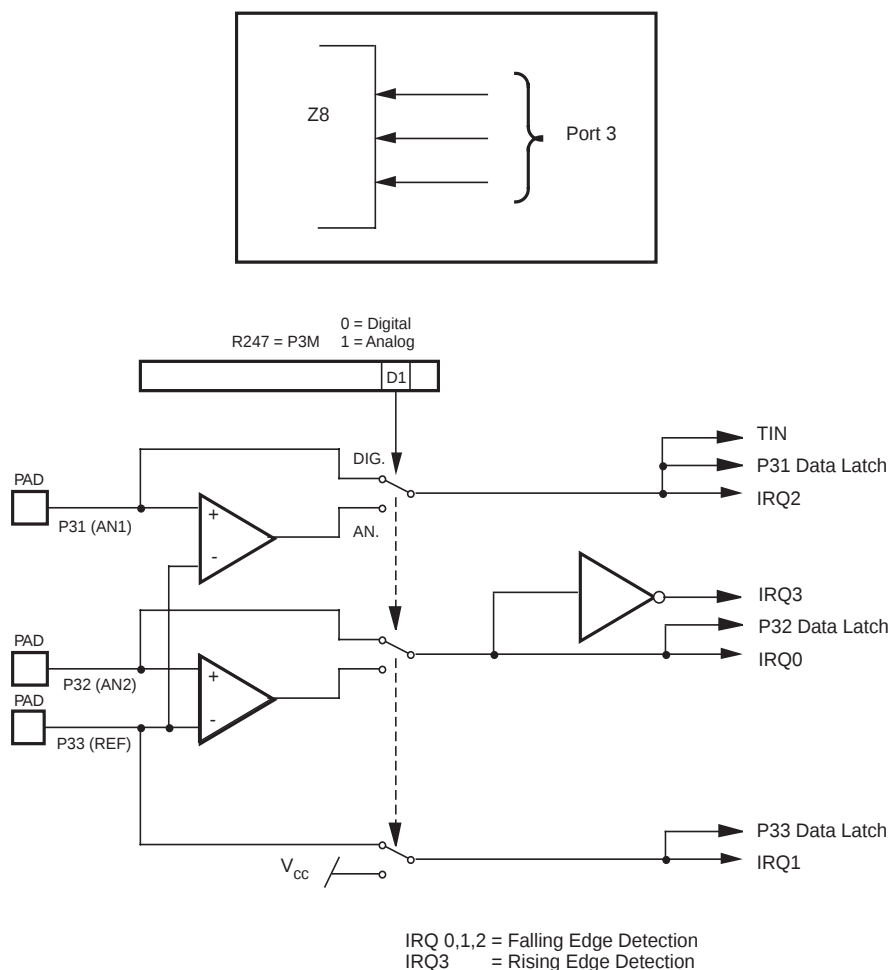


Figure 10. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4 V when the V_{CC}

is 5.0 V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION (Continued)

Program Memory. The Z8 addresses up to 512 bytes of internal program memory (Figure 12). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-511 are on-chip one-time programmable ROM.

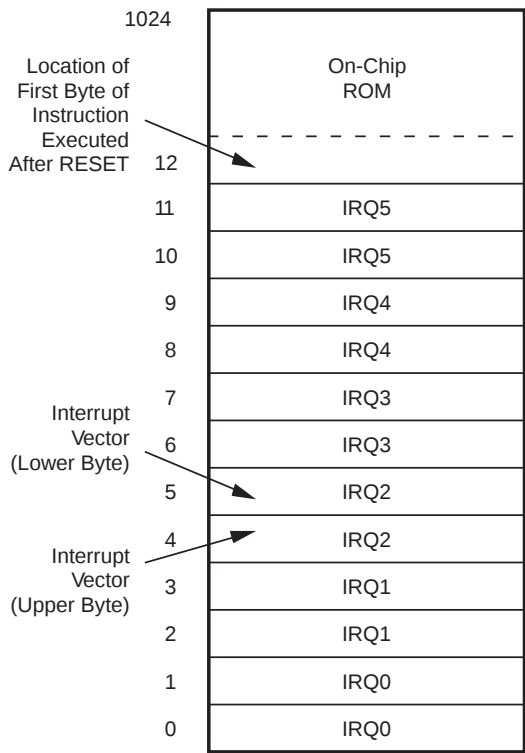


Figure 12. Program Memory Map

Register File. The Register File consists of three I/O port registers, 61 general-purpose registers, and 12 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 13). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 14) addresses the starting location of the active working-register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Reserved	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	To Prescaler	PRE0
244	Timer/Counter0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter1	T1
241	Timer Mode	TMR
240	Not Implemented	
128	General Purpose Registers	
127		
4		
3		
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 13. Register File

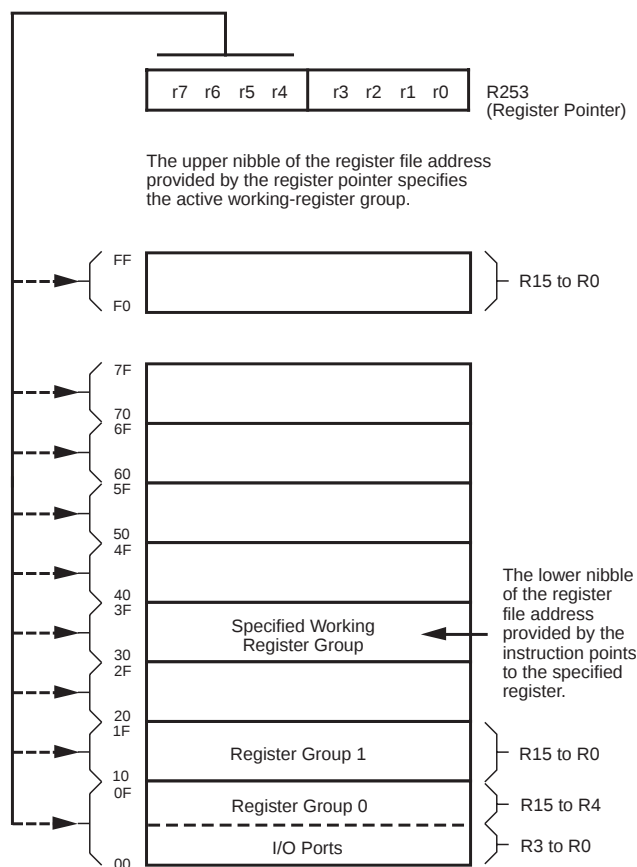


Figure 14. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers. It is set to 00Hex after any reset.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register. But is set to 00Hex after any reset.

Counter/Timer. There is an 8-bit programmable counter/timers (T1), each driven by its 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. (Figure 15).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler

drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counter, but not the prescaler, is read at any time without disturbing its value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

FUNCTIONAL DESCRIPTION (Continued)

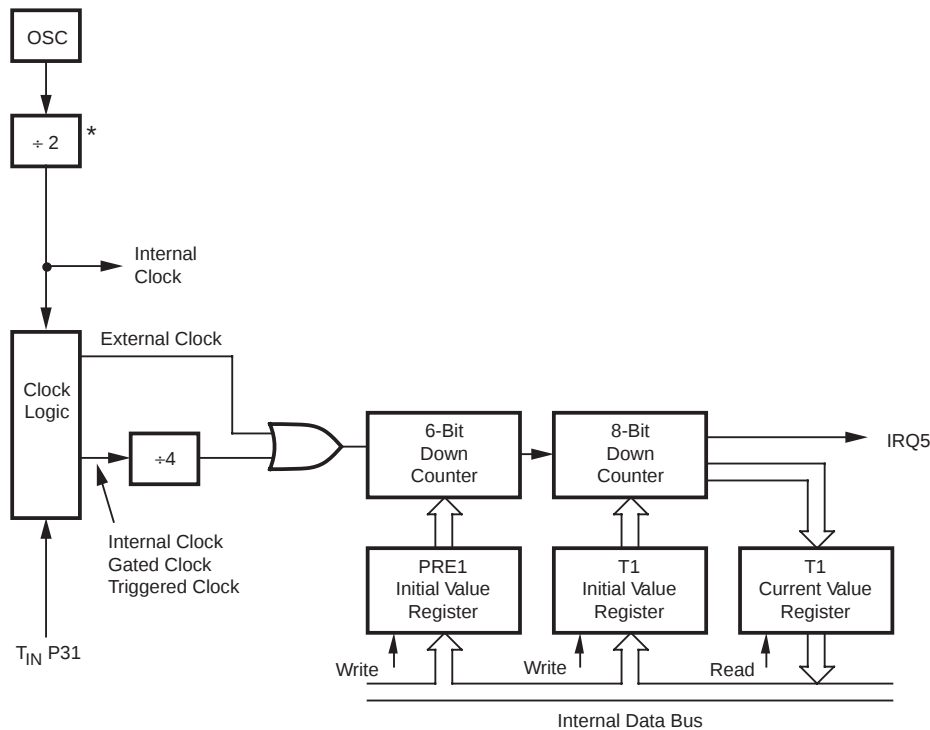


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z8 has five interrupts from four different sources. These interrupts are maskable and prioritized (Figure 16). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the five interrupt requests (Table 5).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

User must select any Z86E08 mode in Zilog's C12 ICE-BOX™ emulator. The rising edge interrupt is not directly supported on the Z86CCP00ZEM emulator.

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	Reserved	8,9	Reserved
IRQ5	T1	10,11	Internal

Notes:

F = Falling edge triggered

R = Rising edge triggered

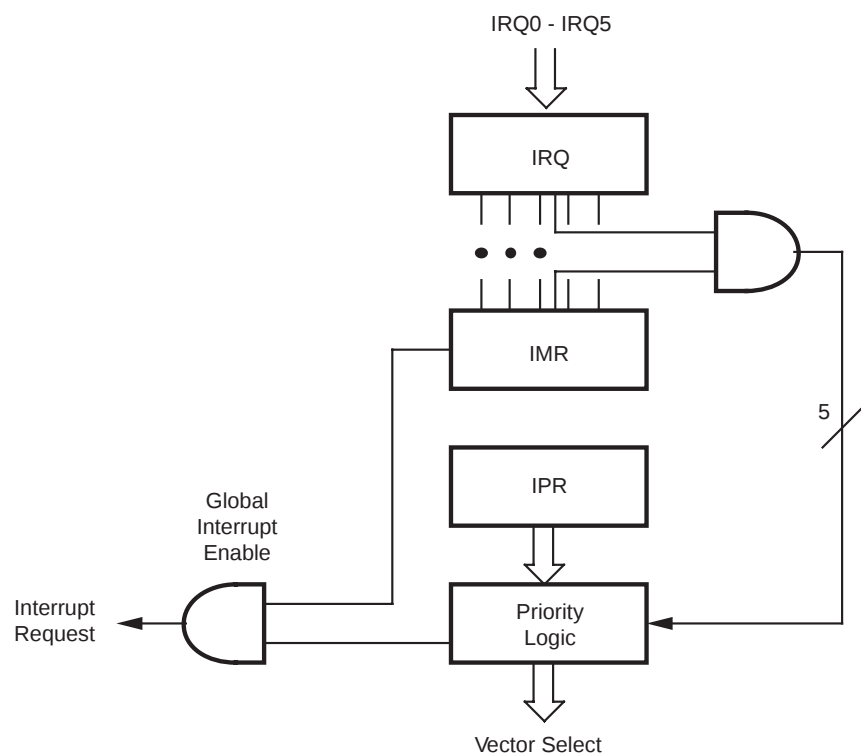


Figure 16. Interrupt Block Diagram

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal or ceramic resonator should be connected across XTAL1 and XTAL2 using the vendors crystal or ceramic resonator recommended capacitors from each pin directly to device ground pin 14 (Figure 17). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

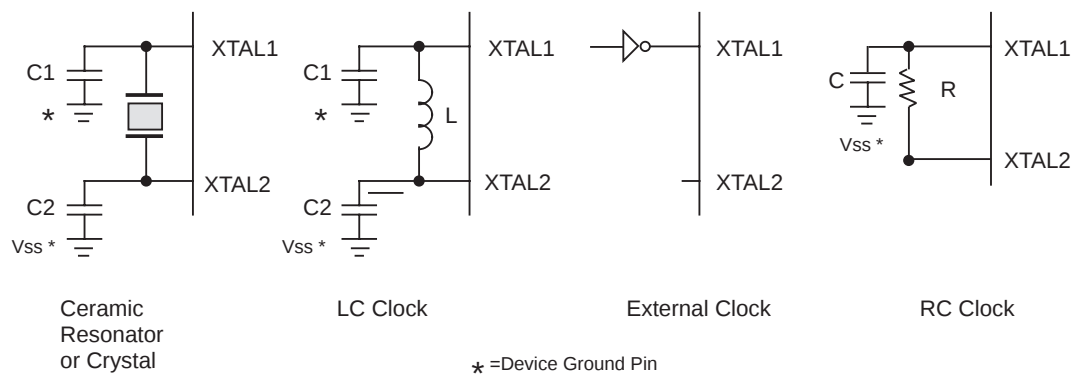


Figure 17. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μ A. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Notes:

X = Dependent on user's application.
Stop-Mode Recovery pin P27 is not edge triggered.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP mode
or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0. WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT} ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR} , plus 18 XTAL clock cycles. The WDT does not run in stop mode, unless the permanent WDT enable option is selected. The WDT does not run in halt mode unless WDH instruction is executed or permanent WDT enable option is selected.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Note: Opcode WDH and permanently enabled WDT is not directly supported by the Z86CCP00ZEM.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV} . Figure 18 shows the Auto Reset Voltage versus temperature.

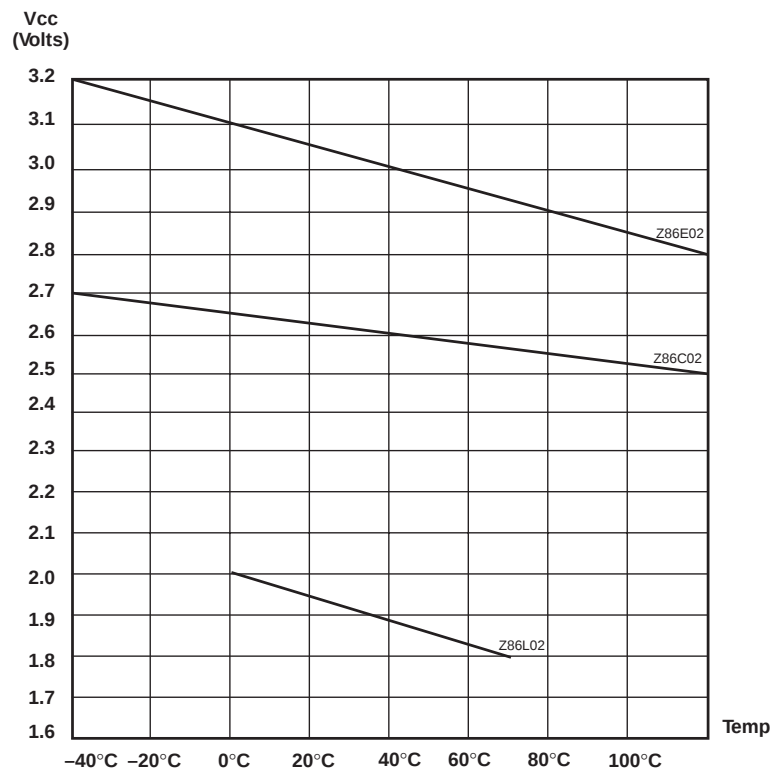


Figure 18. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

Options

The Z86C02/E02/L02 offers ROM protect, Low Noise, Auto Latch Disable, RC Oscillator, and Permanent WDT enable features as options. The Z86E02 must be power cycled to fully implement the selected option after programming.

Low Noise. The Z8 can operate in a low EMI emission mode by selecting the low noise option. Use of this feature will result in:

- All drivers slew rates are reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation is limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry is eliminated.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI are supported. (However, instructions LDE and LDEI are not supported.)

EPROM/TEST MODE Disable. When selected, this bit will permanently disable EPROM and Factory Test mode.

Auto Latch Disable. Auto Latch Disable option when Selected will globally disable all Auto Latches.

RC. RC Oscillator option when selected will allow using a resistor (R) and a capacitor (C) as a clock source.

WDT Enable. WDT Enable option bit when selected will have the WDT permanently enabled in all modes and can not be stopped in HALT or STOP Mode.

EPROM Mode Description. In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as V_{PP} , and P02 functions as /PGM.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. Table 6 shows the programming voltage of each mode of Z86E02.

FUNCTIONAL DESCRIPTION (Continued)

Table 6. EPROM Programming Table

Programming Modes	V _{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V _{CC} *
EPROM READ	NU	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	5.0V
PROGRAM	V _H	V _{IH}	V _{IL}	V _{IH}	V _{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V _H	V _{IH}	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	6.4V
ROM PROTECT	V _H	V _H	V _H	V _{IH}	V _{IL}	NU	NU	5.0-6.4V
LOW NOISE SELECT	V _H	V _{IH}	V _H	V _{IH}	V _{IL}	NU	NU	5.0-6.4V
AUTO LATCH DISABLE	V _H	V _{IH}	V _H	V _{IL}	V _{IL}	NU	NU	5.0-6.4V
WDT ENABLE	V _H	V _{IL}	V _H	V _{IH}	V _{IL}	NU	NU	5.0-6.4V
EPROM/TEST MODE Disable	V _H	V _{IL}	V _H	V _{IL}	V _{IL}	NU	NU	5.0-6.4V

Notes: V_H=13.0V ±0.25 V_{DC}.

V_{IH}=As per specific Z8 DC specification.

V_{IL}=As per specific Z8 DC specification.

X=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.

NU=Not used, but must be set to either V_{IH} or V_{IL} level.

I_{PP} during programming = 40 mA maximum.

I_{CC} during programming, verify, or read = 40 mA maximum.

* V_{CC} has a tolerance of ±0.25V.

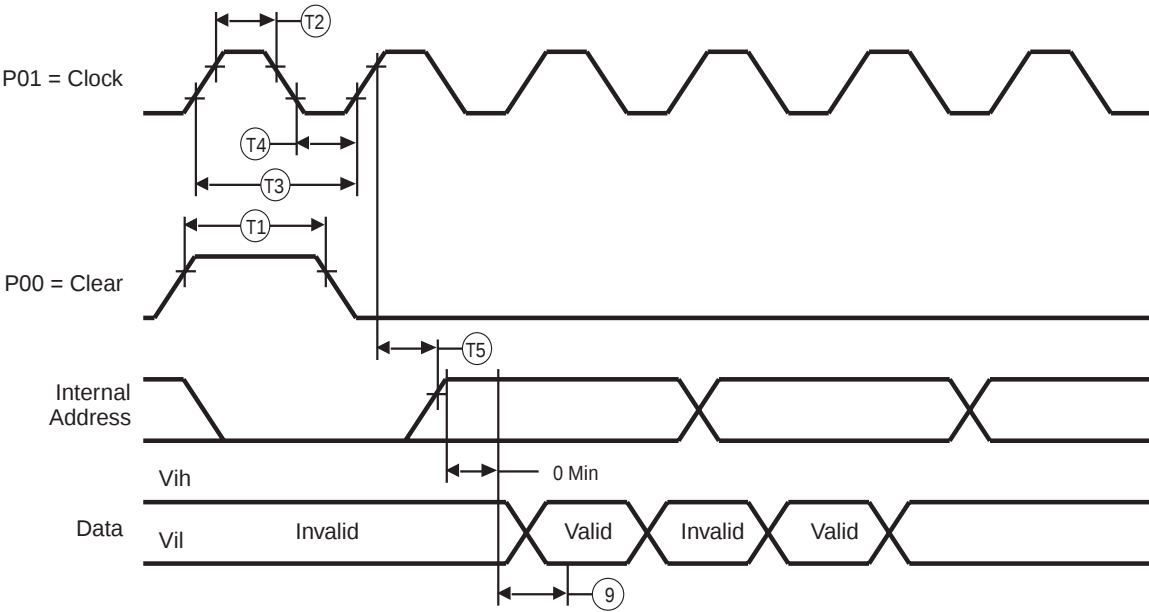
Internal Address Counter. The address of Z86E02 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 19 shows the setup time of the serial address input.

Programming Waveform. Figures 20, 21, 22, and 23 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

Programming Algorithm. Figure 24 shows the flow chart of the Z86E02 programming algorithm.

Table 7. Z86E02 Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		μs
8	/OE Setup Time	2		μs
9	Data Access Time	188	4000	ns
10	Data Output Float Time		100	ns
11	Over-program Pulse Width	2.85	3.2	ms
12	EPM Setup Time	2		μs
13	/PGM Setup Time	2		μs
14	Address to /OE Setup Time	2		μs
15	Option Program Pulse Width	150		ms
16	/OE Low Width	250		ns



Legend:		
T1	Reset Clock Width	30 ns Min
T2	Input Clock High	30 ns Min
T3	Input Clock Period	70 ns Min
T4	Input Clock Low	30 ns Min
T5	Clock to Address Counter Out Delay	15 ns Max

Figure 19. Z86E02 Address Counter Waveform

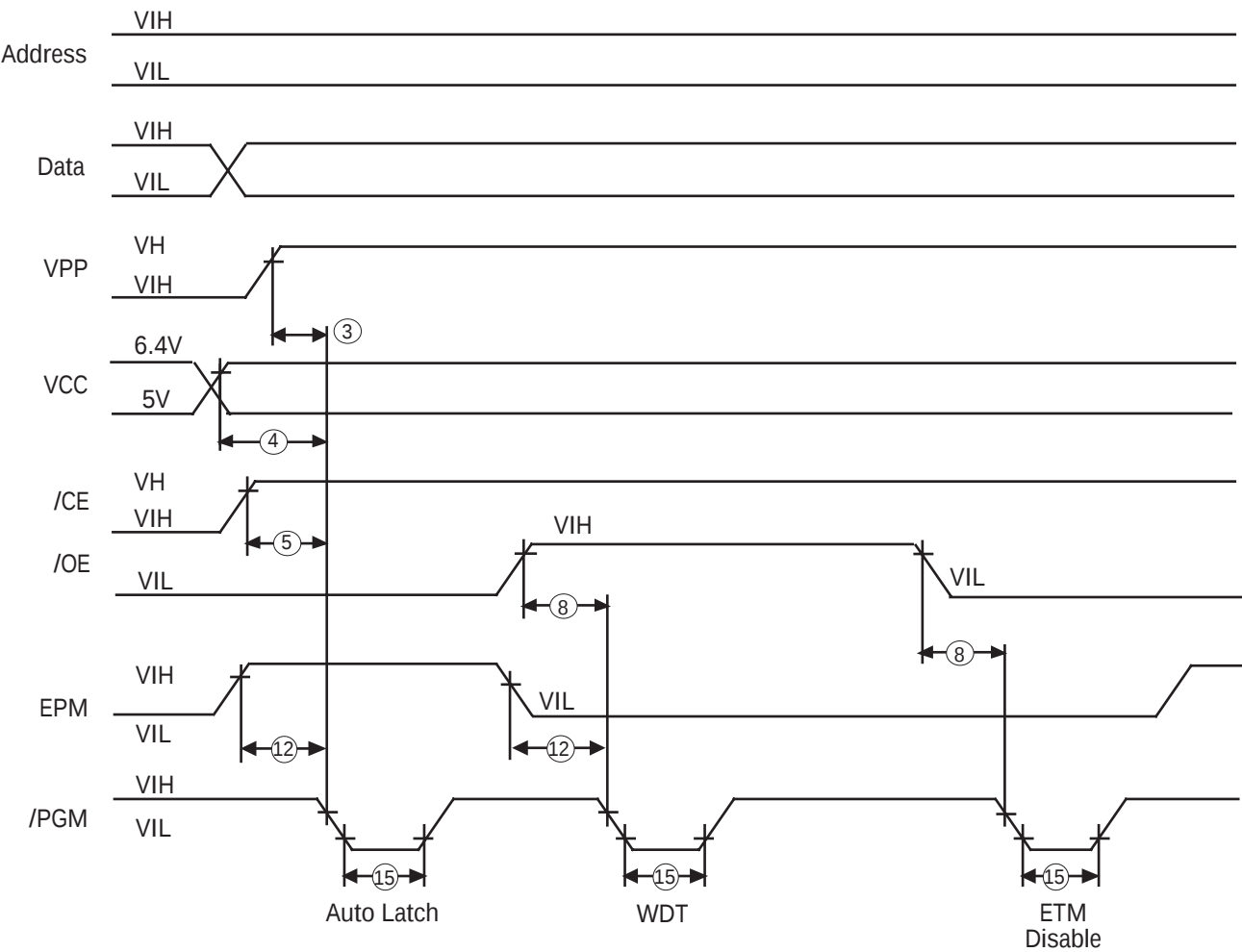


Figure 21. Z86E02 Programming Waveform (Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

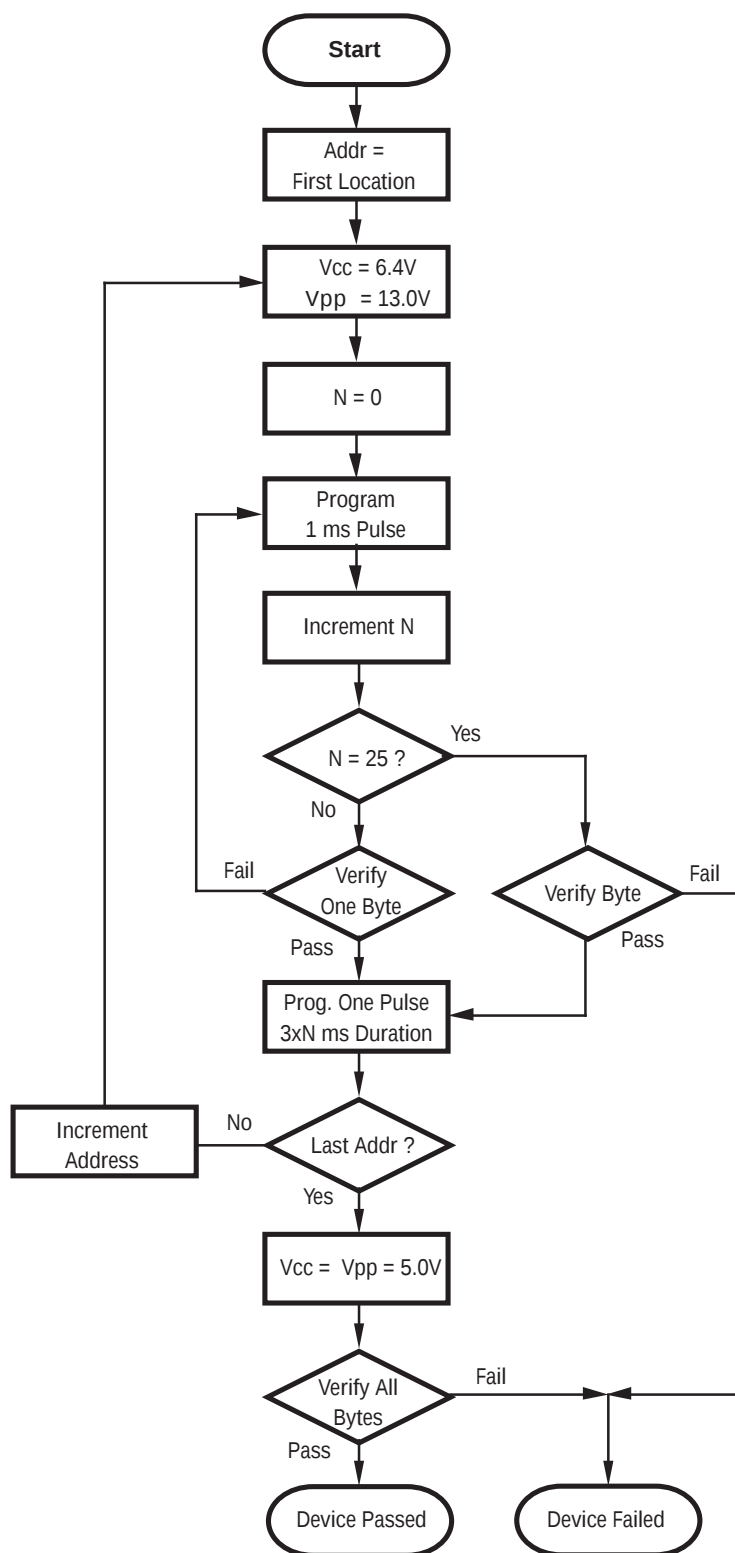
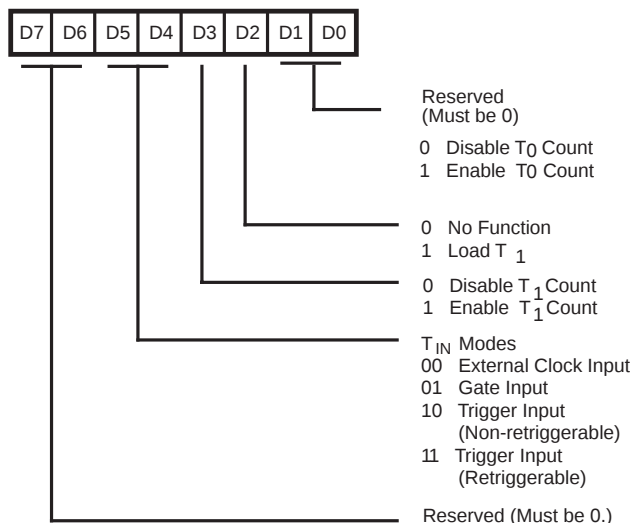


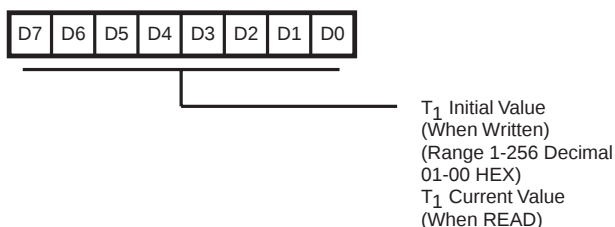
Figure 24. Z86E02 Programming Algorithm

Z8 CONTROL REGISTERS

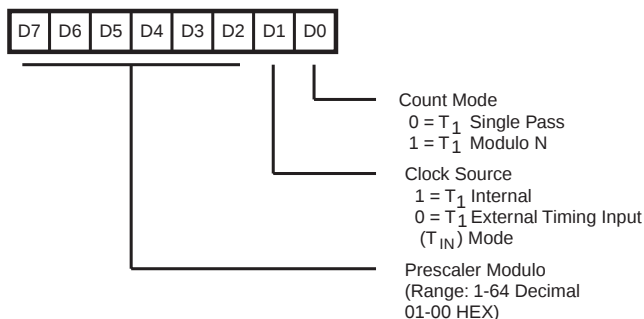
R241 TMR

Figure 25. Timer Mode Register (F1_H: Read/Write)

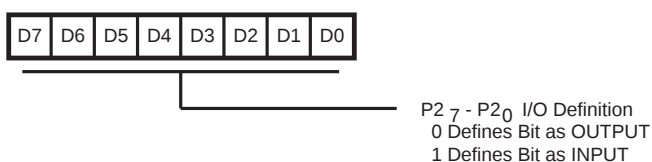
R242 T1

Figure 26. Counter Timer 1 Register (f2_H: Read/Write)

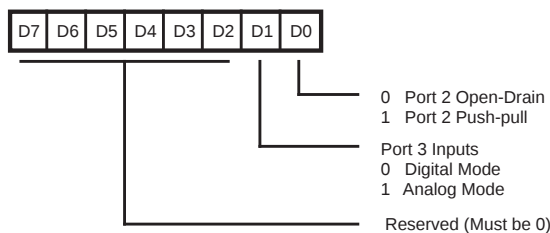
R243 PRE1

Figure 27. Prescaler! Register (F3_H: Write Only)

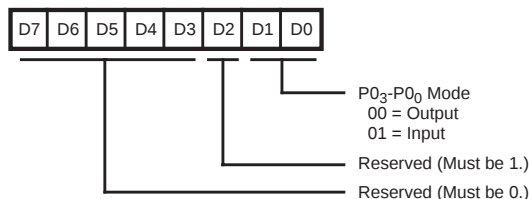
R246 P2M

Figure 28. Port 2 Mode Register (F6_H: Write Only)

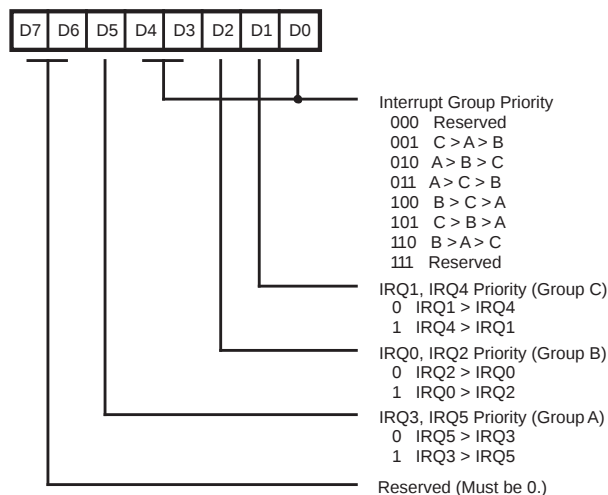
R247 P3M

Figure 29. Port 3 Mode Register (F7_H: Write Only)

R248 P01M

Figure 30. Port 0 and 1 Mode Register (F8_H: Write Only)

R249 IPR

Figure 31. Interrupt Priority Register (F9_H: Write Only)

Z8 CONTROL REGISTERS (Continued)

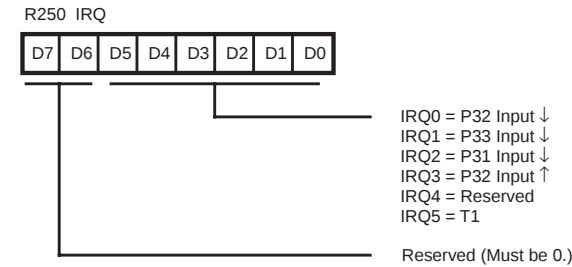


Figure 32. Interrupt Request Register (FA_H: Read/Write)



Figure 33. Interrupt Mask Register (FB_H: Read/Write)

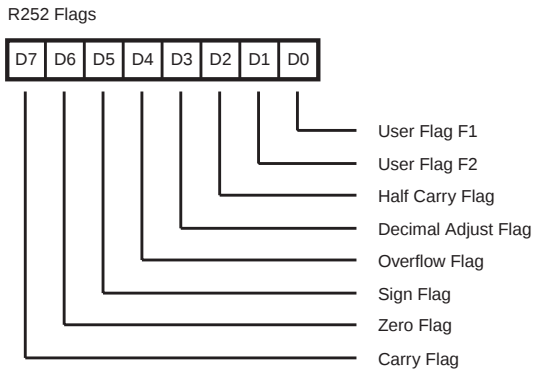


Figure 34. Flag Register (FC_H: Read/Write)

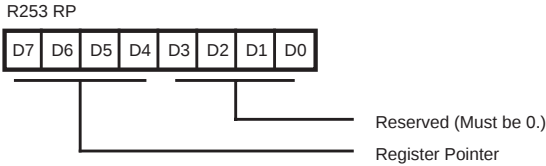


Figure 35. Register Pointer FD_H: Read/Write)

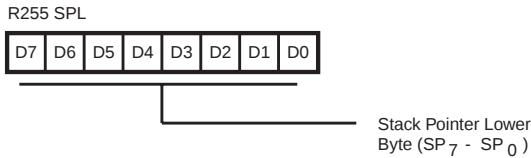


Figure 36. Stack Pointer (FF_H: Read/Write)