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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c0208pscr4448

GENERAL DESCRIPTION (Continued)

cations. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

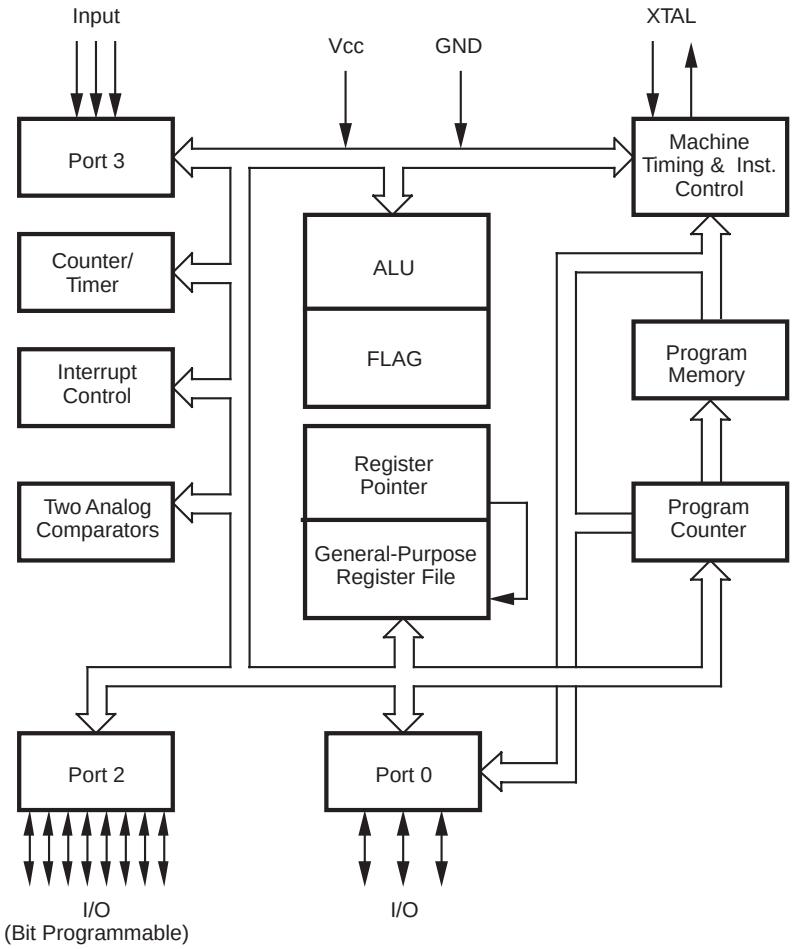

Figure 1. Z86C02/E02/L02 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

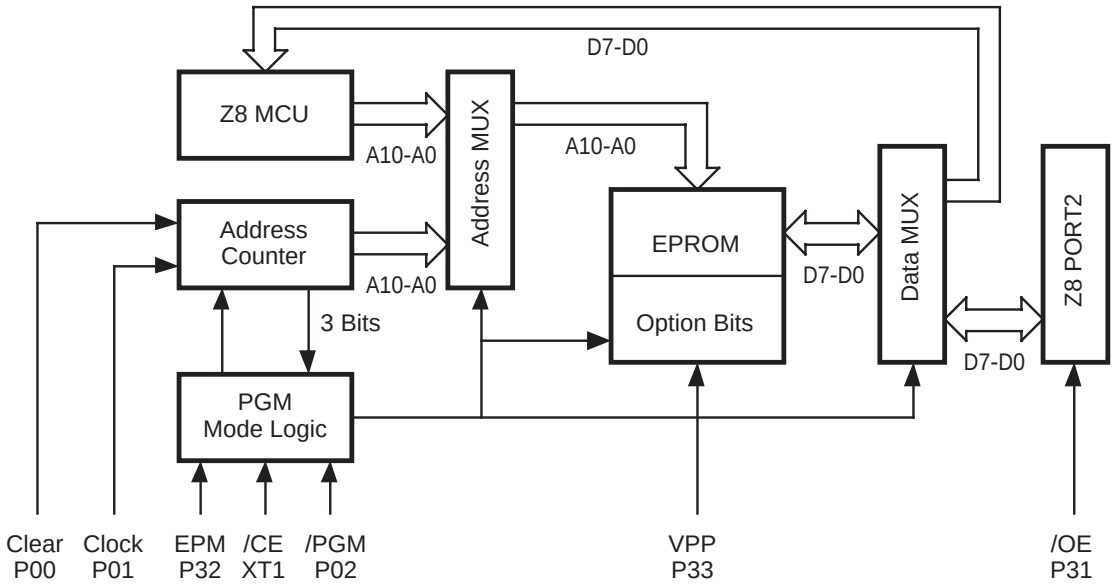

Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTIONS

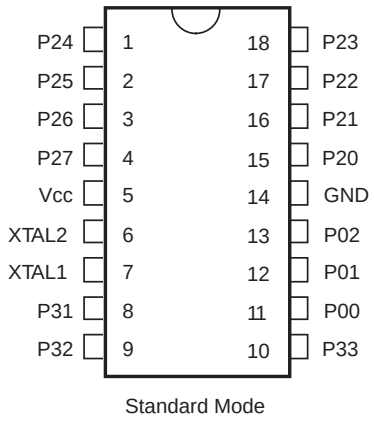

Figure 3. 18-Pin Standard Mode Configuration

Table 1. 18-Pin Standard Mode Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.7	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2] (Z86C02/L02)	–0.7	V_{DD}+1	V
Voltage on Pin 7,8,9,10 with Respect to V_{SS} [Note 2] (Z86E02)	–0.7	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Allowed Current out of V_{SS}		300	mA
Maximum Allowed Current into V_{DD}		270	mA
Maximum Allowed Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowed Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowed Output Current Sinked by Any I/O Pin		20	mA
Maximum Allowed Output Current Sourced by Any I/O Pin		20	mA
Maximum Allowed Output Current Sinked by Port 2, Port 0		80	mA
Maximum Allowed Output Current Sourced by Port 2, Port 0		80	mA

Notes:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

1. This applies to all pins except where otherwise noted.
2. Maximum current into pin must be ±600µA. There is no input protection diode from pin to V_{DD}.
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 6).

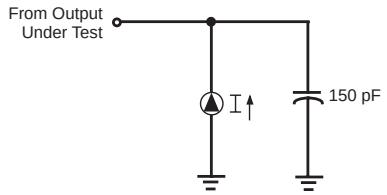

Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Z86C02

Sym.	Parameter	V_{CC} [4]	T_A = 40°C to +105°C T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		[1]
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		[1]
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	0.8	V		[1]
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		[1]
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	[5]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[5]
		3.0V	V_{CC}–0.4		3.0	V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I_{OL} = +4.0 mA	[5]
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	[5]
		3.0V		0.8	0.2	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0	0.8	V	I_{OL} = +12 mA	[5]
		5.5V		0.8	0.3	V	I_{OL} = +12 mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset					V		
			2.2	2.8	2.6	V		[9]
			2.0	3.0	2.6	V		[10]
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{VICR}	Comparator Input Common Mode Voltage Range		V_{SS}–0.3	V_{CC} –1.0		V		[9]
			V_{SS}–0.3	V_{CC} –1.5		V		[10]

DC CHARACTERISTICS

Z86L02

Sym.	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	0.1 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS}–0.3	0.1 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.9 V_{CC}	V_{CC}+0.3		V		[1]
		3.9V	0.9 V_{CC}	V_{CC}+0.3		V		[1]
V_{IL}	Input Low Voltage	2.0V	V_{SS}–0.3	0.1 V_{CC}		V		[1]
		3.9V	V_{SS}–0.3	0.1 V_{CC}		V		[1]
V_{OH}	Output High Voltage	2.0V	V_{CC}–0.4		3.0	V	I_{OH} = – 500 µA	[5]
		3.9V	V_{CC}–0.4		3.0	V	I_{OH} = –500 µA	[5]
V_{OL1}	Output Low Voltage	2.0V		0.8	0.2	V	I_{OL} = +1.0 mA	[5]
		3.9V		0.4	0.1	V	I_{OL} = +1.0 mA	[5]
V_{OL2}	Output Low Voltage	2.0V		1.0	0.8	V	I_{OL} = + 3.0 mA	[5]
		3.9V		0.8	0.3	V	I_{OL} = + 3.0 mA	[5]
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.4	2.15		V		
I_{IL}	Input Leakage (Input Bias Current of Comparator)	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V^{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{VICR}	Comparator Input Common Mode Voltage Range		V_{SS} –0.3	V_{CC} –1.0		V		

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	2.0V		3.3		mA	@ 2 MHz	[5,6]
		3.9V		6.8		mA	@ 2 MHz	[5,6]
		2.0V		6.0		mA	@ 8 MHz	[5,6]
		3.9V		9.0		mA	@ 8 MHz	[5,6]
I_{CC1}	Standby Current (Halt Mode)	2.0V		2.3		mA	@ 2 MHz	[5,6,7]
		3.9V		3.8		mA	@ 2 MHz	[5,6,7]
		2.0V		3.8		mA	@ 8 MHz	[5,6,7]
		3.9V		4.8		mA	@ 8 MHz	[5,6,7]
I_{CC2}	Standby Current (Stop Mode)	2.0V		10	1.0	µA		[6,7]
		3.9V		10	1.0	µA		[6,7]
I_{ALL}	Auto Latch Low Current	2.0V		12	3.0	µA	$0V < V_{IN} < V_{CC}$	
		3.9V		32	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	2.0V		–8	-1.5	µA	$0V < V_{IN} < V_{CC}$	
		3.9V		–16	-8.0	µA		

Notes:

1. Port 0, 2, and 3 only
2. V_{SS} = 0V = GND.The device operates down to V_{LV}. The minimum operational V_{CC} is determined by the value of the voltage V_{LV} at the ambient temperature.
3. V_{CC} = 2.0V to 3.9V, typical values measured at V_{CC} = 3.3 V.
4. Standard Mode (not Low EMI mode).
5. Inputs at V_{CC} or V_{SS}, outputs are unloaded.
6. WDT is not running.

			T_A = –40°C to +105°C T_A = 0°C to +70°C		Typical			
Sym.	**Parameter**	**V_{CC} [4]**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	4.5V		9.0	3.8	mA	@ 2 MHz	[5,6]
		5.5V		9.0	3.8	mA	@ 2 MHz	[5,6]
		4.5V		15.0	4.4	mA	@ 8 MHz	[5,6]
		5.5V		15.0	4.4	mA	@ 1 MHz	[5,6]
I_{CC1}	Standby Current (HALT mode)	4.5V		4.0	2.5	mA	@ 2 MHz	[5,6]
		5.5V		4.0	2.5	mA	@ 2 MHz	[5,6]
		4.5V		5.0	3.0	mA	@ 4 MHz	[5,6]
		5.5V		5.0	3.0	mA	@ 4 MHz	[5,6]
I_{CC}	Supply Current (Low Noise Mode)	4.5V		9.0	3.8	mA		[6]
		5.5V		9.0	3.8	mA		[6]
		4.5V		11.0	4.0	mA	@ 2 MHz	[6]
		5.5V		11.0	4.0	mA	@ 2 MHz	[6]
		4.5V		15.0	4.4	mA	@ 4 MHz	[6]
		5.5V		15.0	4.4	mA	@ 4 MHz	[6]
I_{CC1}	Standby Current (Low Noise Halt Mode)	4.5V		4.0	2.5	mA	@ 1 MHz	[6,7,8]
		5.5V		4.0	2.5	mA	@ 1 MHz	[6,7,8]
		4.5V		4.5	2.7	mA	@ 2 MHz	[6,7,8]
		5.5V		4.5	2.7	mA	@ 2 MHz	[6,7,8]
		4.5V		5.0	3.0	mA	@ 4 MHz	[6,7,8]
		5.5V		5.0	3.0	mA	@ 4 MHz	[6,7,8]
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	1.0	µA		[6,7,9]
		4.5V		20	1.0	µA		[6,7,10]
		5.5V		10	1.0	µA		[6,7,9]
		5.5V		20	1.0	µA		6,7,10]
I_{ALL}	Auto Latch Low Current	4.5V		32	16	µA	0V <V_{IN}<V_{CC}	
		5.5V		32	16	µA	0V <V_{IN}<V_{CC}	
ALH	Auto Latch High	4.5V		–16	-8.0	µA	0V <V_{IN}<V_{CC}	
		5.5V		–16	–8.0	µA	0V <V_{IN}<V_{CC}	

Notes:

1. Port 0, 2, and 3 only.
2. V_{SS} = 0V = GND.
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined by the value of the voltage V_{LV} at the ambient temperature.
4. The V_{LV} increases as the temperature decreases.
5. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V.
6. Standard mode (not Low EMI mode).
7. Inputs at V_{CC} or V_{SS}, outputs unloaded.
8. WDT not running.
9. Halt mode and Low EMI mode.
10. T_A= 0˚C to 70˚C.T_A= –40˚C to 105˚C.

AC ELECTRICAL CHARACTERISTICS

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Figure 7. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A = –40°C to +105°C T_A= 0°C to +70°C 8 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	2.0V	125	DC	ns	[1]
			5.5V	125	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	[1]
			5.5V		25	ns	[1]
3	TwC	Input Clock Width	2.0V	62		ns	[1]
			5.5V	62		ns	[1]
4	TwTinL	Timer Input Low Width	2.0V	70		ns	[1]
			5.5V	70		ns	[1]
5	TwTinH	Timer Input High Width	2.0V	5TpC			[1]
			5.5V	5TpC			[1]
6	TpTin	Timer Input Period	2.0V	8TpC			[1]
			5.5V	8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Time	2.0V		100	ns	[1]
			5.5V		100	ns	[1]
8	TwIL	Int. Request Input Low Time	2.0V	70		ns	[1,2,3]
			5.5V	70		ns	[1,2,3]
9	TwIH	Int. Request Input High Time	3.0V	5TpC			[1,2,3]
			5.5V	5TpC			[1,2,3]
10	Twdt	Watch-Dog Timer Delay Time Before Time-Out	2.0V	25		ms	
			3.0V	10		ms	
			5.5V	5		ms	
11	Tpor	Power-On Reset Time	2.0V	70	250	ms	[4]
			3.0V	50	150	ms	[4]
			5.5V	10	70	ms	[4]
			2.0V	8	76	ms	[5]
			3.0V	4	38	ms	[5]
			5.5V	2	18	ms	[5]

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. IRQ 0,1,2 only.
4. Z86E02 only.
5. Z86C02/L02 only.

LOW NOISE VERSION

Low EMI Emission

The Z8 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option (Z86C02) or OTP bit option (Z86E02). Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM Code is submitted (for Z86C02 only).

PRECAUTION

Stack pointer register (SPL) at FFHex and general purpose register at FEHex are set to 00Hex after reset.

PIN FUNCTIONS

OTP Programming Mode

D7-D0 Data Bus. Data can be read from, or written to the EPROM through this data bus.

V_{CC} Power Supply. It is 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, etc.).

/CE Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input. This pin must toggle for each data output read.

EPM EPROM Program Mode. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear Clear (active High). This pin resets the internal address counter at the High Level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one with one clock cycle.

/PGM Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V_{PP}, /CE, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to $V_{CC.}$
- Adding a capacitor to the affected pin.

Port 2, P27-P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 9).

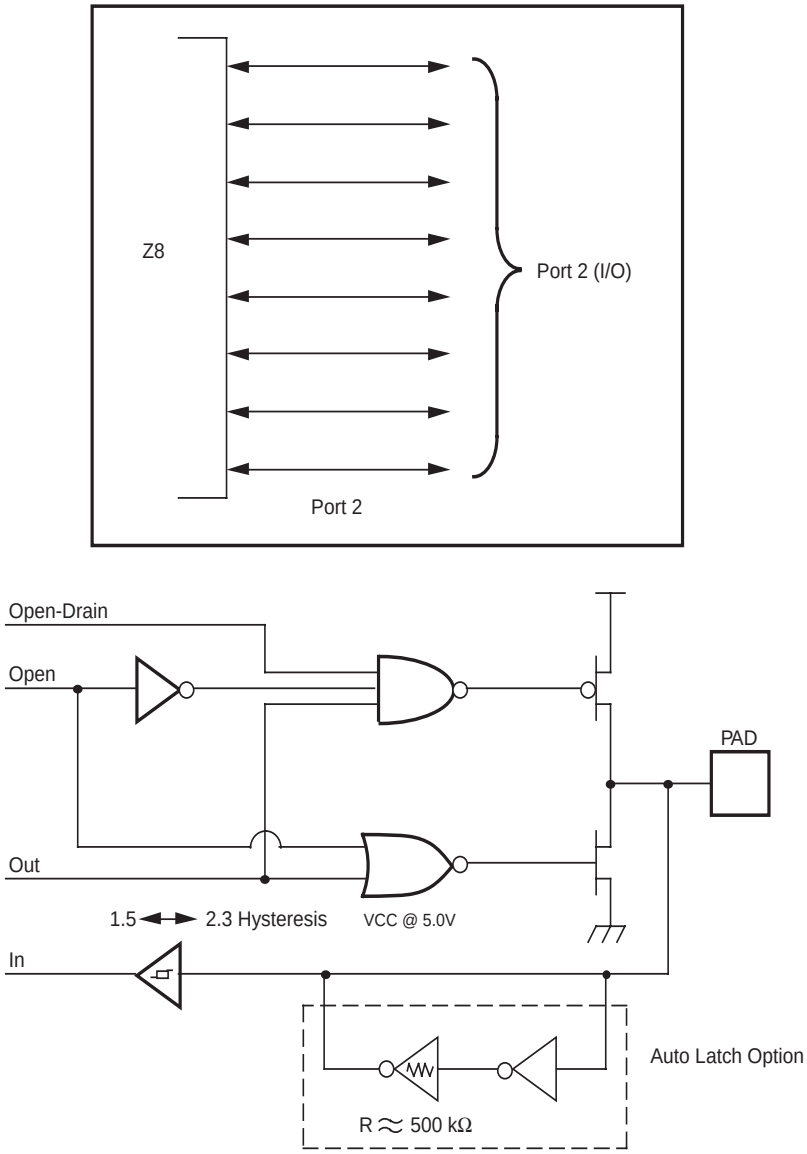


Figure 9. Port 2 Configuration

FUNCTIONAL DESCRIPTION (Continued)

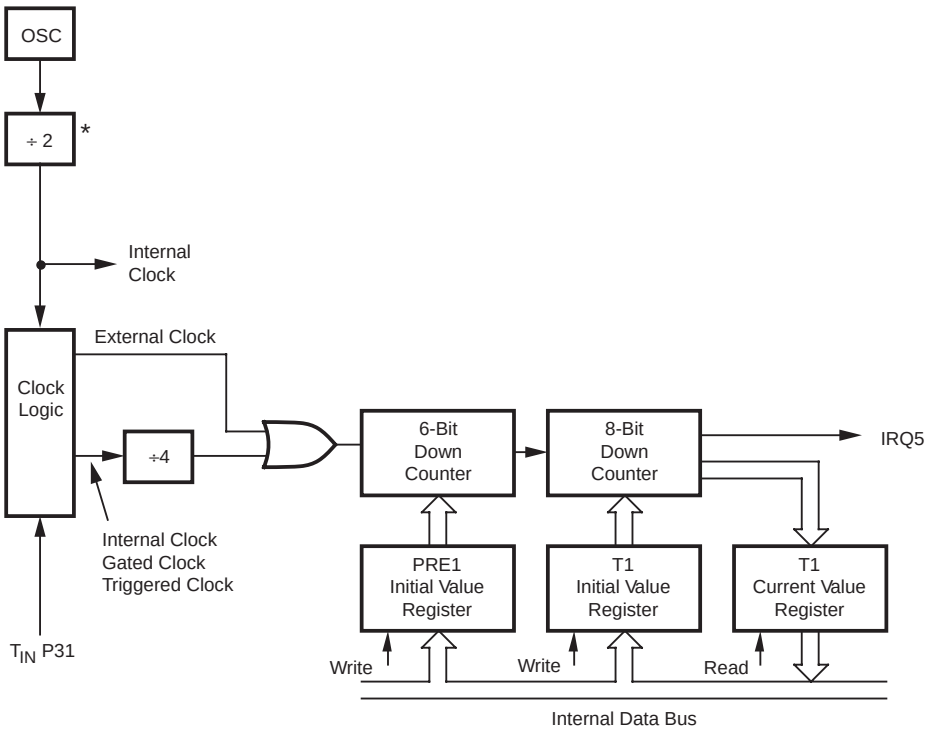


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z8 has five interrupts from four different sources. These interrupts are maskable and prioritized (Figure 16). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the five interrupt requests (Table 5).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

User must select any Z86E08 mode in Zilog's C12 ICE-BOX™ emulator. The rising edge interrupt is not directly supported on the Z86CCP00ZEM emulator.

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	Reserved	8,9	Reserved
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

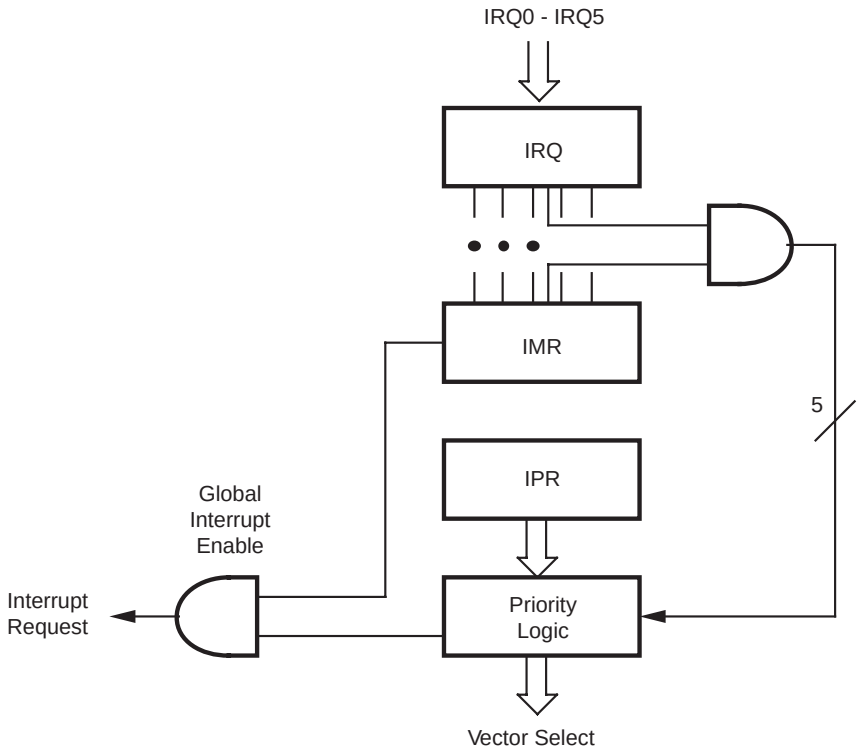


Figure 16. Interrupt Block Diagram

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal or ceramic resonator should be connected across XTAL1 and XTAL2 using the vendors crystal or ceramic resonator recommended capacitors from each pin directly to device ground pin 14 (Figure 17). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

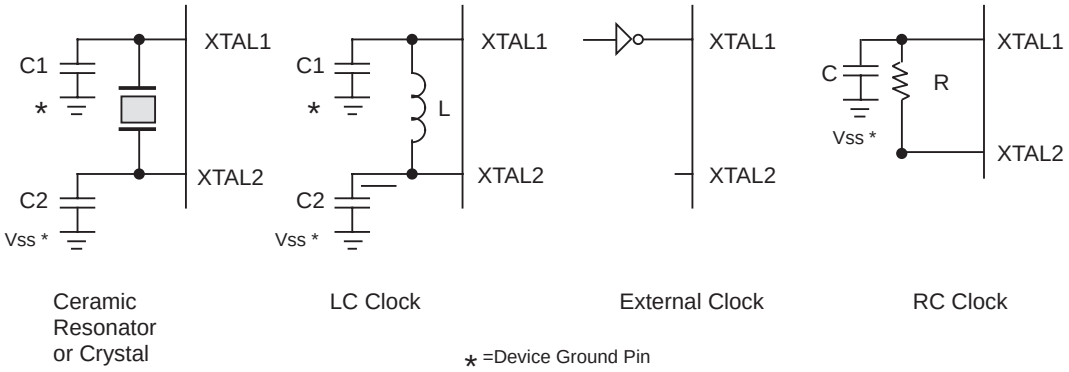


Figure 17. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 6. EPROM Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ	NU	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.0V
PROGRAM	V_H	V_{IH}	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_{IH}	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.4V
ROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V
AUTO LATCH DISABLE	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	5.0-6.4V
WDT ENABLE	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	5.0-6.4V
EPROM/TEST MODE Disable	V_H	V_{IL}	V_H	V_{IL}	V_{IL}	NU	NU	5.0-6.4V

Notes: V_H=13.0V ±0.25 V_{DC}.
V_{IH}=As per specific Z8 DC specification.
V_{IL}=As per specific Z8 DC specification.
X=Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU=Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

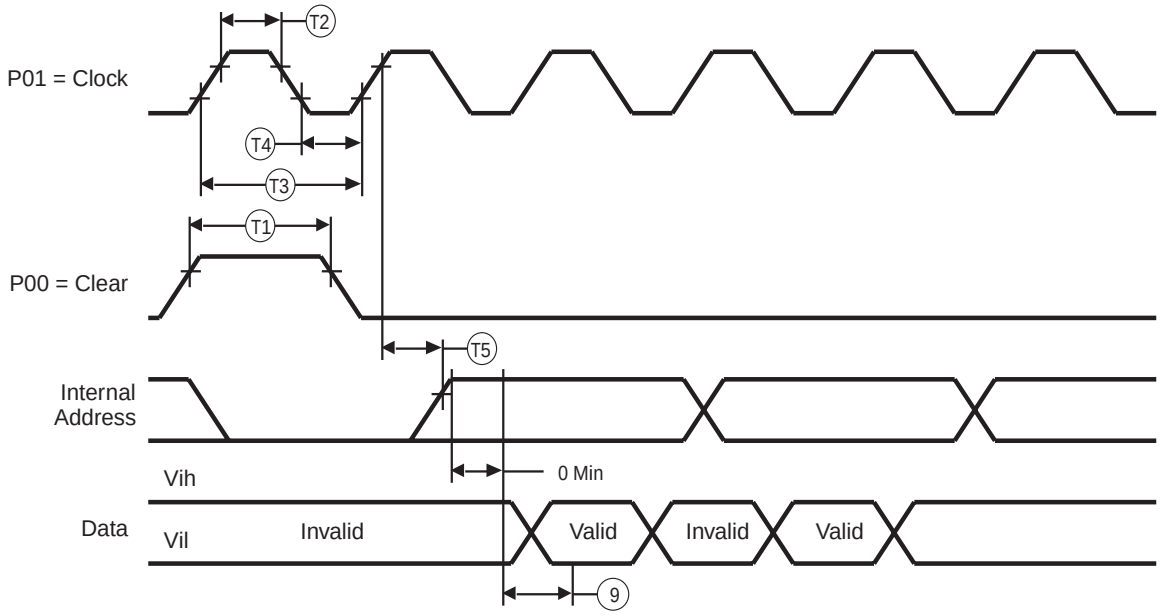
Internal Address Counter. The address of Z86E02 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 19 shows the setup time of the serial address input.

Programming Waveform. Figures 20, 21, 22, and 23 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

Programming Algorithm. Figure 24 shows the flow chart of the Z86E02 programming algorithm.

Table 7. Z86E02 Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time	188	4000	ns
10	Data Output Float Time		100	ns
11	Over-program Pulse Width	2.85	3.2	ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	150		ms
16	/OE Low Width	250		ns



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 19. Z86E02 Address Counter Waveform

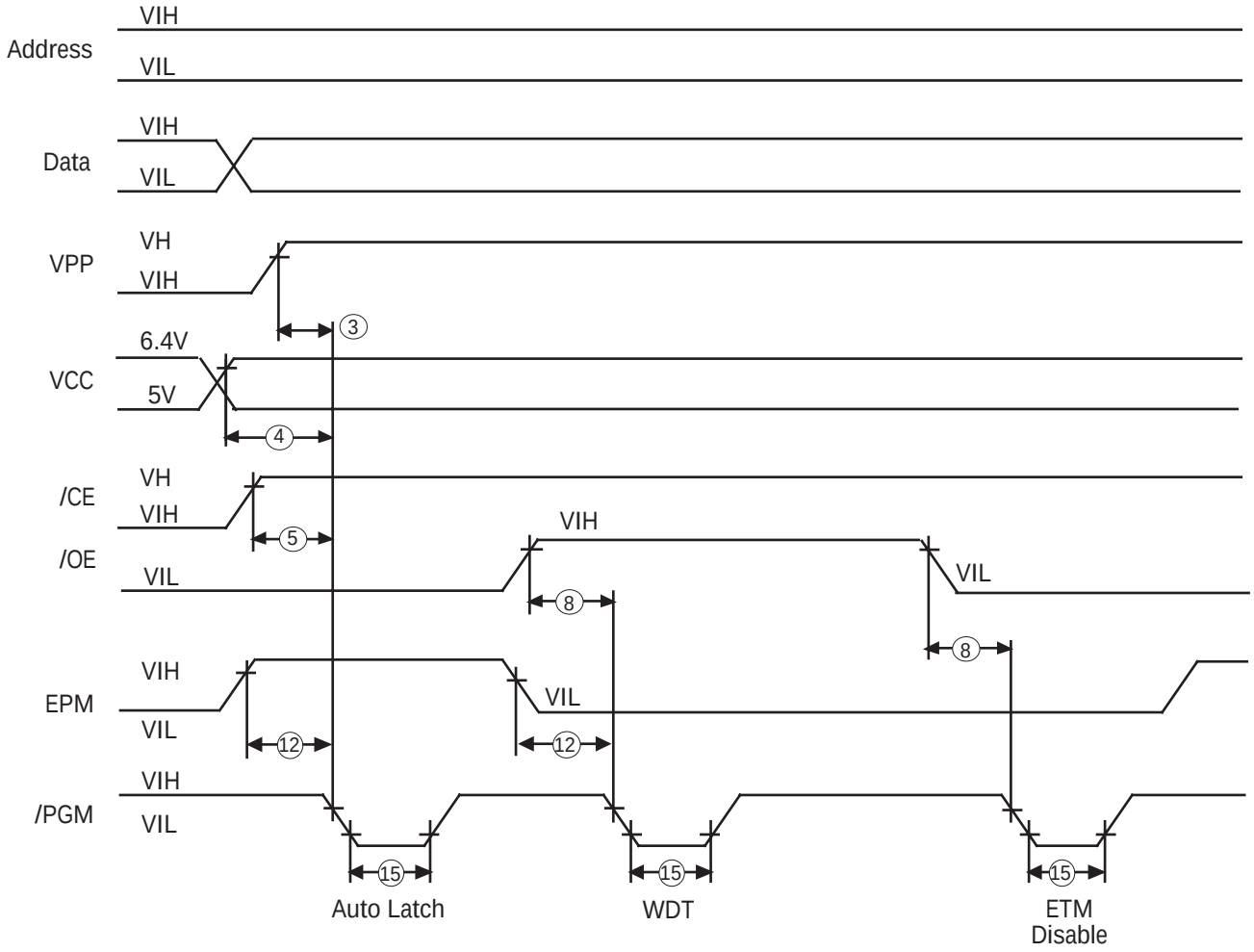


Figure 21. Z86E02 Programming Waveform (Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

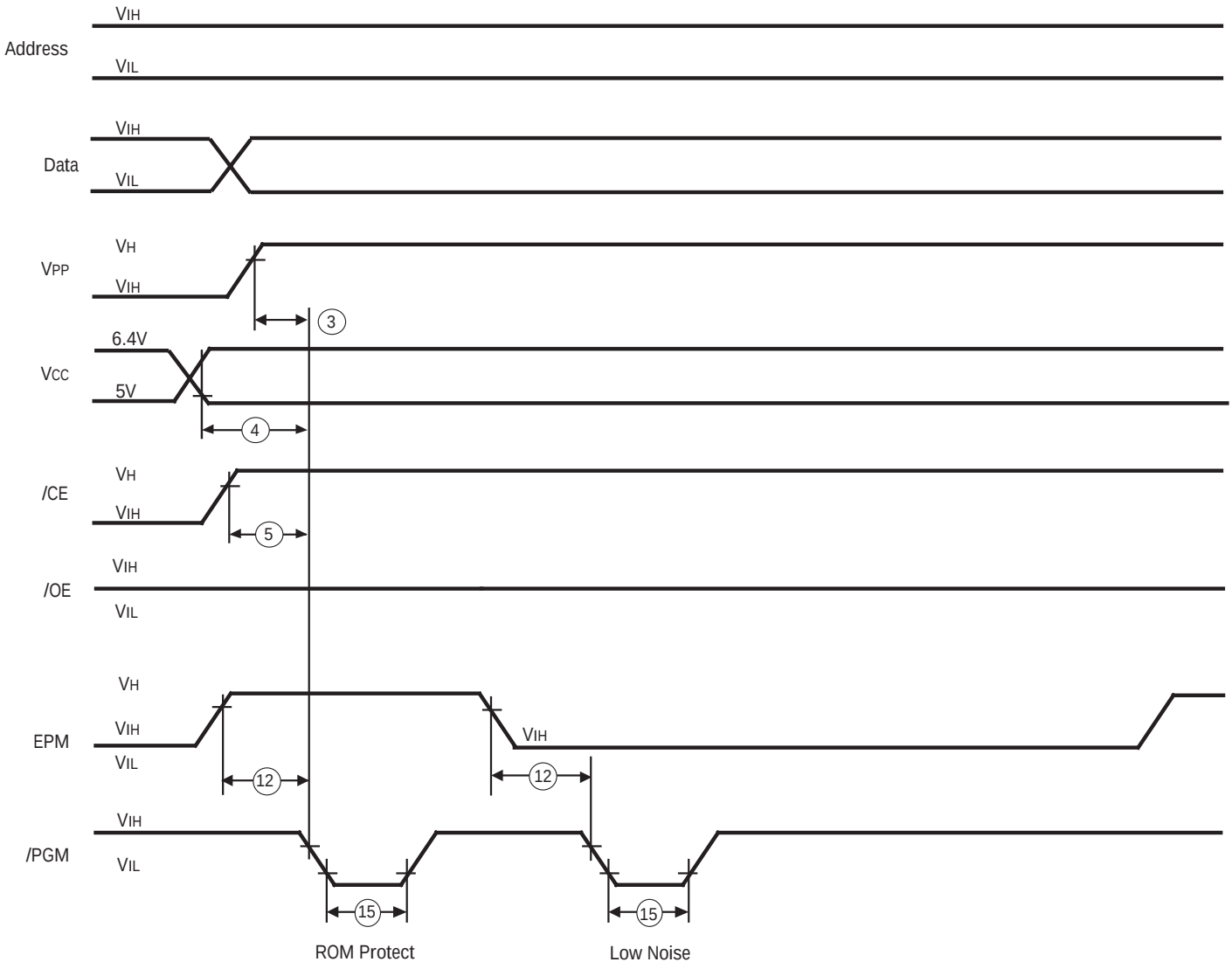


Figure 22. Z86E02 Programming Options Waveform (ROM Protect and Low Noise Program)

FUNCTIONAL DESCRIPTION (Continued)

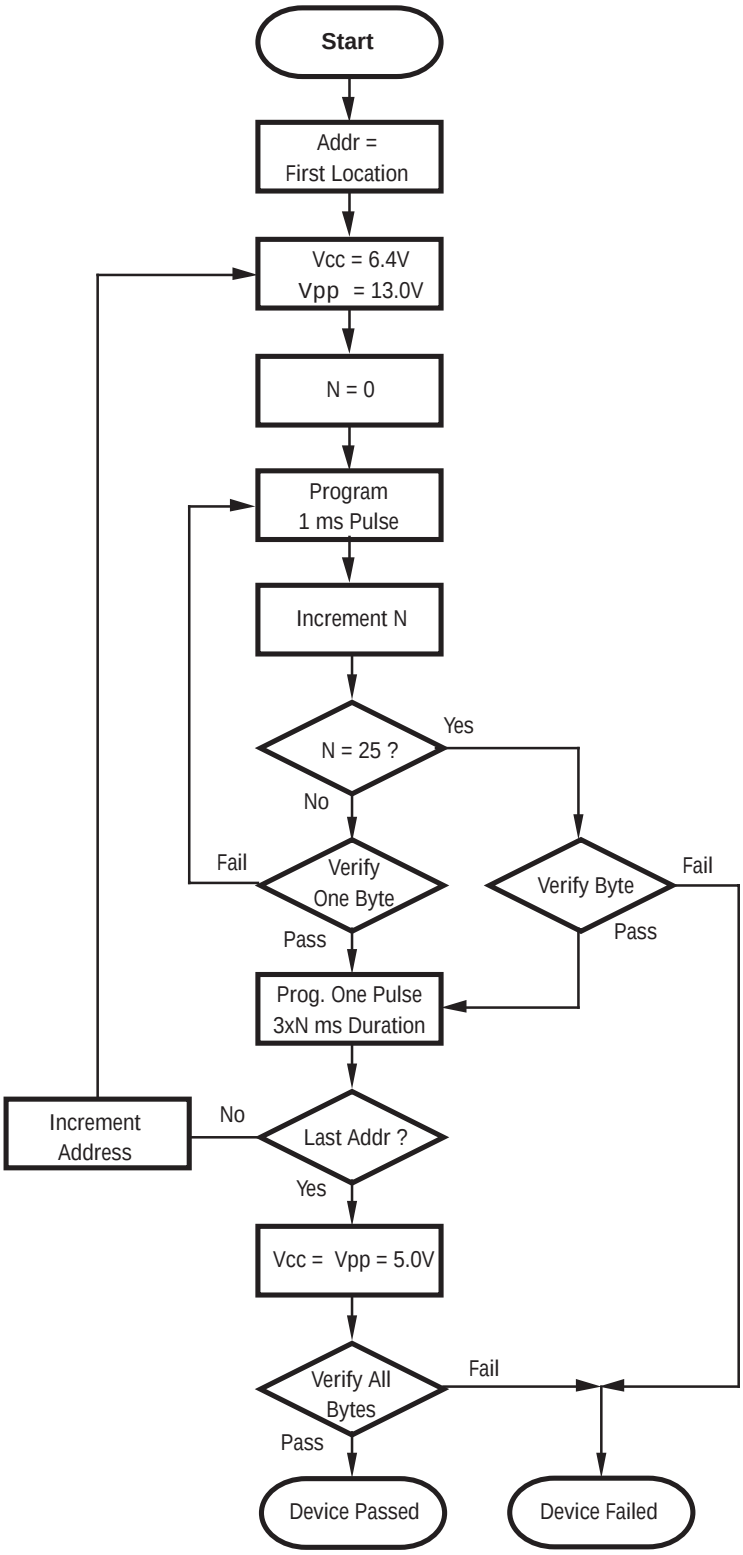


Figure 24. Z86E02 Programming Algorithm

Z8 CONTROL REGISTERS

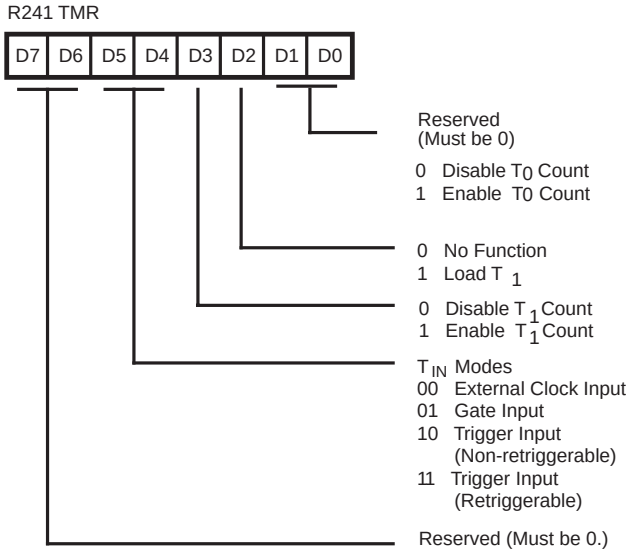


Figure 25. Timer Mode Register ($F1_H$: Read/Write)

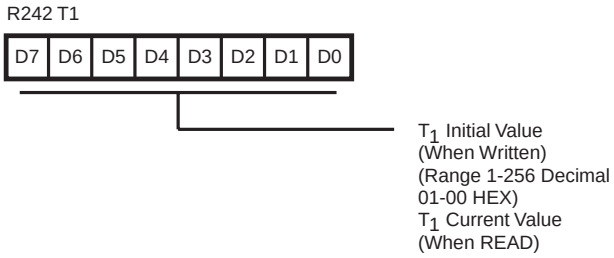


Figure 26. Counter Timer 1 Register ($f2_H$:Read/Write)

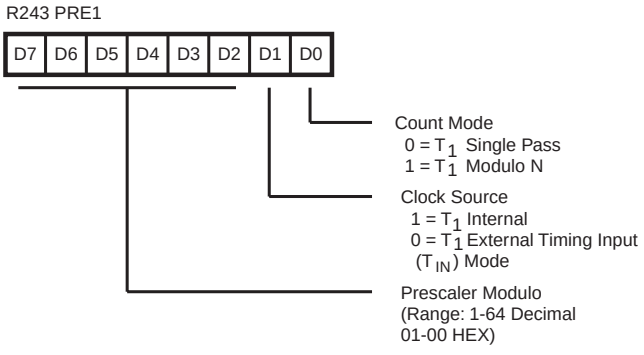


Figure 27. Prescaler! Register ($F3_H$: Write Only)

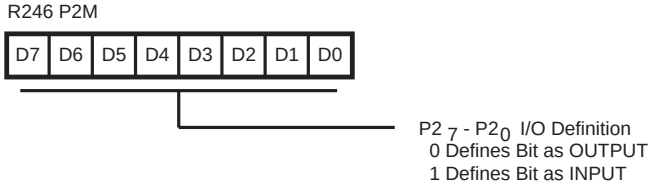


Figure 28. Port 2 Mode Register ($F6_H$: Write Only)

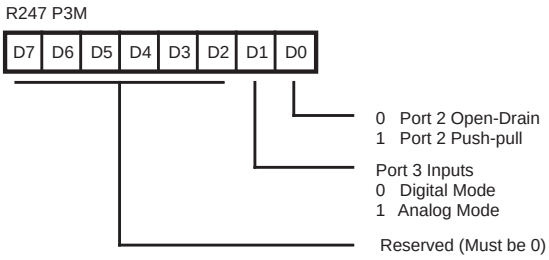


Figure 29. Port 3 Mode Register ($F7_H$: Write Only)

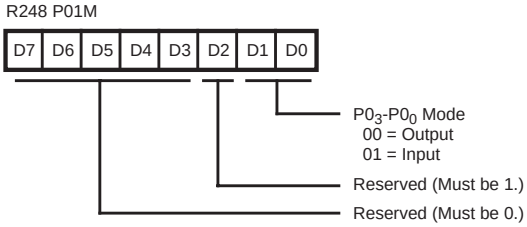


Figure 30. Port 0 and 1 Mode Register ($F8_H$: Write Only)

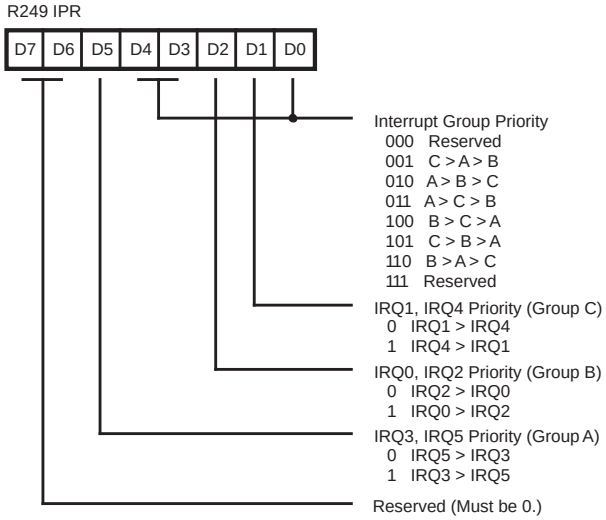


Figure 31. Interrupt Priority Register ($F9_H$: Write Only)

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com