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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	32-SDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08sv16cbm

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	4/2/2009	Initial public release.
2	7/20/2009	Updated Section 5.13, “EMC Performance.” Corrected Table 1. Corrected default trim value to 31.25 kHz.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08SV16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08SV16 series MCU.

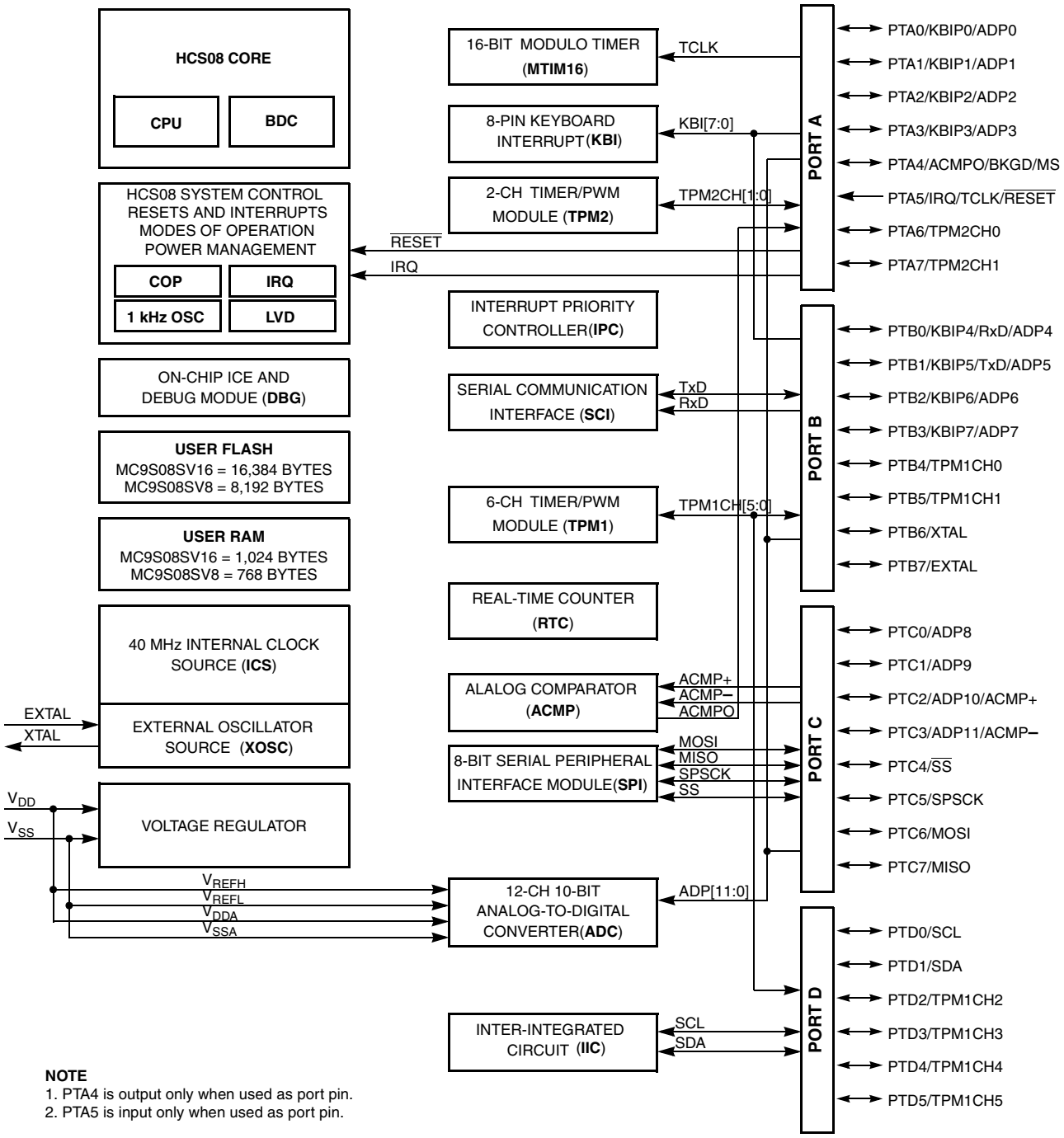


Figure 1. MC9S08SV16 Series Block Diagram

2 System Clock Distribution

MC9S08SV16 series use ICS module as clock sources. The ICS module can use internal or external clock source as reference to provide up to 40 MHz CPU clock. The output of ICS module includes,

- OSCOUT— XOSC output provides EXTAL reference clock to ADC and RTC.
- ICSIRCLK — ICS internal clock reference provides clock source of RTC.
- ICSFFCLK — ICS fixed frequency clock reference (around 32.768 kHz) provides double of the fixed lock signal to TPMs and MTIM16.
- ICSOUT — ICS CPU clock provides double of bus clock which is basic clock reference of peripherals.
- ICSLCLK — Alternate BDC clock provides debug signal to BDC module.

The TCLK pin is an extra external clock source. When TCLK is enabled, it can provide alternate clock source to TPMs and MTIM16. The on-chip 1 kHz clock can provide clock source of RTC and COP modules.

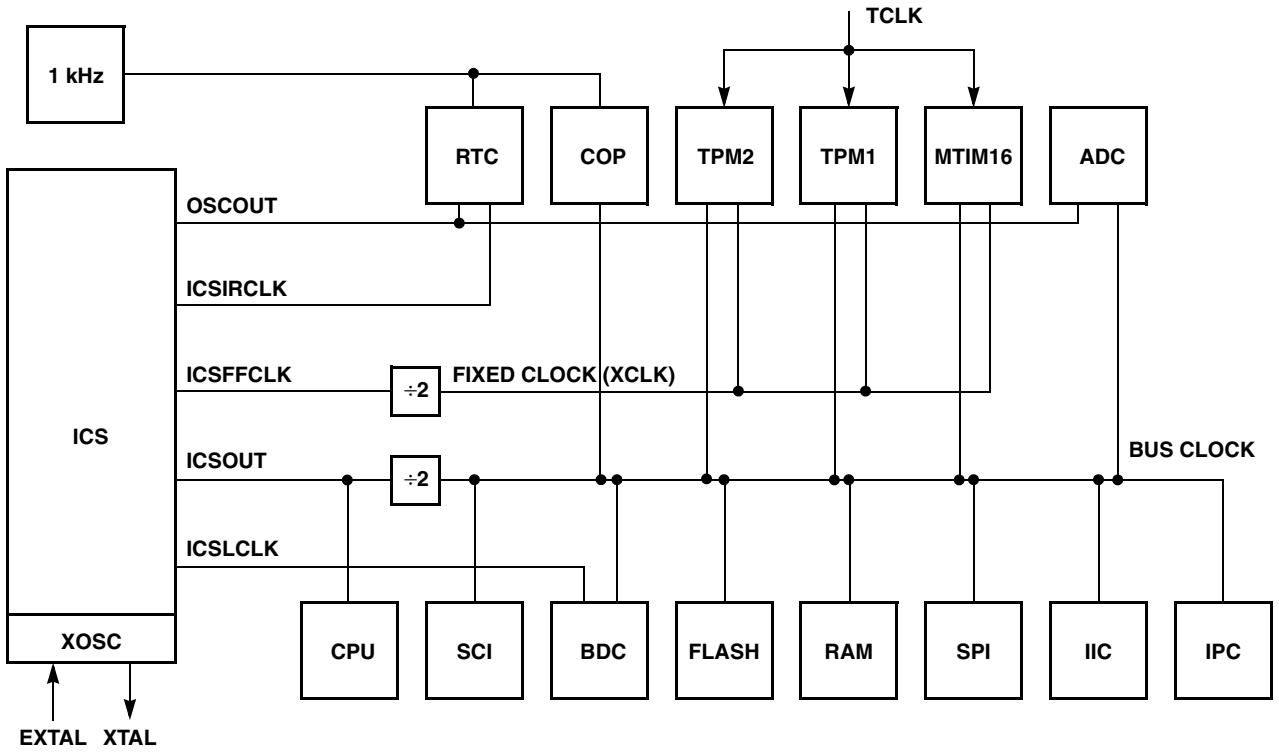


Figure 2. System Clock Distribution Diagram

3 Pin Assignments

This section shows the pin assignments for the MC9S08SV16 series devices.

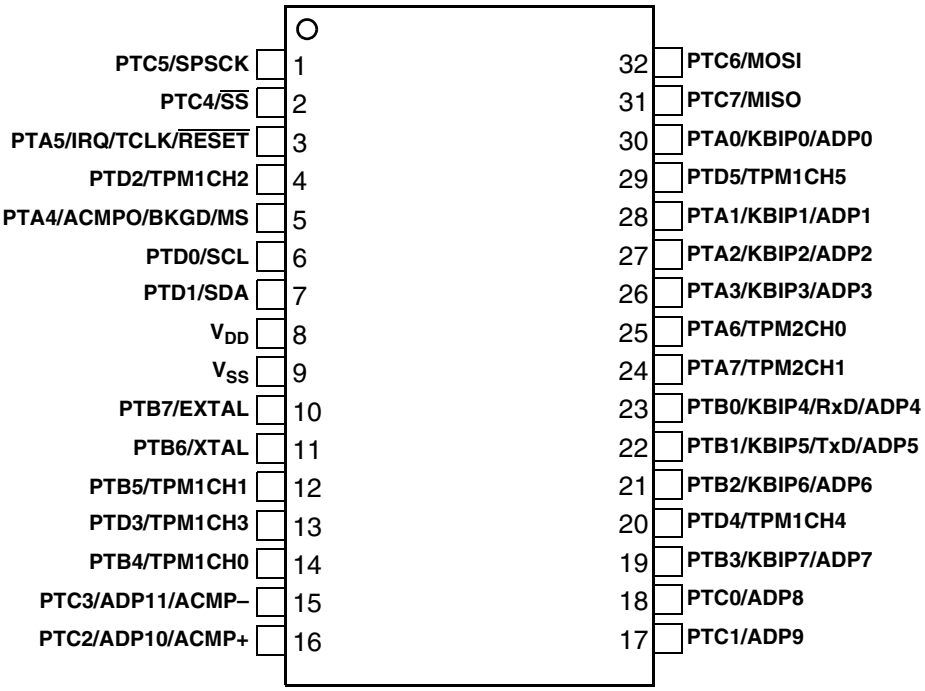


Figure 3. MC9S08SV16 Series 32-Pin SDIP Package

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

5.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
32-pin SDIP	θ_{JA}	60	°C/W
32-pin LQFP		85	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	35	°C/W
32-pin LQFP		56	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

5.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
1	—	Operating voltage		—	—	2.7	—	5.5	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 2.7 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 4.1 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 2.7 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 2.7 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 4.1 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	All digital inputs	V_{IH}	V_{DD} > 4.1 V	0.70 × V_{DD}	—	—	V
	C				V_{DD} > 2.7 V	0.85 × V_{DD}	—	—	
7	P	Input low voltage	All digital inputs	V_{IL}	V_{DD} > 4.1 V	—	—	0.35 × V_{DD}	
	C				V_{DD} > 2.7 V	—	—	0.30 × V_{DD}	
8	C	Input hysteresis	All digital inputs	V_{hys}	—	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current	All input only pins (per pin)	$\|I_{In}\|$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$\|I_{OZ}\|$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA

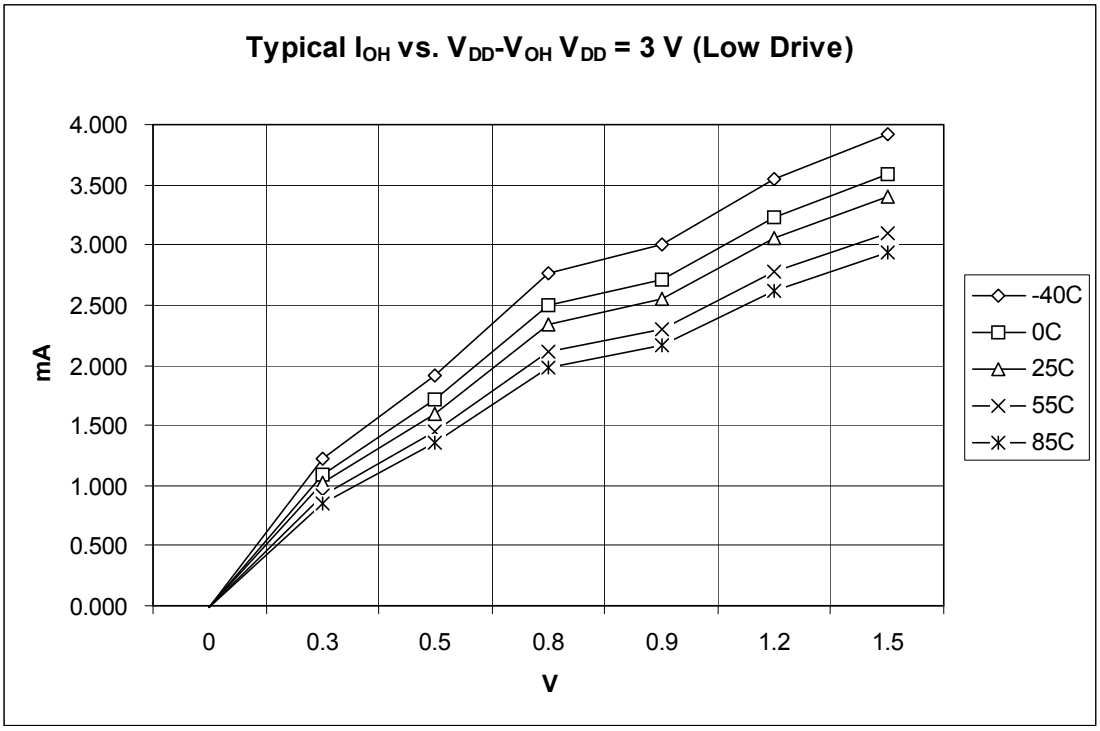


Figure 11. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 3.0 V) (Low Drive)

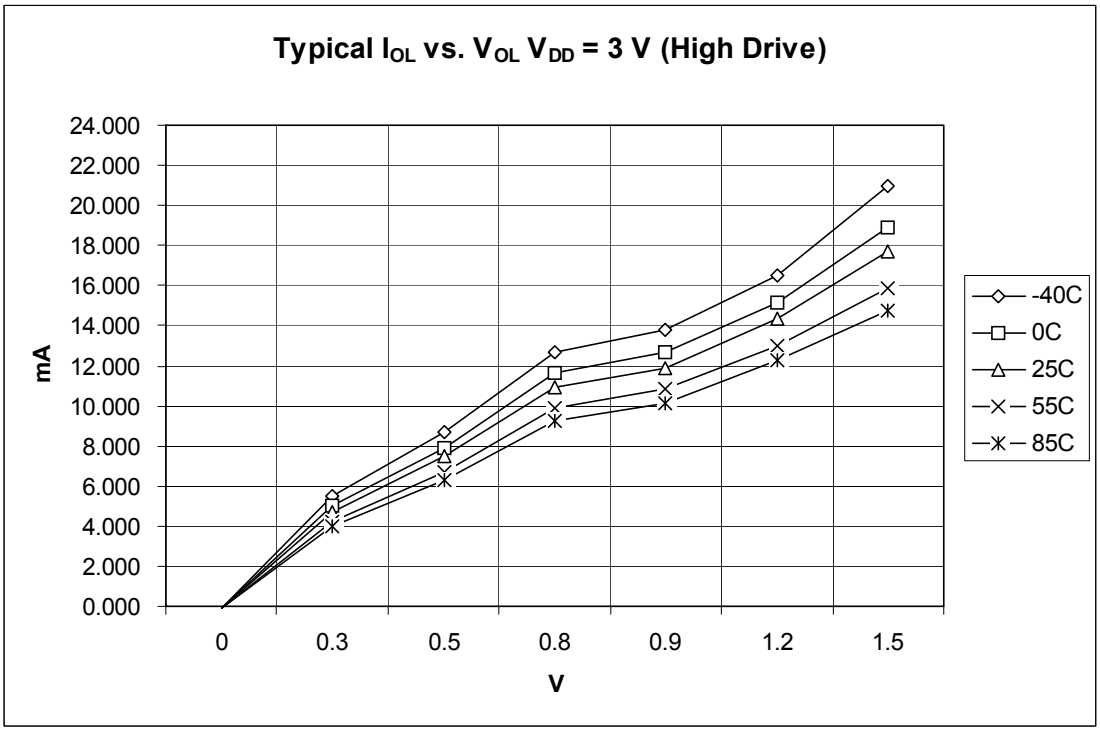


Figure 12. Typical I_{OL} Vs. V_{OL} (V_{DD} = 3.0 V) (High Drive)

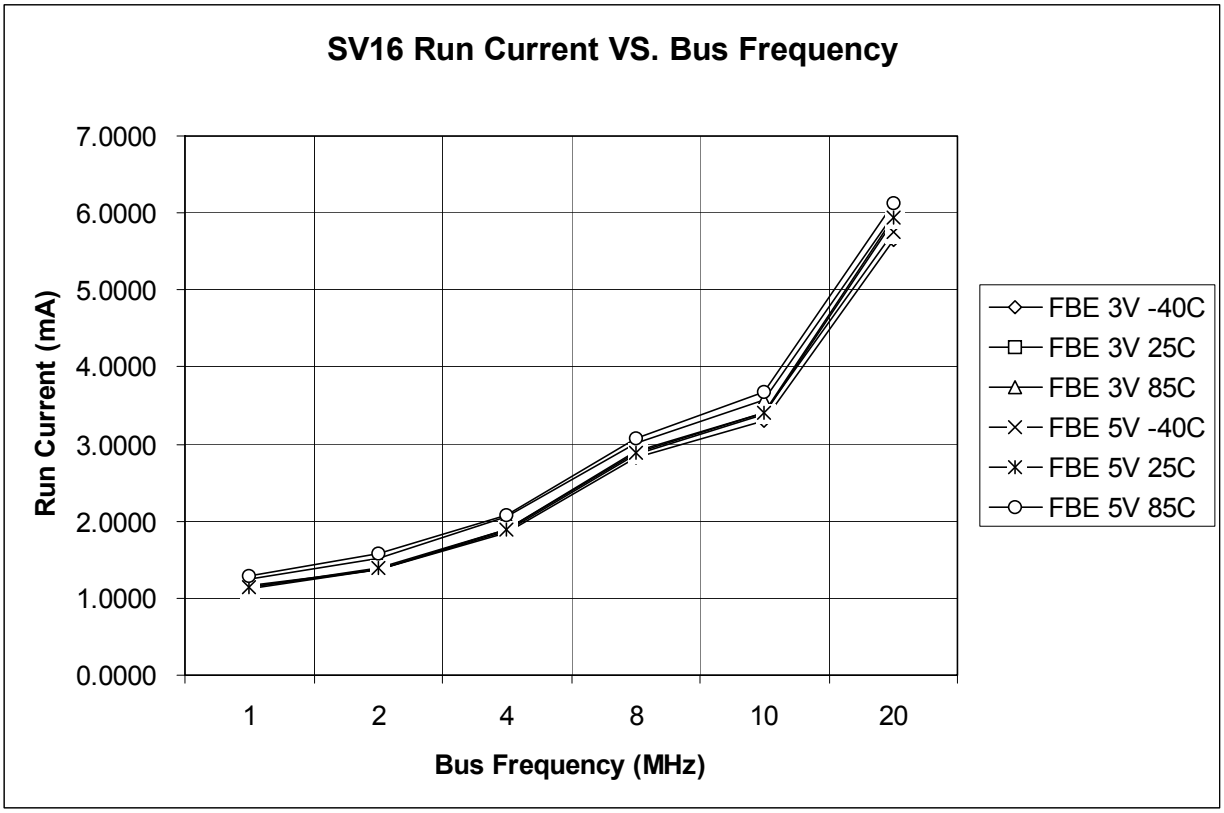


Figure 14. Typical Run I_{DD} for FBE (All Modules Off)

5.8 External Oscillator (XOSC) and ICS Characteristics

Refer to Figure 16 for crystal or resonator circuits.

Table 9. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1), high gain (HGO = 1), FBELP mode High range (RANGE = 1), low power (HGO = 0), FBELP mode	 f_{lo} f_{hi} f_{hi} f_{hi}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See Note [3]			
3	D	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F	—	 10 1	—	 MΩ MΩ
4	D	Series resistor — Low range Low gain (HGO = 0) High gain (HGO = 1)	R_S	—	 0 100	—	kΩ
5	D	Series resistor — High range Low gain (HGO = 0) High gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	—	 0 0 0	 0 10 20	kΩ
6	C	Crystal start-up time [4, 5] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH}	 —	 200 400 5 15	 —	ms
7	T	Internal reference start-up time	t_{IRST}	—	60	100	µs
8	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	0.03125 0	—	5 40	MHz MHz
9	P	Average internal reference frequency — trimmed	f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range — trimmed — Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P	Middle range (DRS = 10)		32	—	40	
11	C	Total deviation of DCO output from trimmed frequency[4] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	±2 ±1	$\%f_{dco}$
12	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	1	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

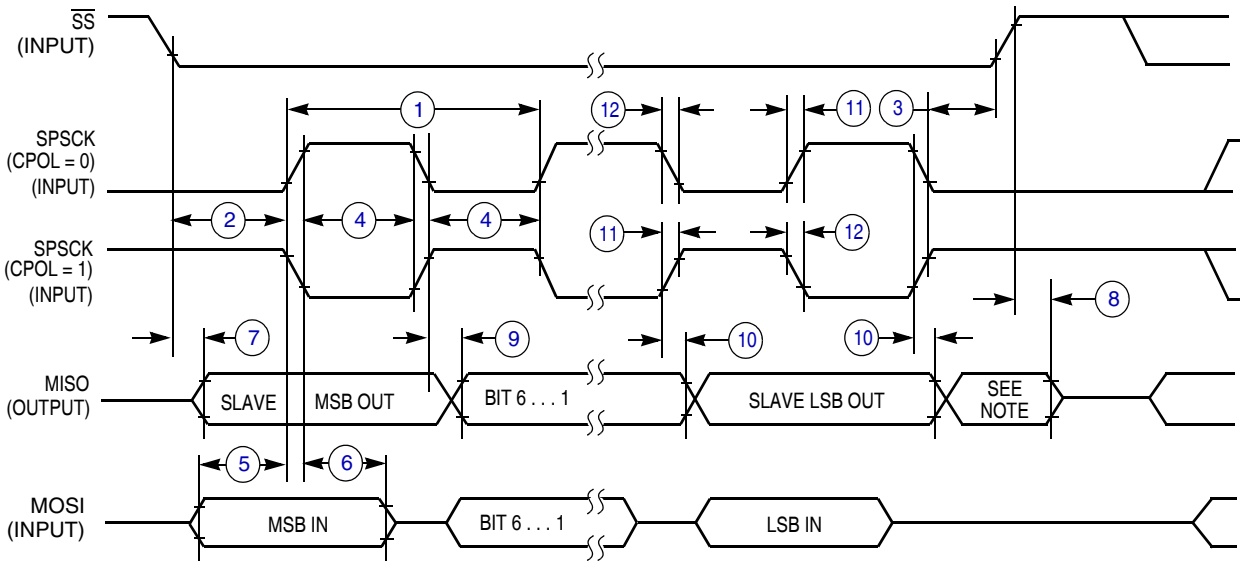
[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

5.9.3 SPI Timing

Table 12 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 12. SPI Timing

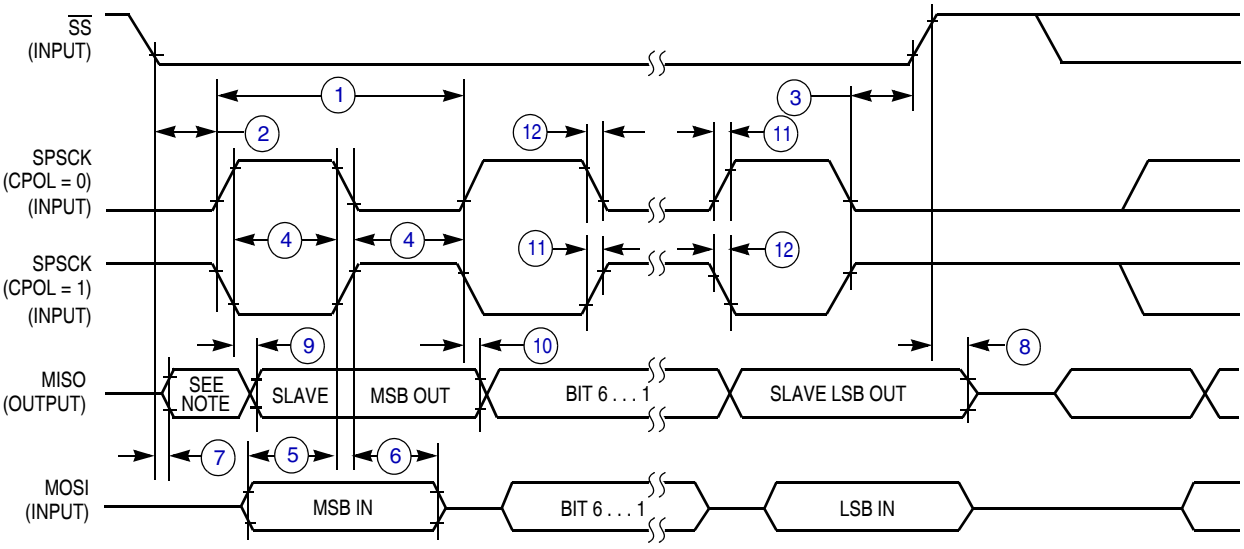
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTE:

1. Not defined but normally MSB of character just received

Figure 23. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

5.10 Analog Comparator (ACMP) Electricals

Table 13. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	2.7	—	5.5	V
P	Supply current (active)	I_{DDAC}	—	20	35	µA

Table 13. Analog Comparator Electrical Specifications (continued)

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

5.11 ADC Characteristics

Table 14. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	— —	— —	5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

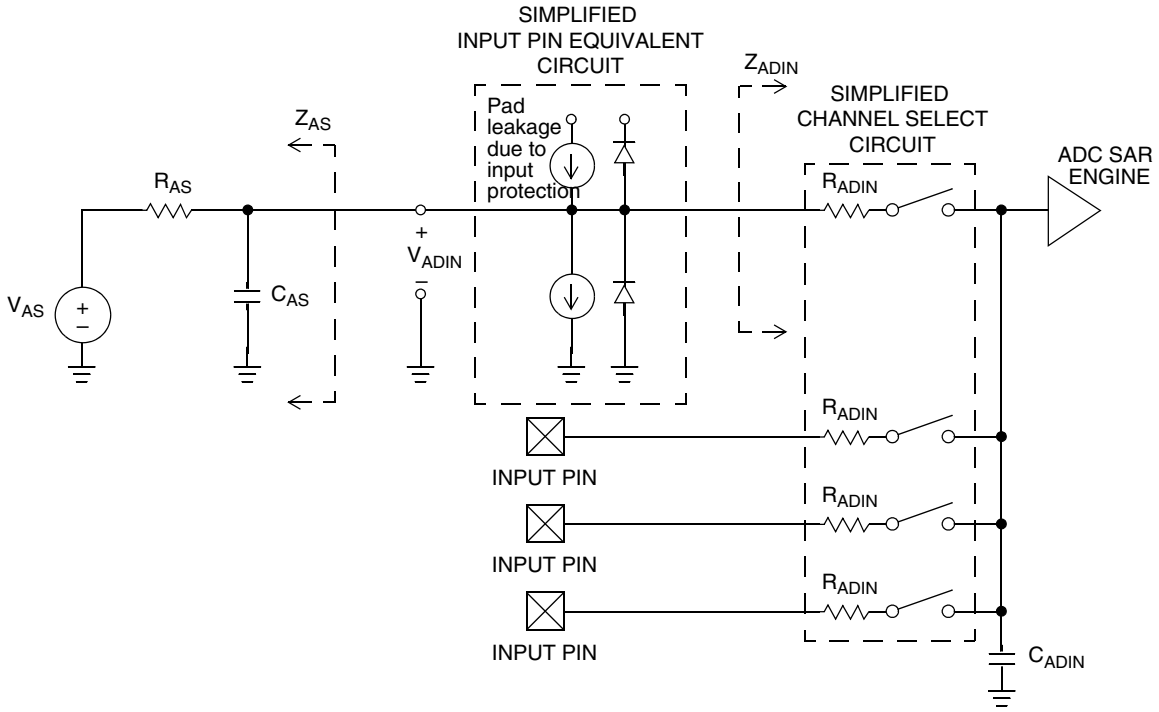


Figure 25. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	µA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDA}	—	218	—	µA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	µA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	3.266	—	mV/°C	
		25 °C– 85 °C		—	3.638	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	
P	Total unadjusted error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
P		8-bit mode		—	±0.7	±1.5		
P	Differential non-linearity	10-bit mode[3]	DNL	—	±0.5	±1.0	LSB[2]	
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
T		8-bit mode		—	±0.3	±0.5		
P	Zero-scale error	10-bit mode	E_{ZS}	—	±1.5	±2.1	LSB[2]	V_{ADIN} = V_{SSA}
P		8-bit mode		—	±0.5	±0.7		
T	Full-scale error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	V_{ADIN} = V_{DDA}
T		8-bit mode		—	±0.5	±0.5		
D	Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input leakage error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[4] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

5.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 16. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
C	Byte program current[3]	RI_{DDBP}	—	4	—	mA
C	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

5.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (the North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 17. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = 25 °C package type 32-pin LQFP	0.15 – 50 MHz	4 MHz crystal 19 MHz bus	9	dBμV
			50 – 150 MHz		5	
			150 – 500 MHz		2	
			500 – 1000 MHz		1	
			IEC Level		N	—
			SAE Level		1	—

1 Data based on qualification test results.

6 Ordering Information

This section contains ordering information for MC9S08SV16 series devices. See below for an example of the device numbering system.

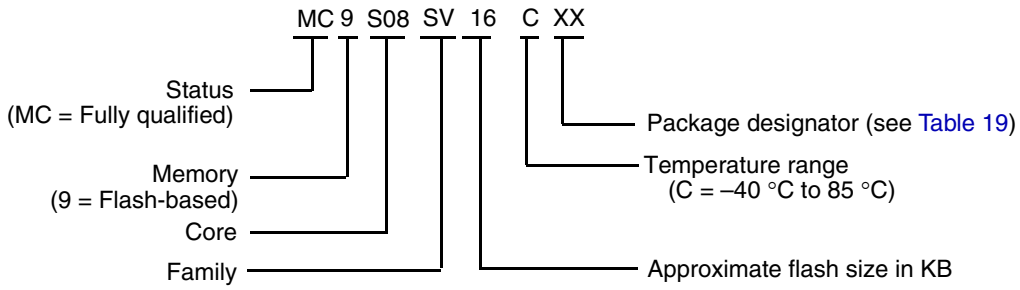
Table 18. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	FLASH	RAM	
MC9S08SV16	16 KB	1024 Byte	32-pin SDIP 32-pin LQFP
MC9S08SV8	8 KB	768 Byte	

1 See the reference manual, *MC9S08SV16 Series Reference Manual*, for a complete description of modules included on each device.

2 See Table 19 for package information.

Example of the device numbering system:



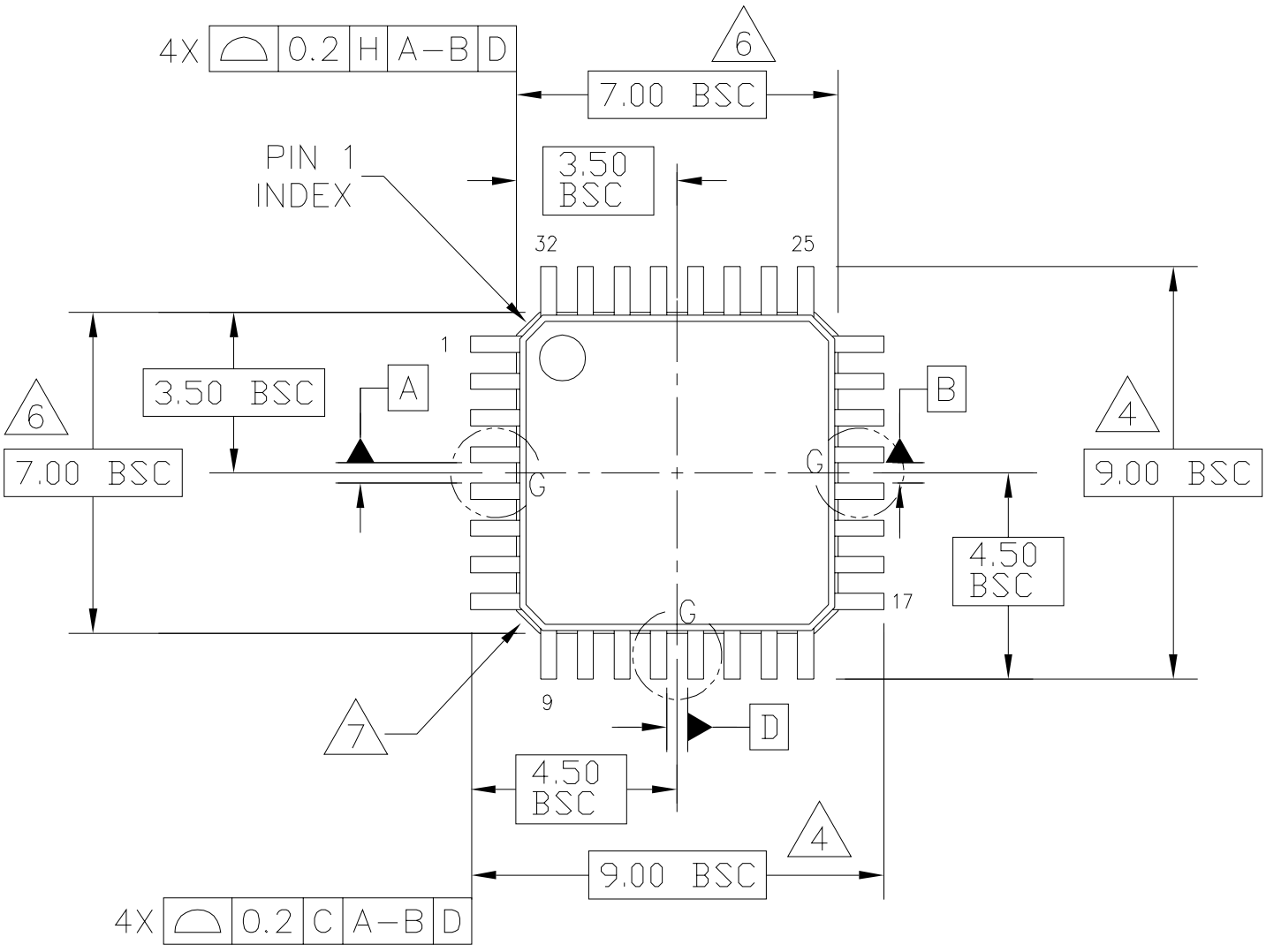
7 Package Information

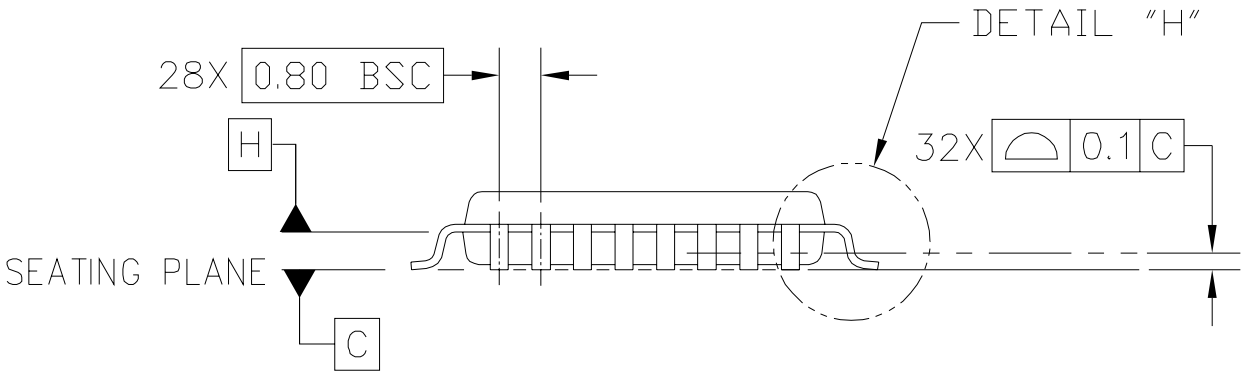
Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
32	Low Quad Flat Package	LQFP	LC	873A-03	98ASH70029A
32	Shrink Dual In-line Package	SDIP	BM	1376-02	98ASA99330D

7.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19.





MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70029A	REV: D
LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70029A	REV: D
LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

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