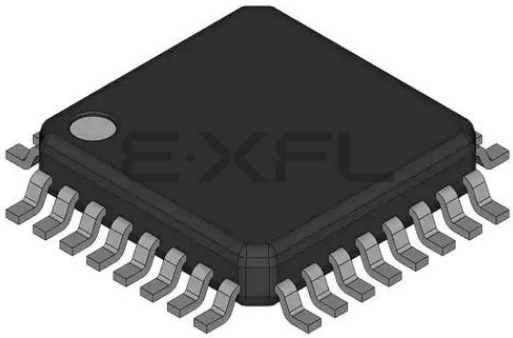


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08sv8clc

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	4/2/2009	Initial public release.
2	7/20/2009	Updated Section 5.13, “EMC Performance.” Corrected Table 1. Corrected default trim value to 31.25 kHz.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08SV16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08SV16 series MCU.

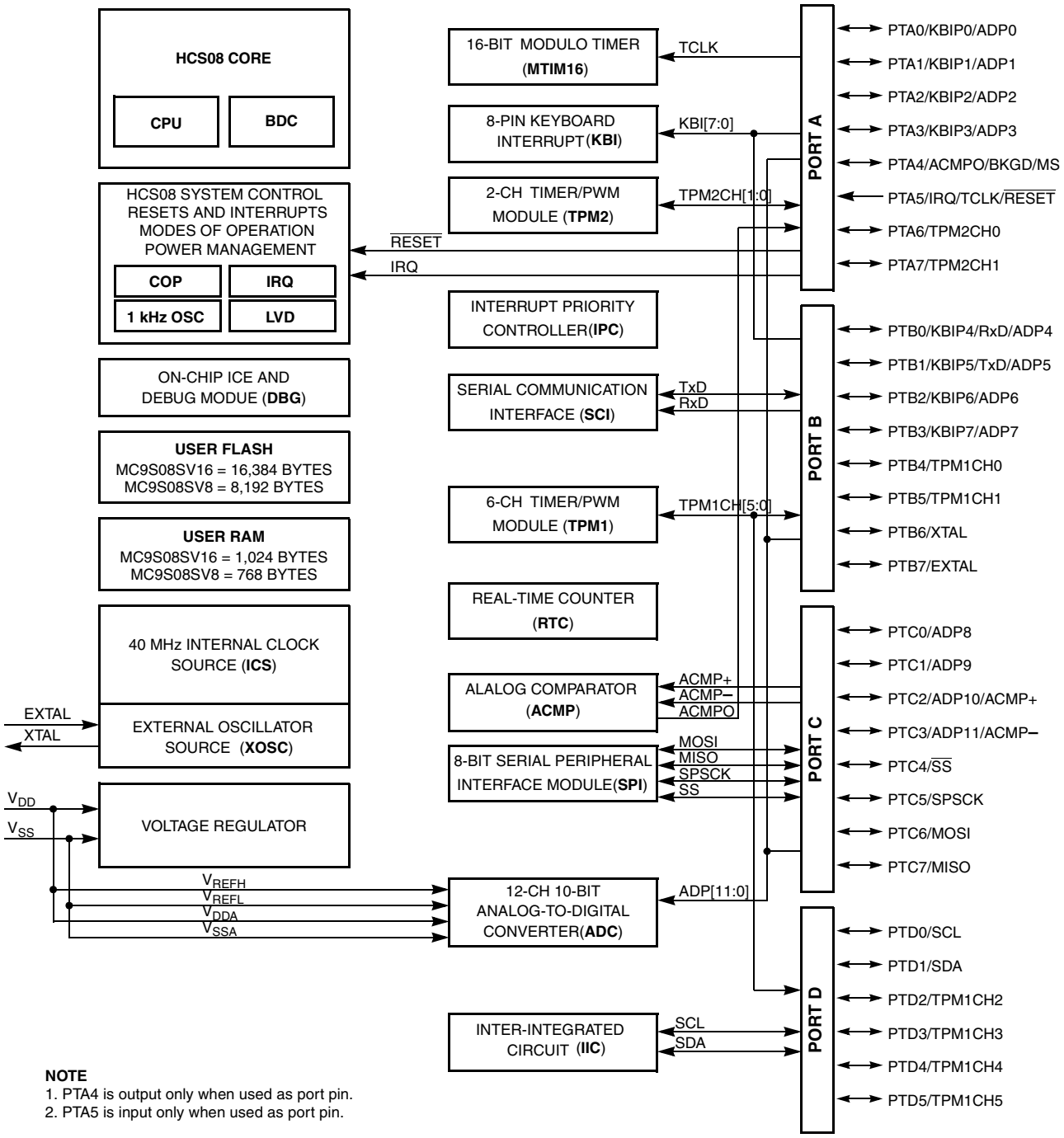


Figure 1. MC9S08SV16 Series Block Diagram

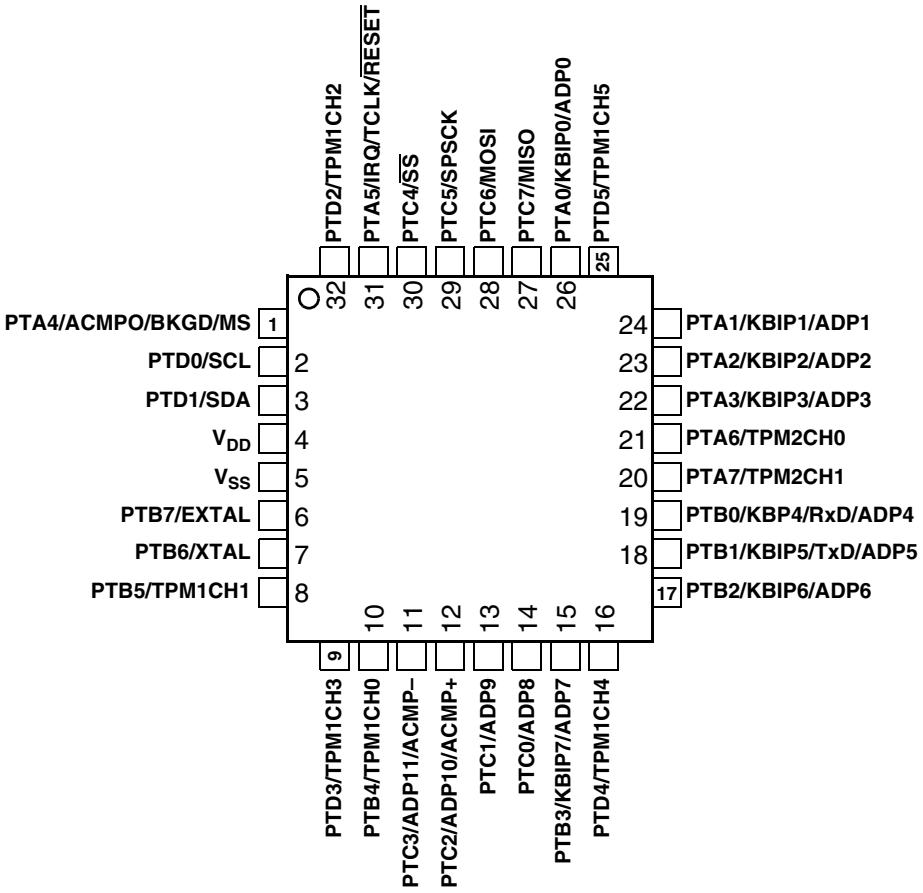


Figure 4. MC9S08SV16 Series 32-Pin LQFP Package

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
1	29	PTC5	I/O	SPSCK	I/O				
2	30	PTC4	I/O	$\overline{SS}$	I/O				
3	31	PTA5	I	IRQ	I	TCLK	I	$\overline{RESET}$	I
4	32	PTD2	I/O			TPM1CH2	I/O		
5	1	PTA4	O	ACMPO	O	BKGD	I	MS	I
6	2	PTD0	I/O	SCL	I/O				
7	3	PTD1	I/O	SDA	I/O				
8	4							V_{DD}	I
9	5							V_{SS}	I
10	6	PTB7	I/O	EXTAL	I				
11	7	PTB6	I/O	XTAL	O				
12	8	PTB5	I/O			TPM1CH1	I/O		
13	9	PTD3	I/O			TPM1CH3	I/O		
14	10	PTB4	I/O			TPM1CH0	I/O		

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
15	11	PTC3	I/O			ADP11	I	ACMP–	I
16	12	PTC2	I/O			ADP10	I	ACMP+	I
17	13	PTC1	I/O			ADP9	I		
18	14	PTC0	I/O			ADP8	I		
19	15	PTB3	I/O	KBIP7	I	ADP7	I		
20	16	PTD4	I/O			TPM1CH4	I/O		
21	17	PTB2	I/O	KBIP6	I	ADP6	I		
22	18	PTB1	I/O	KBIP5	I	TxD	I/O	ADP5	I
23	19	PTB0	I/O	KBIP4	I	RxD	I	ADP4	I
24	20	PTA7	I/O			TPM2CH1	I/O		
25	21	PTA6	I/O			TPM2CH0	I/O		
26	22	PTA3	I/O	KBIP3	I	ADP3	I		
27	23	PTA2	I/O	KBIP2	I	ADP2	I		
28	24	PTA1	I/O	KBIP1	I	ADP1	I		
29	25	PTD5	I/O			TPM1CH5	I/O		
30	26	PTA0	I/O	KBIP0	I	ADP0	I		
31	27	PTC7	I/O	MISO	I/O				
32	28	PTC6	I/O	MOSI	I/O				

NOTE

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear out any associated flags before interrupts are enabled. Table 1 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

4 Memory Map

Figure 5 shows the memory map for the MC9S08SV16 series. On-chip memory in the MC9S08SV16 series of MCUs consist of RAM, flash program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into two groups:

- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x1800 through 0x187F)

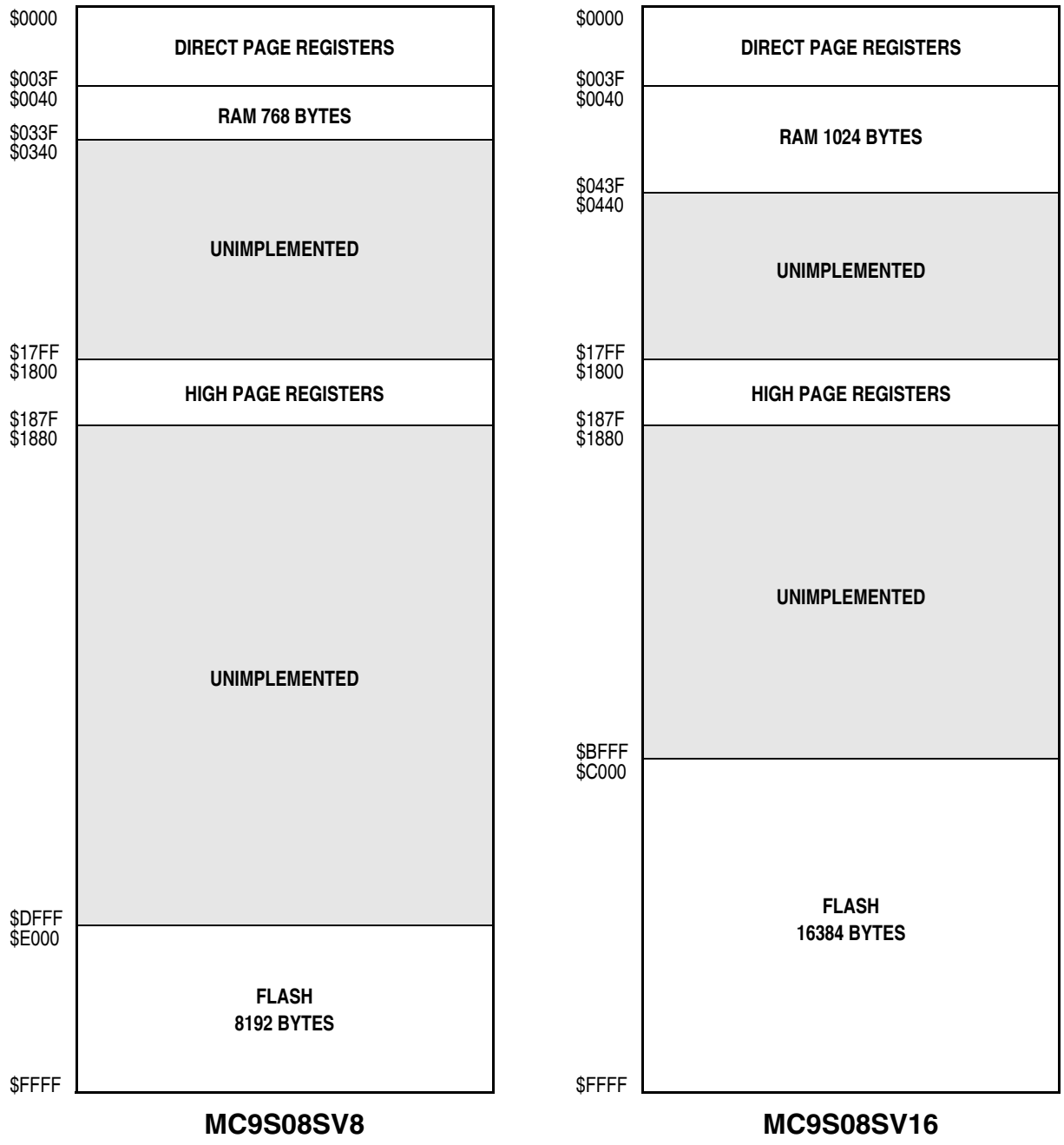


Figure 5. MC9S08SV16 Series Memory Map

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

5.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
32-pin SDIP	θ_{JA}	60	°C/W
32-pin LQFP		85	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	35	°C/W
32-pin LQFP		56	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min.	Typical[1]	Max.	Unit
11a	P	Pullup, pulldown resistors — All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
11b	C	Pullup, pulldown resistors — (PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD} (Note[2])	—	17.5	—	52.5	kΩ
12	C	DC injection current [3, 4, 5] — Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input capacitance, all pins	C_{In}	—	—	—	8	pF
14	C	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V
15	C	POR re-arm voltage[6]	V_{POR}	—	0.9	1.4	2.0	V
16	D	POR re-arm time	t_{POR}	—	10	—	—	µs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	—	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	—	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
18	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	—	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	—	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
19	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	—	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	—	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
21	C	Low-voltage inhibit reset/recover hysteresis	V_{hys}	—	—	80	—	mV
22	C	Bandgap voltage reference[7]	V_{BG}	—	—	1.21	—	V

1 Typical values are measured at 25 °C. Characterized, not tested.

2 The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

3 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

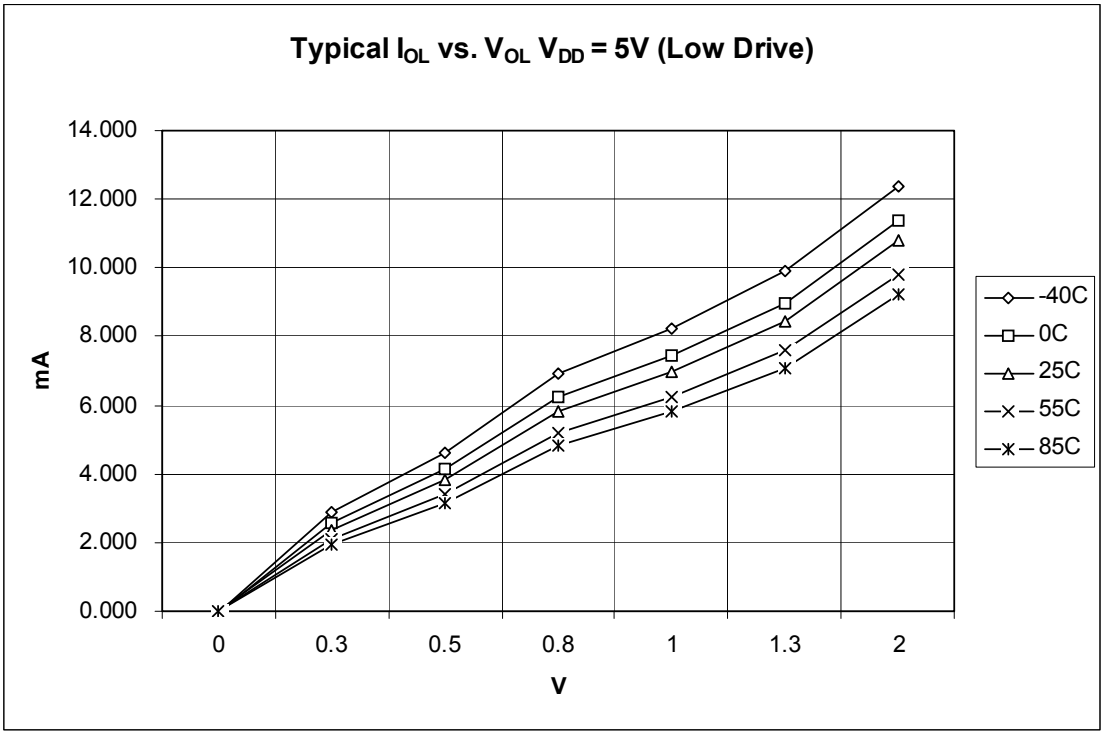


Figure 9. Typical I_{OH} Vs. V_{OL} (V_{DD} = 5.0 V) (Low Drive)

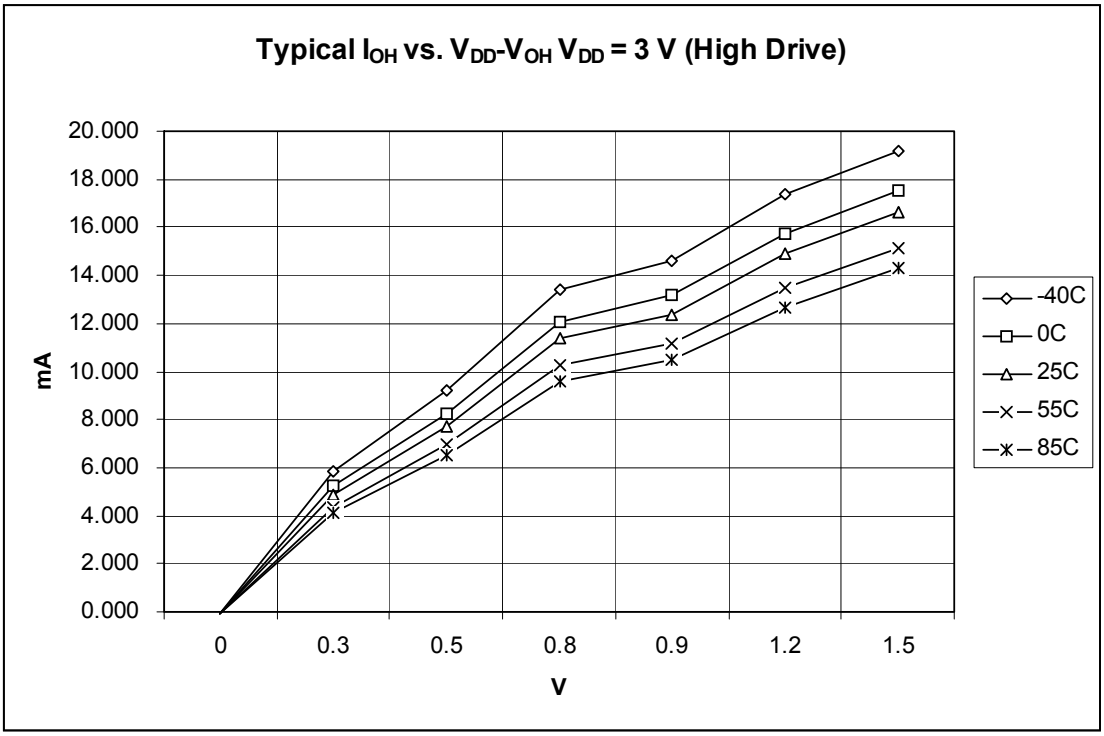


Figure 10. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 3.0 V) (High Drive)

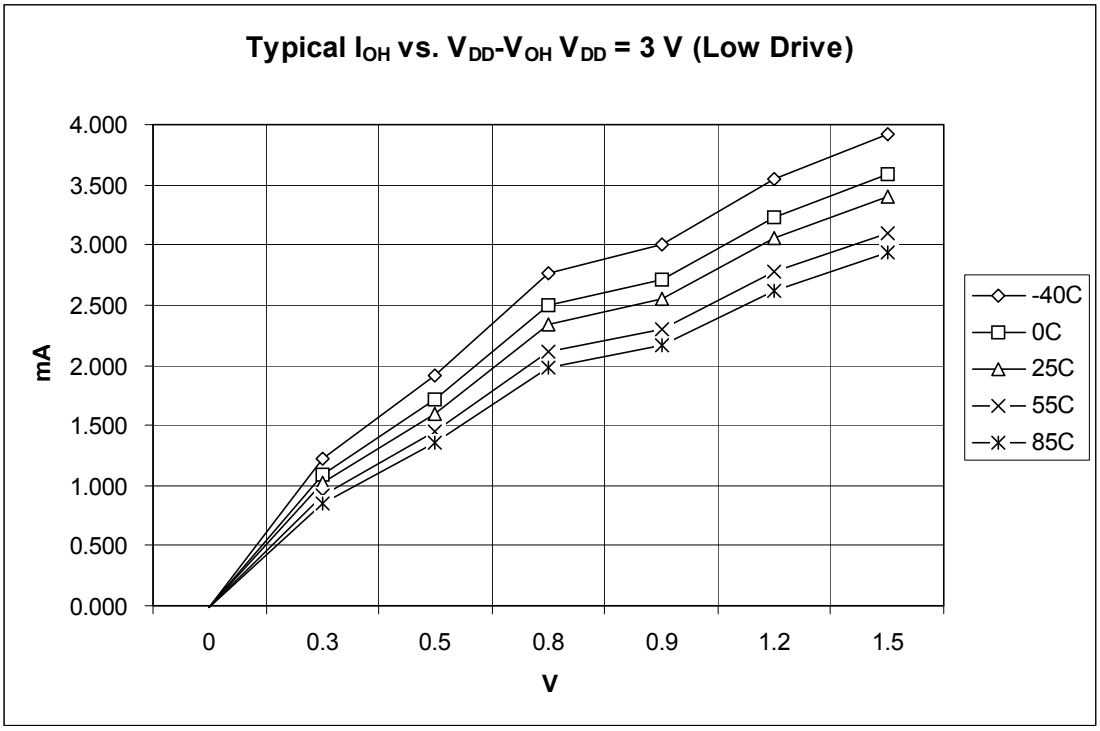


Figure 11. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 3.0 V) (Low Drive)

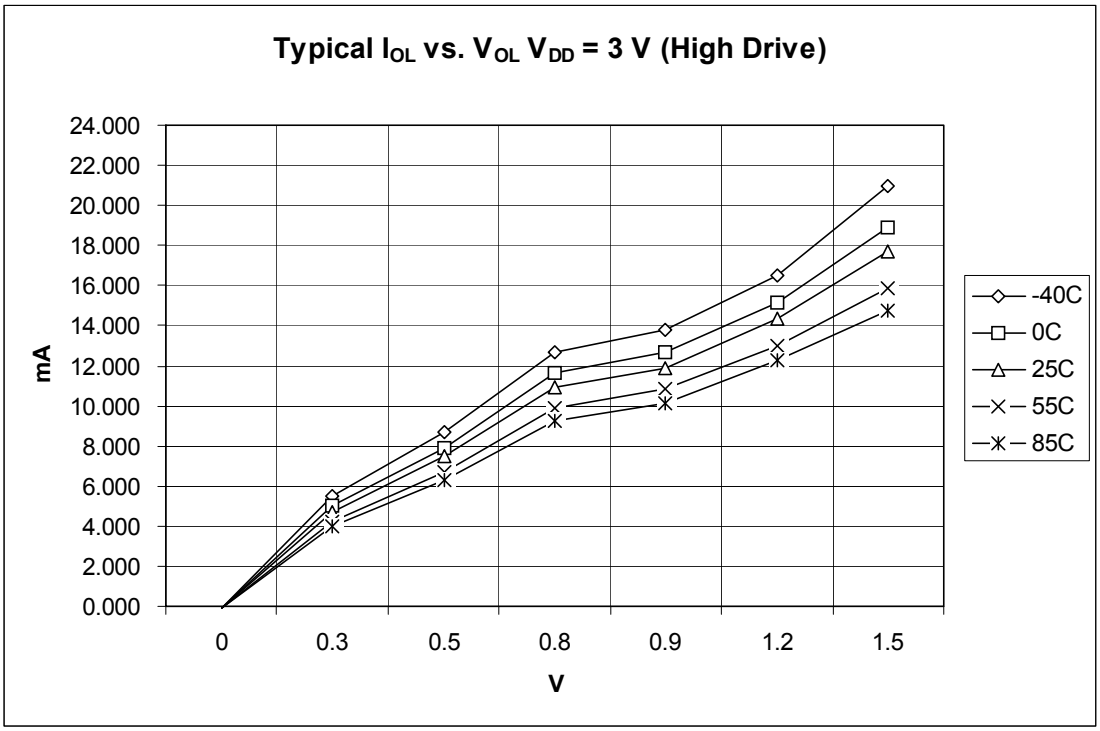


Figure 12. Typical I_{OL} Vs. V_{OL} (V_{DD} = 3.0 V) (High Drive)

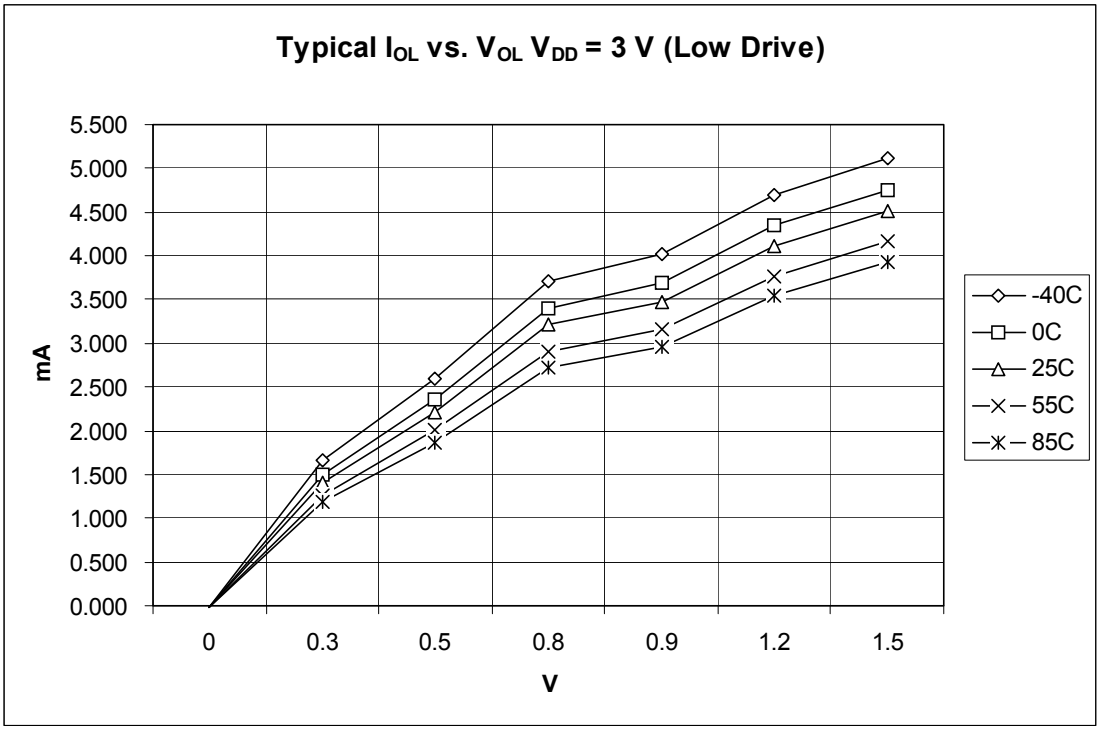


Figure 13. Typical I_{OL} Vs. V_{OL} (V_{DD} = 3.0 V) (Low Drive)

5.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	P	Run supply current FBE mode, all modules on	RI_{DD}	20 MHz	5	10.57	12.96	mA	–40 to 85 °C
	C			8 MHz		5.24	6.48		
	C			1 MHz		2.00	2.60		
2	P	Run supply current FBE mode, all modules on	RI_{DD}	20 MHz	3	8.86	10.86	mA	–40 to 85 °C
	C			8 MHz		4.53	5.61		
	C			1 MHz		1.82	2.31		
3	C	Run supply current FBE mode, all modules off	RI_{DD}	20 MHz	5	5.91	7.25	mA	–40 to 85 °C
	C			8 MHz		2.94	3.69		
	C			1 MHz		1.18	1.54		
4	C	Run supply current FBE mode, all modules off	RI_{DD}	20 MHz	3	5.69	6.98	mA	–40 to 85 °C
	C			8 MHz		2.90	3.60		
	C			1 MHz		1.17	1.49		
5	C	Wait mode current FBE mode, all modules off	WI_{DD}	20 MHz	5	4.83	—	mA	–40 to 85 °C
	C			1 MHz		1.06	—		

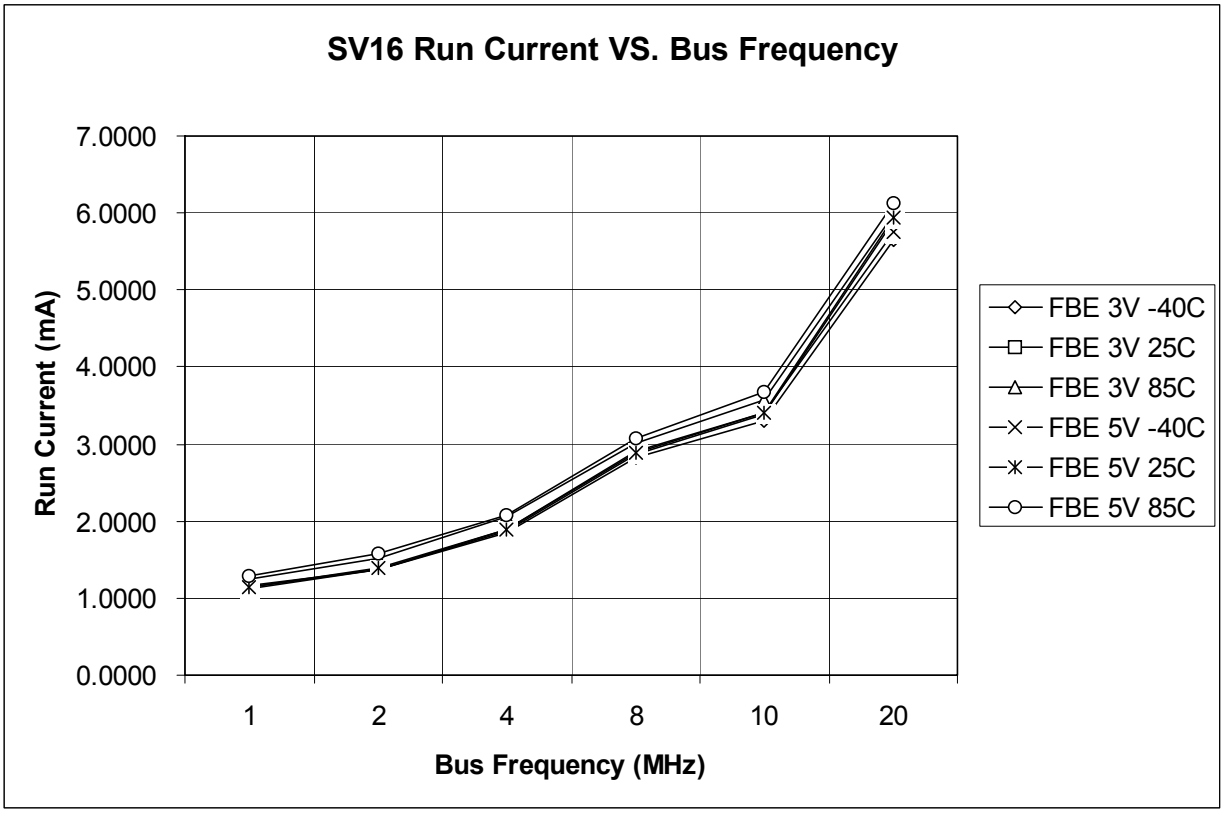


Figure 14. Typical Run I_{DD} for FBE (All Modules Off)

5.8 External Oscillator (XOSC) and ICS Characteristics

Refer to Figure 16 for crystal or resonator circuits.

Table 9. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1), high gain (HGO = 1), FBELP mode High range (RANGE = 1), low power (HGO = 0), FBELP mode	 f_{lo} f_{hi} f_{hi} f_{hi}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See Note [3]			
3	D	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F	—	 10 1	—	 MΩ MΩ
4	D	Series resistor — Low range Low gain (HGO = 0) High gain (HGO = 1)	R_S	—	 0 100	—	kΩ
5	D	Series resistor — High range Low gain (HGO = 0) High gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	—	 0 0 0	 0 10 20	kΩ
6	C	Crystal start-up time [4, 5] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH}	 —	 200 400 5 15	 —	ms
7	T	Internal reference start-up time	t_{IRST}	—	60	100	µs
8	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	0.03125 0	—	5 40	MHz MHz
9	P	Average internal reference frequency — trimmed	f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range — trimmed — Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P	Middle range (DRS = 10)		32	—	40	
11	C	Total deviation of DCO output from trimmed frequency[4] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	±2 ±1	$\%f_{dco}$
12	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	1	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

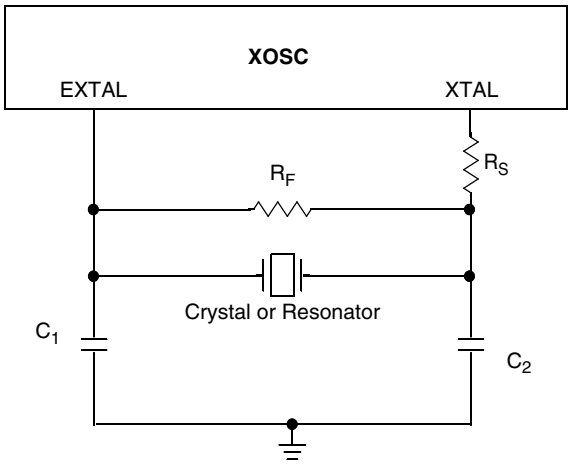


Figure 15. Typical Crystal or Resonator Circuit

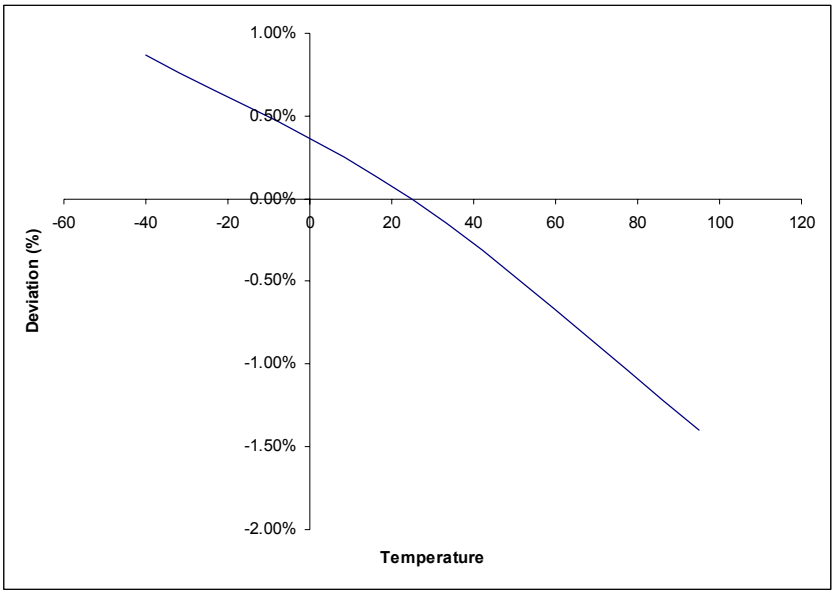


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 5.0 V)

5.9 AC Characteristics

This section describes timing characteristics for each peripheral system.

5.9.1 Control Timing

Table 10. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	16 23	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	5 9	— —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

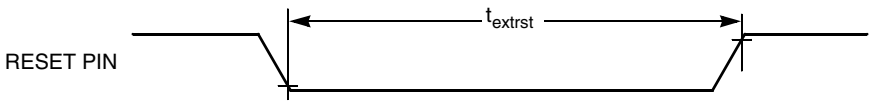


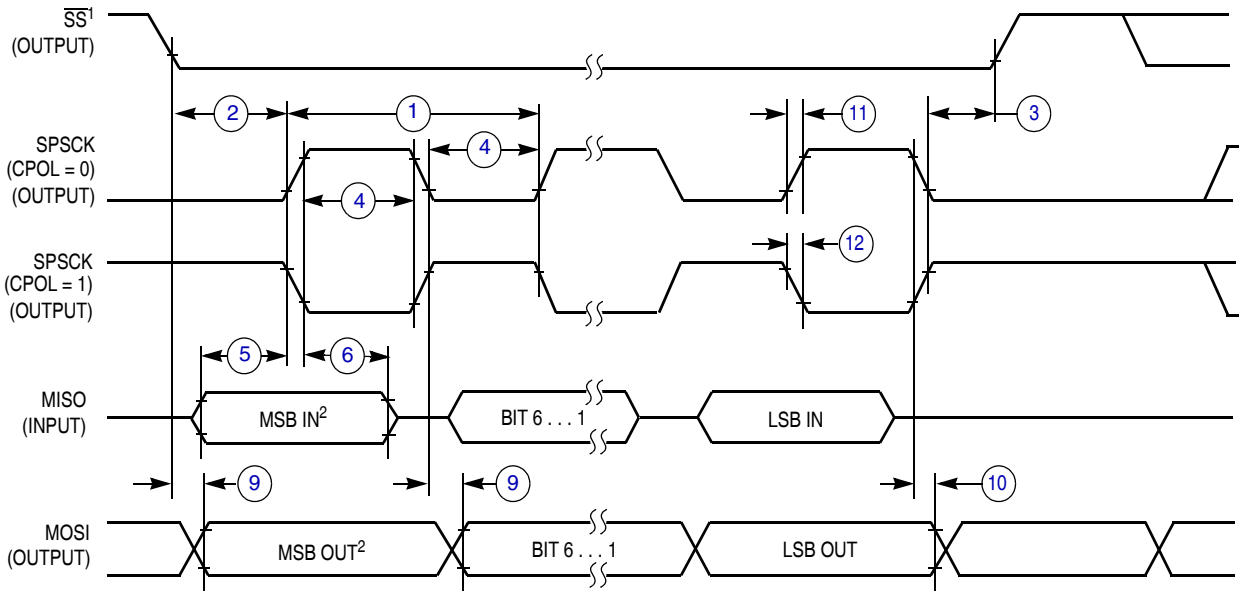
Figure 17. Reset Timing

5.9.3 SPI Timing

Table 12 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 12. SPI Timing

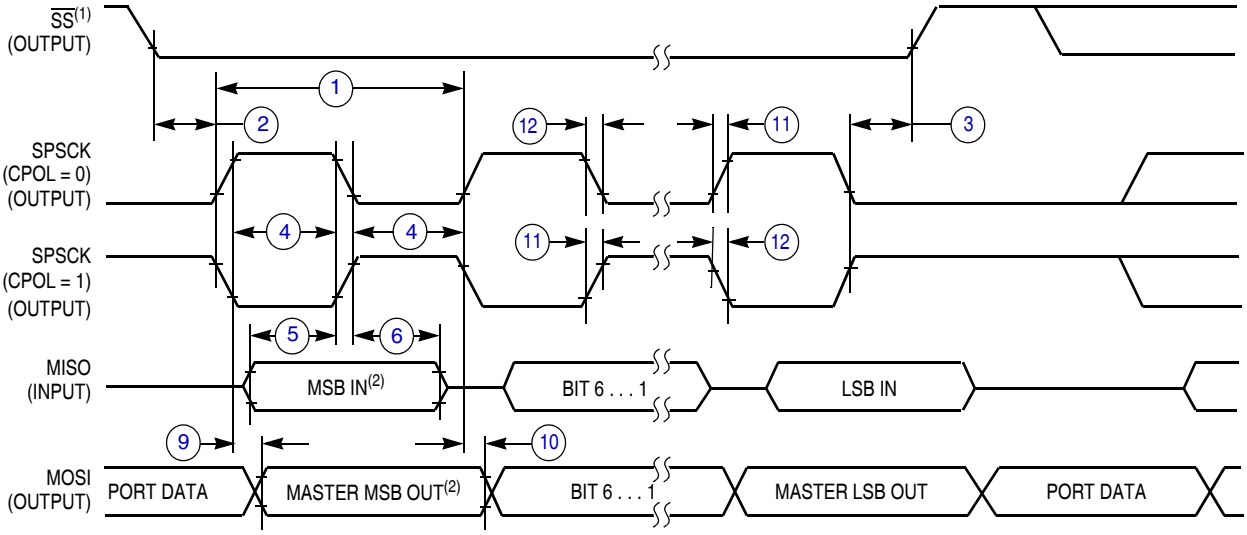
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)

Table 13. Analog Comparator Electrical Specifications (continued)

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

5.11 ADC Characteristics

Table 14. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	— —	— —	5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	3.266	—	mV/°C	
		25 °C– 85 °C		—	3.638	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	
P	Total unadjusted error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
P		8-bit mode		—	±0.7	±1.5		
P	Differential non-linearity	10-bit mode[3]	DNL	—	±0.5	±1.0	LSB[2]	
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
T		8-bit mode		—	±0.3	±0.5		
P	Zero-scale error	10-bit mode	E_{ZS}	—	±1.5	±2.1	LSB[2]	V_{ADIN} = V_{SSA}
P		8-bit mode		—	±0.5	±0.7		
T	Full-scale error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	V_{ADIN} = V_{DDA}
T		8-bit mode		—	±0.5	±0.5		
D	Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input leakage error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[4] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

5.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 17. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.0 V T_A = 25 °C package type 32-pin LQFP	0.15 – 50 MHz	4 MHz crystal 19 MHz bus	9	dBμV
			50 – 150 MHz		5	
			150 – 500 MHz		2	
			500 – 1000 MHz		1	
			IEC Level		N	—
			SAE Level		1	—

1 Data based on qualification test results.

6 Ordering Information

This section contains ordering information for MC9S08SV16 series devices. See below for an example of the device numbering system.

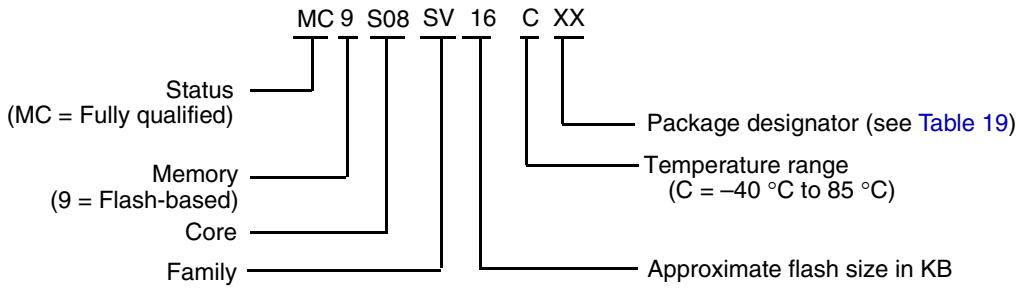
Table 18. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	FLASH	RAM	
MC9S08SV16	16 KB	1024 Byte	32-pin SDIP 32-pin LQFP
MC9S08SV8	8 KB	768 Byte	

1 See the reference manual, *MC9S08SV16 Series Reference Manual*, for a complete description of modules included on each device.

2 See Table 19 for package information.

Example of the device numbering system:



7 Package Information

Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
32	Low Quad Flat Package	LQFP	LC	873A-03	98ASH70029A
32	Shrink Dual In-line Package	SDIP	BM	1376-02	98ASA99330D

7.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19.