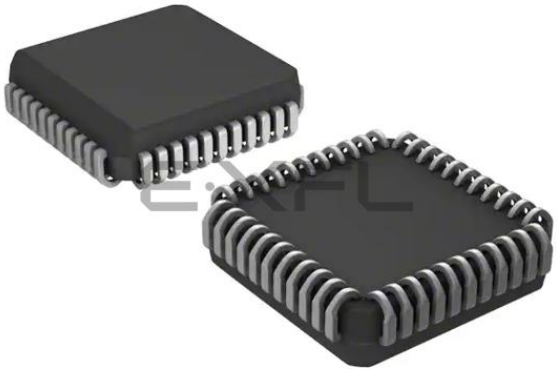


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-plg44c

The systems are available for 386/486/Pentium™ PC and for HP™ and Sun™ workstations and for running Viewlogic®, Mentor Graphics®, Cadence™, OrCAD™, and Synopsys design environments.

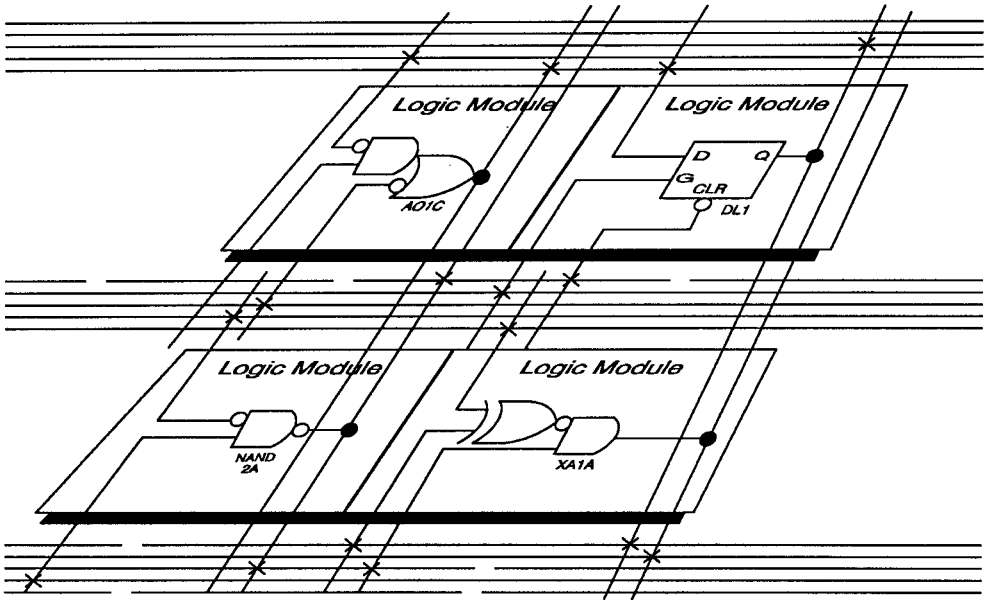


Figure 1 • *Partial View of an ACT 1 Device*

ACT 1 Device Structure

A partial view of an ACT 1 device (Figure 1) depicts four logic modules and distributed horizontal and vertical interconnect tracks. PLICE antifuses, located at intersections of the horizontal and vertical tracks, connect logic module inputs and outputs. During programming, these antifuses are addressed and programmed to make the connections required by the circuit application.

The ACT 1 Logic Module

The ACT 1 logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 2).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array, since latches and flip-flops may be constructed from logic modules wherever needed in the application.

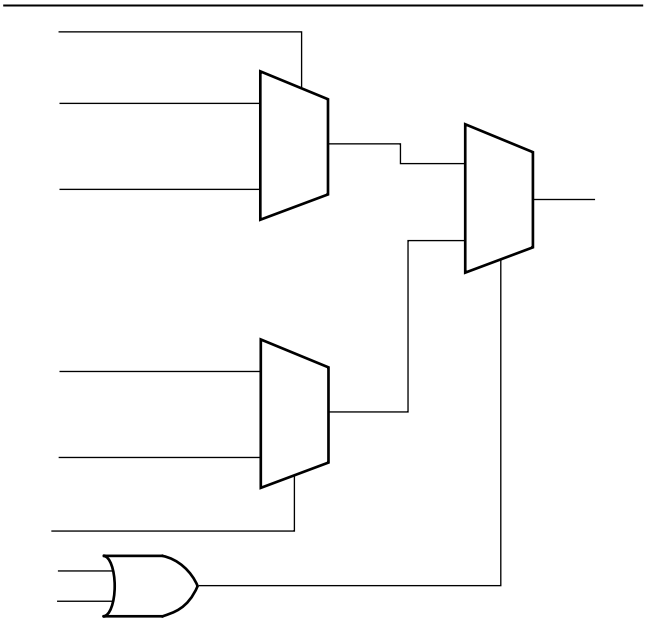


Figure 2 • *ACT 1 Logic Module*

I/O Buffers

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Outputs sink or

source 10 mA at TTL levels. See Electrical Specifications for additional I/O buffer specifications.

Device Organization

ACT 1 devices consist of a matrix of logic modules arranged in rows separated by wiring channels. This array is surrounded by a ring of peripheral circuits including I/O buffers, testability circuits, and diagnostic probe circuits providing real-time diagnostic capability. Between rows of logic modules are routing channels containing sets of segmented metal tracks with PLICE antifuses. Each channel has 22 signal tracks. Vertical routing is permitted via 13 vertical tracks per logic module column. The resulting network allows arbitrary and flexible interconnections between logic modules and I/O modules.

Probe Pin

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe® diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished.

ACT 1 Array Performance

Temperature and Voltage Effects

Worst-case delays for ACT 1 arrays are calculated in the same manner as for masked array products. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects. However, in an ACT 1 array, temperature and voltage effects are less dramatic than with masked devices. The electrical characteristics of module interconnections on ACT 1 devices remain constant over voltage and temperature fluctuations.

As a result, the total derating factor from typical to worst-case for a standard speed ACT 1 array is only 1.19 to 1, compared to 2 to 1 for a masked gate array.

Logic Module Size

Logic module size also affects performance. A mask programmed gate array cell with four transistors usually implements only one logic level. In the more complex logic module (similar to the complexity of a gate array macro) of an ACT 1 array, implementation of multiple logic levels within a single module is possible. This eliminates interlevel wiring and associated RC delays. The effect is termed "net compression."

Ordering Information

A1010 B – 2 PL 84 C

- **C** — Application (Temperature Range)
  - C = Commercial (0 to +70°C)
  - I = Industrial (–40 to +85°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
- **84** — Package Lead Count
- **PL** — Package Type
  - PL = Plastic J-Leaded Chip Carriers
  - PQ = Plastic Quad Flatpacks
  - CQ = Ceramic Quad Flatpack
  - PG = Ceramic Pin Grid Array
  - VQ = Very Thin Quad Flatpack
- **2** — Speed Grade
  - Blank = Standard Speed
  - –1 = Approximately 15% faster than Standard
  - –2 = Approximately 25% faster than Standard
  - –3 = Approximately 35% faster than Standard
- **B** — Die Revision
  - B = 1.0 micron CMOS Process
- **A1010** — Part Number
  - A1010 = 1200 Gates (5 V)
  - A1020 = 2000 Gates (5 V)
  - A10V10 = 1200 Gates (3.3 V)
  - A10V20 = 2000 Gates (3.3 V)

Product Plan

	Speed Grade*				Application			
	Std	–1	–2	–3	C	I	M	B
A1010B Device								
44-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	✔	—	—
68-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	✔	✔	—	—
80-pin Very Thin (1.0 mm) Quad Flatpack (VQ)	✔	✔	✔	✔	✔	—	—	—
84-pin Ceramic Pin Grid Array (PG)	✔	✔	—	—	✔	—	✔	✔
A1020B Device								
44-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	✔	—	—
68-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	✔	—	—
84-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	✔	✔	—	—
80-pin Very Thin (1.0 mm) Quad Flatpack (VQ)	✔	✔	✔	✔	✔	—	—	—
84-pin Ceramic Pin Grid Array (PG)	✔	✔	—	—	✔	—	✔	✔
84-pin Ceramic Quad Flatpack (CQ)	✔	✔	—	—	✔	—	✔	✔
A10V10B Device								
68-pin Plastic Leaded Chip Carrier (PL)	✔	—	—	—	✔	—	—	—
80-pin Very Thin (1.0 mm) Quad Flatpack (VQ)	✔	—	—	—	✔	—	—	—
A10V20B Device								
68-pin Plastic Leaded Chip Carrier (PL)	✔	—	—	—	✔	—	—	—
84-pin Plastic Leaded Chip Carrier (PL)	✔	—	—	—	✔	—	—	—
80-pin Very Thin (1.0 mm) Quad Flatpack (VQ)	✔	—	—	—	✔	—	—	—

Applications: C = Commercial
I = Industrial
M = Military
B = MIL-STD-883

Availability: ✔ = Available
P = Planned
— = Not Planned

* Speed Grade: –1 = Approx. 15% faster than Standard
–2 = Approx. 25% faster than Standard
–3 = Approx. 35% faster than Standard

Device Resources

Device	Logic Modules	Gates	User I/Os				
			44-pin	68-pin	80-pin	84-pin	100-pin
A1010B, A10V10B	295	1200	34	57	57	57	57
A1020B, A10V20B	547	2000	34	57	69	69	69

Pin Description

CLK Clock (Input)

TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/O. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage

Input HIGH supply voltage.

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	–0.5 to +7.0	Volts
V_I	Input Voltage	–0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	–0.5 to V_{CC} +0.5	Volts
I_{IO}	I/O Sink/Source Current[3]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *$V_{PP} = V_{CC}$, except during device programming.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) used for commercial and industrial; case temperature (T_C) used for military.*

Package Thermal Characteristics

The device junction to case thermal characteristics is θjc, and the junction to ambient air characteristics is θja. The thermal characteristics for θja are shown with two different air flow rates. Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for an 84-pin plastic leaded chip carrier at commercial temperature is as follows:

$$\frac{\text{Max junction temp.(°C)} - \text{Max commercial temp.(°C)}}{\theta ja(°C/W)} = \frac{150°C - 70°C}{37°C/W} = 2.2\ W$$

Package Type	Pin Count	θjc	θja Still Air	θja 300 ft/min	Units
Plastic J-Leaded Chip Carrier	44	15	45	35	°C/W
	68	13	38	29	°C/W
	84	12	37	28	°C/W
Plastic Quad Flatpack	100	13	48	40	°C/W
Very Thin (1.0 mm) Quad Flatpack	80	12	43	35	°C/W
Ceramic Pin Grid Array	84	8	33	20	°C/W
Ceramic Quad Flatpack	84	5	40	30	°C/W

General Power Equation

$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

I_{CC}	V_{CC}	Power
3 mA	5.25 V	15.75 mW (max)
1 mA	5.25 V	5.25 mW (typ)
0.75 mA	3.60 V	2.70 mW (max)
0.30 mA	3.30 V	0.99 mW (typ)

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the

external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1.

$$\text{Power (uW)} = C_{EQ} * V_{CC2} * F \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

	A10V10B A10V20B	A1010B A1020B
Modules (C_{EQM})	3.2	3.7
Input Buffers ($_{CEQI}$)	10.9	22.1
Output Buffers (C_{EQO})	11.6	31.2
Routed Array Clock Buffer Loads (C_{EQCR})	4.1	4.6

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1}] \quad (2)$$

Where:

m	=	Number of logic modules switching at fm
n	=	Number of input buffers switching at fn
p	=	Number of output buffers switching at fp
q_1	=	Number of clock loads on the first routed array clock (All families)
r_1	=	Fixed capacitance due to first routed array clock (All families)
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz (All families)

Fixed Capacitance Values for Actel FPGAs (pF)

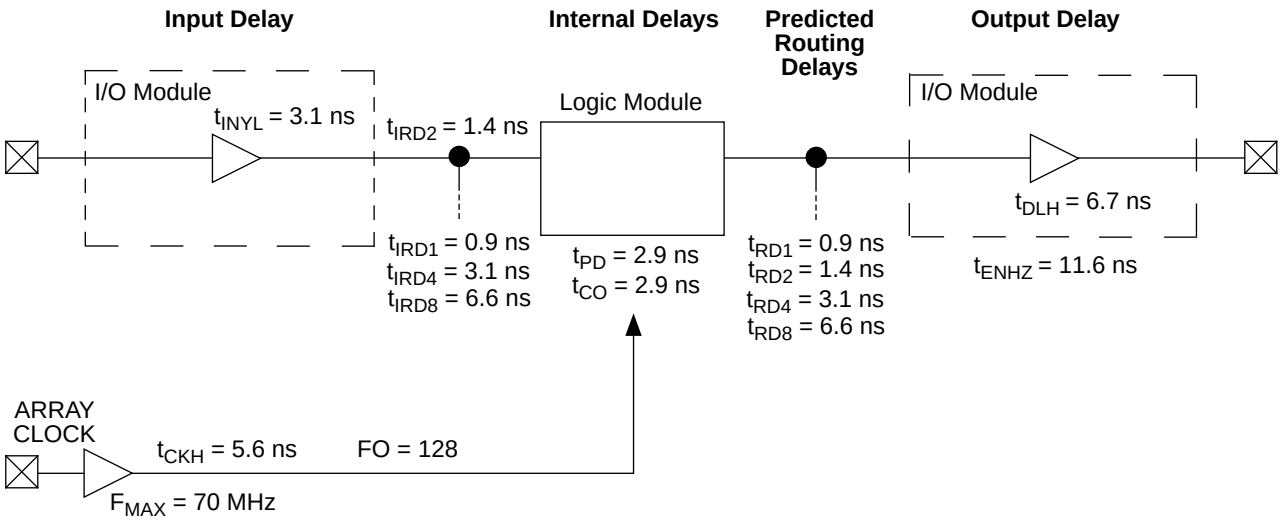
Device Type	r_1 routed_Clk1
A1010B	41.4
A1020B	68.6
A10V10B	40
A10V20B	65

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Logic Modules (m)	90% of modules
Inputs switching (n)	#inputs/4
Outputs switching (p)	#outputs/4
First routed array clock loads (q_1)	40% of modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F

ACT 1 Timing Module*



** Values shown for ACT 1 '–3 speed' devices at worst-case commercial conditions.*

Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The ACT 1 family delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 1 family's antifuses, fabricated in 1.0 micron lithography, offer nominal levels of 200 ohms resistance and 7.5 femtofarad (fF) capacitance per antifuse.

The ACT 1 fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The ACT 1 family's proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for ACT 1 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 1 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 5 ns to 10 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A best case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the "standard speed" timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	**Max.**	**Min.**	**Max.**
(Commercial Minimum/Maximum Specification) x	0.69	1.11	0.67	1.23

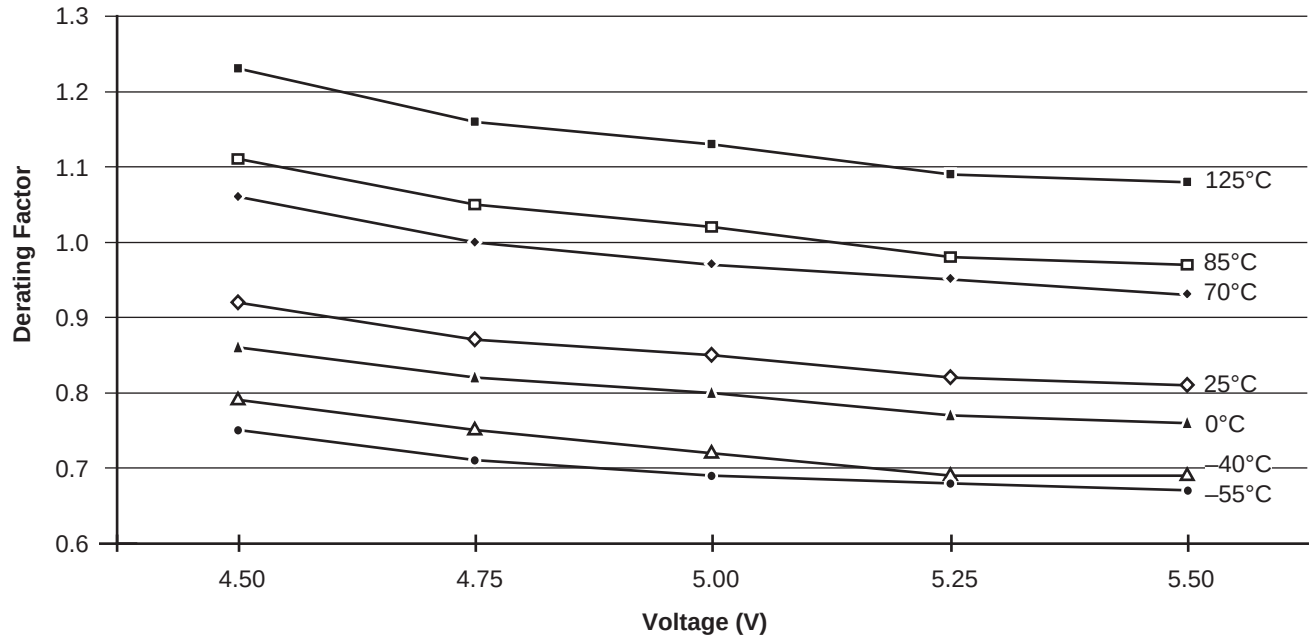
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	–55	**–40**	**0**	**25**	**70**	**85**	**125**
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.16
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

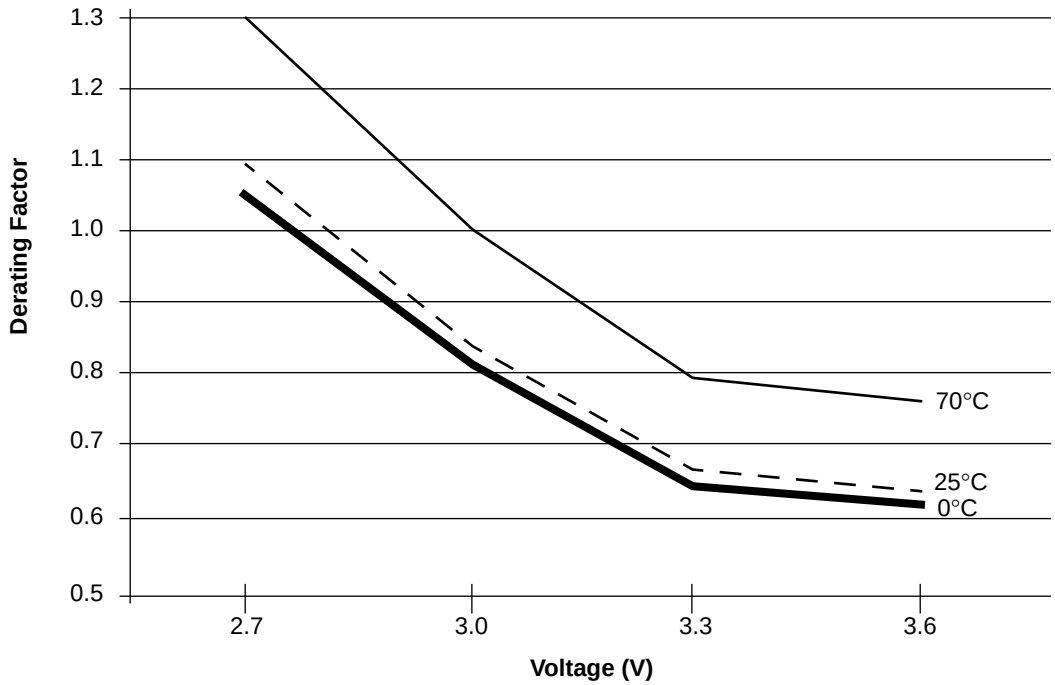


Note: *This derating factor applies to all routing and propagation delays.*

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 3.0 V, 70°C)

	0	25	70
2.7	1.05	1.09	1.30
3.0	0.81	0.84	1.00
3.3	0.64	0.67	0.79
3.6	0.62	0.64	0.76

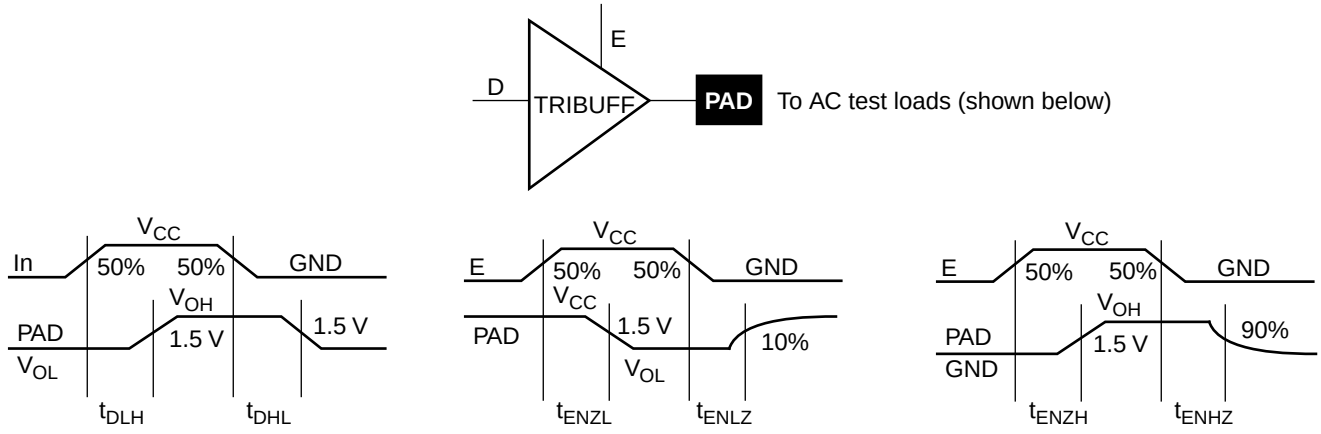
Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, T_J = 3.0 V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*

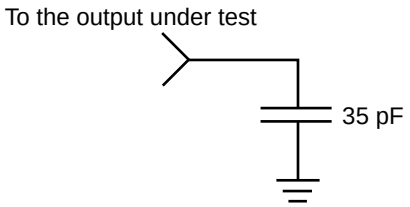
Parameter Measurement

Output Buffer Delays

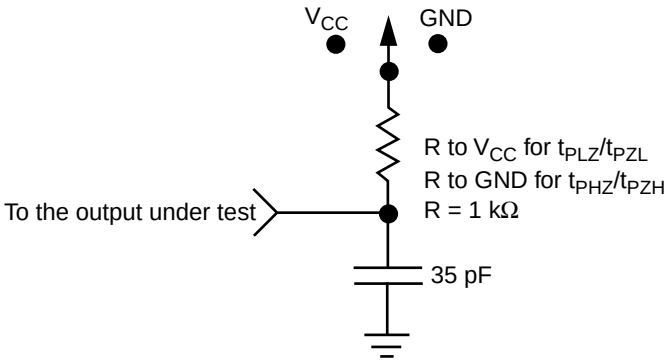


AC Test Loads

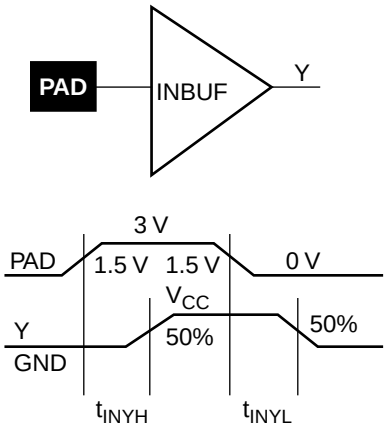
Load 1
(Used to measure propagation delay)



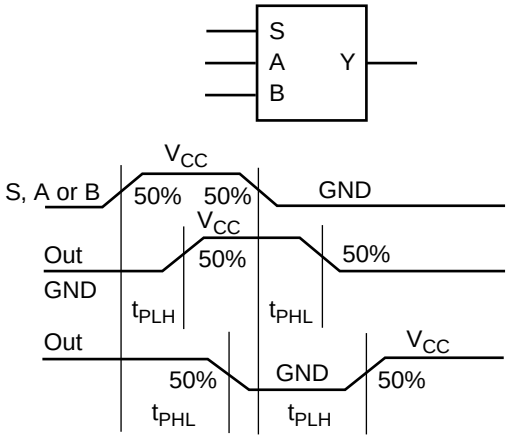
Load 2
(Used to measure rising/falling edges)

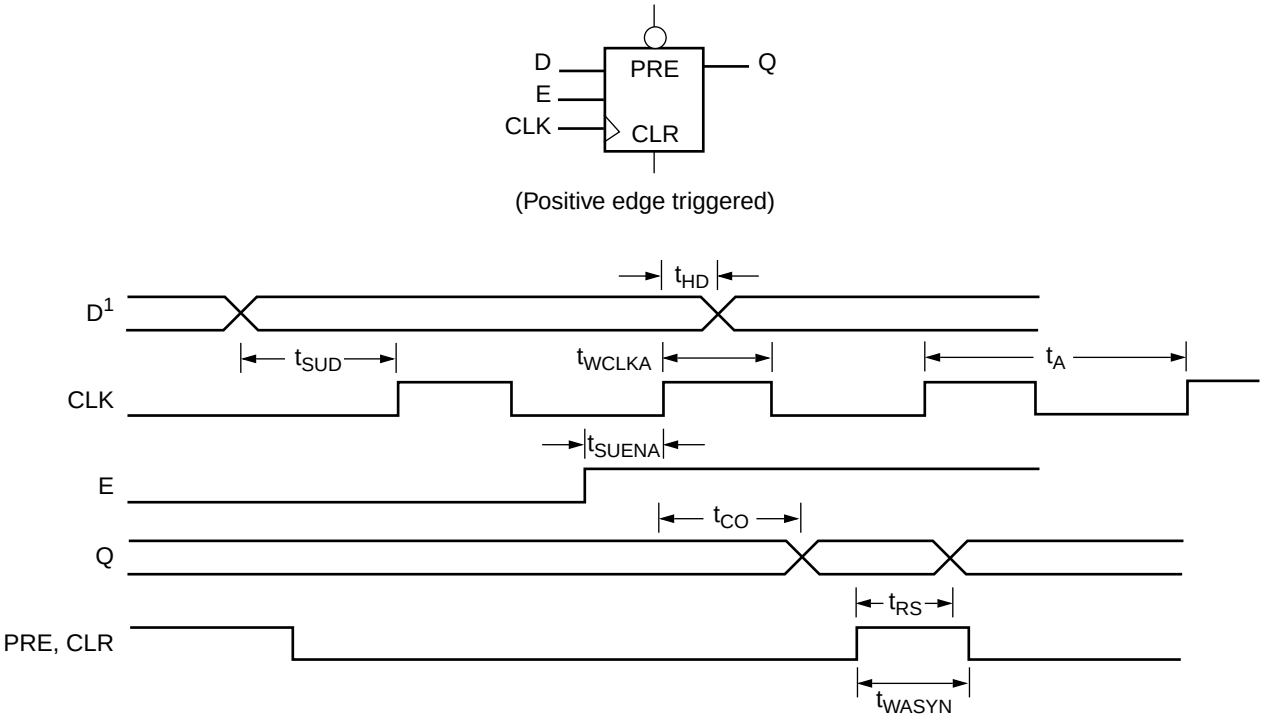


Input Buffer Delays



Module Delays





Note: *D represents all data functions involving A, B, S for multiplexed flip-flops.*

ACT 1 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3 V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.9		3.4		3.8		4.5		6.5	ns
t_{PD2}	Dual Module Macros		6.8		7.8		8.8		10.4		15.1	ns
t_{CO}	Sequential Clk to Q		2.9		3.4		3.8		4.5		6.5	ns
t_{GO}	Latch G to Q		2.9		3.4		3.8		4.5		6.5	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.9		3.4		3.8		4.5		6.5	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		0.9		1.1		1.2		1.4		2.0	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.7		1.9		2.2		3.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5		2.8		3.3		4.8	ns
t_{RD4}	FO=4 Routing Delay		3.1		3.6		4.1		4.8		7.0	ns
t_{RD8}	FO=8 Routing Delay		6.6		7.7		8.7		10.2		14.8	ns
Sequential Timing Characteristics[3]												
t_{SUD}	Flip-Flop (Latch) Data Input Setup	5.5		6.4		7.2		8.5		10.0		ns
t_{HD}[4]	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	5.5		6.4		7.2		8.5		10.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.8		8.0		9.0		10.5		9.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.8		8.0		9.0		10.5		9.8		ns
t_A	Flip-Flop Clock Input Period	14.2		16.7		18.9		22.3		20.0		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		70		60		53		45		50	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
4. *The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.*

ACT 1 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3 V Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			3.1		3.5		4.0		4.7		6.8	ns
t_{INYL}	Pad to Y Low			3.1		3.5		4.0		4.7		6.8	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			0.9		1.1		1.2		1.4		2.0	ns
t_{IRD2}	FO=2 Routing Delay			1.4		1.7		1.9		2.2		3.2	ns
t_{IRD3}	FO=3 Routing Delay			2.1		2.5		2.8		3.3		4.8	ns
t_{IRD4}	FO=4 Routing Delay			3.1		3.6		4.1		4.8		7.0	ns
t_{IRD8}	FO=8 Routing Delay			6.6		7.7		8.7		10.2		14.8	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 16		4.9		5.6		6.4		7.5		6.7	
		FO = 128		5.6		6.4		7.3		8.6		7.9	ns
t_{CKL}	Input High to Low	FO = 16		6.4		7.4		8.4		9.9		8.8	
		FO = 128		7.0		8.1		9.2		10.8		10.0	ns
t_{PWH}	Minimum Pulse Width	FO = 16	6.5		7.5		8.5		10.0		8.9		
	High	FO = 128	6.8		8.0		9.0		10.5		9.8		ns
t_{PWL}	Minimum Pulse Width	FO = 16	6.5		7.5		8.5		10.0		8.9		
	Low	FO = 128	6.8		8.0		9.0		10.5		9.8		ns
t_{CKSW}	Maximum Skew	FO = 16		1.2		1.3		1.5		1.8		1.5	
		FO = 128		1.8		2.1		2.4		2.8		2.4	ns
t_P	Minimum Period	FO = 16	13.2		15.4		17.6		20.9		18.2		
		FO = 128	14.2		16.7		18.9		22.3		20		ns
f_{MAX}	Maximum Frequency	FO = 16		75		65		57		48		55	
		FO = 128		70		60		53		45		50	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

ACT 1 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

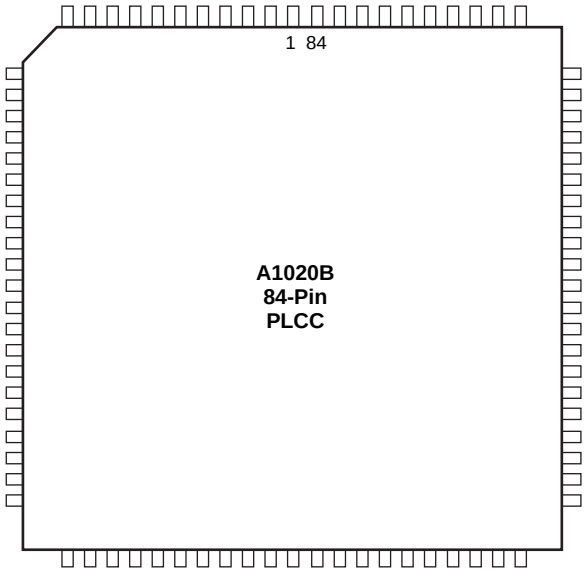
Output Module Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		3.3 V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data to Pad High		6.7		7.6		8.7		10.3		15.0	ns
t_{DHL}	Data to Pad Low		7.5		8.6		9.8		11.5		16.7	ns
t_{ENZH}	Enable Pad Z to High		6.6		7.5		8.6		10.2		14.8	ns
t_{ENZL}	Enable Pad Z to Low		7.9		9.1		10.4		12.2		17.7	ns
t_{ENHZ}	Enable Pad High to Z		10.0		11.6		13.1		15.4		22.4	ns
t_{ENLZ}	Enable Pad Low to Z		9.0		10.4		11.8		13.9		20.2	ns
d_{TLH}	Delta Low to High		0.06		0.07		0.08		0.09		0.13	ns/pF
d_{THL}	Delta High to Low		0.08		0.09		0.10		0.12		0.17	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data to Pad High		7.9		9.2		10.4		12.2		17.7	ns
t_{DHL}	Data to Pad Low		6.4		7.2		8.2		9.8		14.2	ns
t_{ENZH}	Enable Pad Z to High		6.0		6.9		7.9		9.2		13.4	ns
t_{ENZL}	Enable Pad Z to Low		8.3		9.4		10.7		12.7		18.5	ns
t_{ENHZ}	Enable Pad High to Z		10.0		11.6		13.1		15.4		22.4	ns
t_{ENLZ}	Enable Pad Low to Z		9.0		10.4		11.8		13.9		20.2	ns
d_{TLH}	Delta Low to High		0.10		0.11		0.13		0.15		0.22	ns/pF
d_{THL}	Delta High to Low		0.06		0.07		0.08		0.09		0.13	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the “Simultaneous Switching Output Limits for Actel FPGAs” application note on page 4-125.*

Package Pin Assignments (continued)

84-Pin PLCC



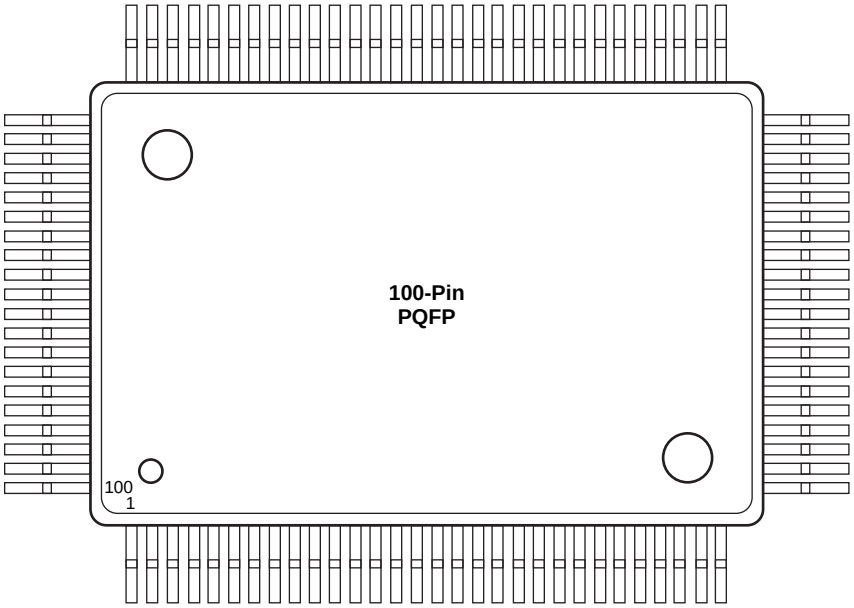
Signal	A1020B, A10V20B Function
4	VCC
12	NC
18	GND
19	GND
25	VCC
26	VCC
33	VCC
40	GND
46	VCC
60	GND
61	GND
64	CLK, I/O
66	MODE
67	VCC
68	VCC
72	SDI, I/O
73	DCLK, I/O
74	PRA, I/O
75	PRB, I/O
82	GND

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP



Pin	A1010B Function	A1020B Function
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
6	PRB, I/O	PRB, I/O
13	GND	GND
19	VCC	VCC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	I/O
32	NC	I/O
33	NC	I/O
36	GND	GND
37	GND	GND
43	VCC	VCC
44	VCC	VCC
48	NC	I/O
49	NC	I/O
50	NC	I/O
51	NC	NC
52	NC	NC

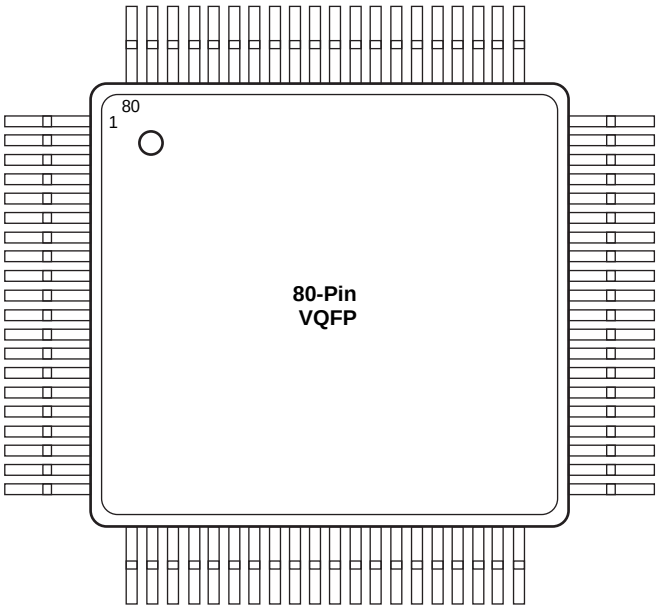
Pin	A1010B Function	A1020B Function
53	NC	NC
54	NC	NC
55	NC	NC
56	VCC	VCC
63	GND	GND
69	VCC	VCC
77	NC	NC
78	NC	NC
79	NC	NC
80	NC	I/O
81	NC	I/O
82	NC	I/O
86	GND	GND
87	GND	GND
90	CLK, I/O	CLK, I/O
92	MODE	MODE
93	VCC	VCC
94	VCC	VCC
95	NC	I/O
96	NC	I/O
97	NC	I/O
98	SDI, I/O	SDI, I/O
99	DCLK, I/O	DCLK, I/O
100	PRA, I/O	PRA, I/O

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

80-Pin VQFP



Pin	A1010B, A10V10B Function	A1020B, A10V20B Function
2	NC	I/O
3	NC	I/O
4	NC	I/O
7	GND	GND
13	VCC	VCC
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
27	GND	GND
33	VCC	VCC
41	NC	I/O
42	NC	I/O
43	NC	I/O

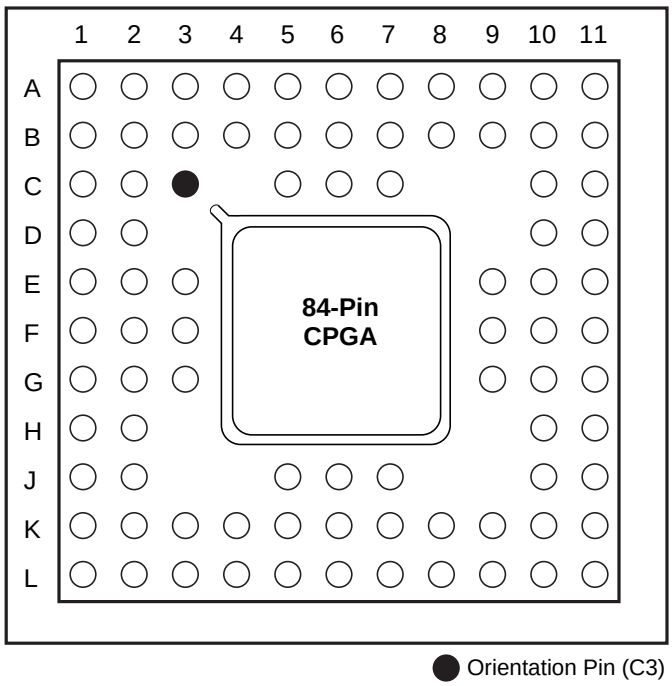
Pin	A1010B, A10V10B Function	A1020B, A10V20B Function
47	GND	GND
50	CLK, I/O	CLK, I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
68	GND	GND
74	VCC	VCC

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin CPGA



Pin	A1010B Function	A1020B Function
A11	PRA, I/O	PRA, I/O
B1	NC	I/O
B2	NC	NC
B5	VCC	VCC
B7	GND	GND
B10	PRB, I/O	PRB, I/O
B11	SDI, I/O	SDI,I/O
C1	NC	I/O
C2	NC	I/O
C10	DCLK, I/O	DCLK, I/O
C11	NC	I/O
D10	NC	I/O
D11	NC	I/O
E2	GND	GND
E3	GND	GND
E9	VCC	VCC

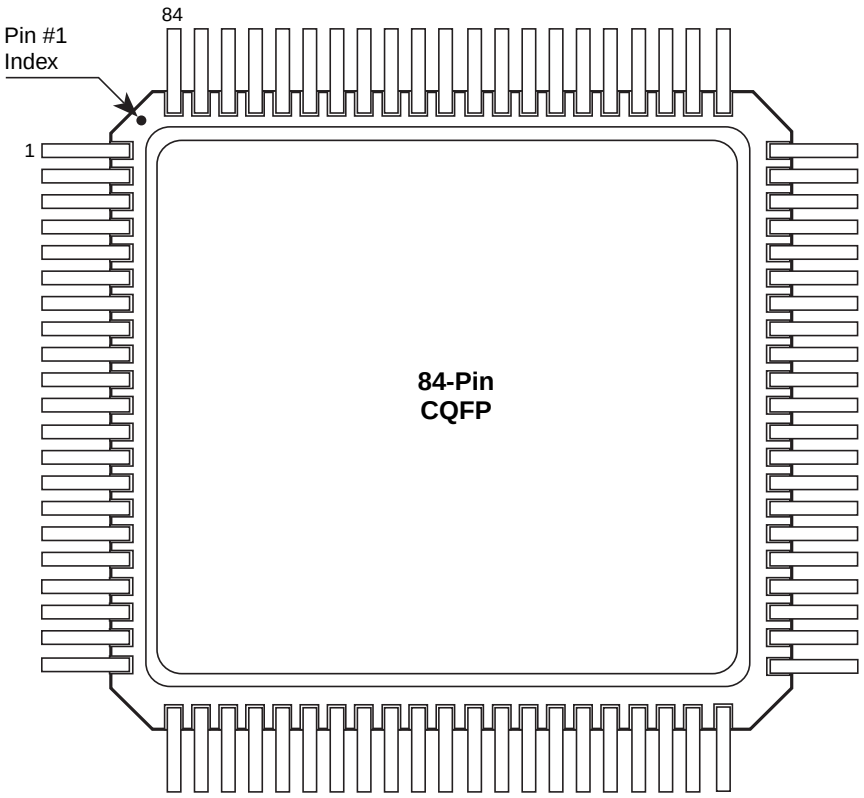
Pin	A1010B Function	A1020B Function
E10	VCC	VCC
E11	MODE	MODE
F1	VCC	VCC
F9	CLK, I/O	CLK, I/O
F10	GND	GND
G2	VCC	VCC
G10	GND	GND
J2	NC	I/O
J10	NC	I/O
K1	NC	I/O
K2	VCC	VCC
K5	GND	GND
K7	VCC	VCC
K10	NC	I/O
K11	NC	I/O
L1	NC	I/O

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin CQFP



Pin	A1020B Function
1	NC
7	GND
8	GND
14	VCC
15	VCC
22	VCC
29	GND
35	VCC
49	GND
50	GND

Pin	A1020B Function
53	CLK, I/O
55	MODE
56	VCC
57	VCC
61	SDI, I/O
62	DCLK, I/O
63	PRA, I/O
64	PRB, I/O
71	GND
77	VCC

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*