Infineon Technologies - MB91F464AAPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	73
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 21x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f464aapmc-gse2

Package and technology

- Package : 100-pin plastic LQFP (LQFP-100)
- CMOS 0.18 µm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Description
57	P21_0	I/O	A	General-purpose input/output port
	SIN0			Data input pin for USART0
58	P21_1	I/O	A	General-purpose input/output port
	SOT0			Data output pin for USART0
59	P21_2	I/O	A	General-purpose input/output port
	SCK0			Clock input/output pin for USART0
	CK0			External clock input pin for free-run timer 0
60	P21_4	I/O	A	General-purpose input/output port
	SIN1			Data input pin for USART1
61	P21_5	I/O	A	General-purpose input/output port
	SOT1			Data output pin for USART1
62	P21_6	I/O	A	General-purpose input/output port
	SCK1			Clock input/output pin for USART1
	CK1			External clock input pin for free-run timer 1
65 to 67	P17_5 to P17_7	I/O	A	General-purpose input/output ports
	PPG5 to PPG7			PPG timer output pins
68 to 71	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
72	P22_0	I/O	A	General-purpose input/output port
	RX4			RX input pin for CAN4
	INT12			External interrupt input pin
73	P22_1	I/O	A	General-purpose input/output port
	TX4			TX output pin for CAN4
74, 77 to 83	P24_0 to P24_7	I/O	A	General-purpose input/output ports
	INT0 to INT7			External interrupt input pins
84	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin for USART2
85	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin for USART2

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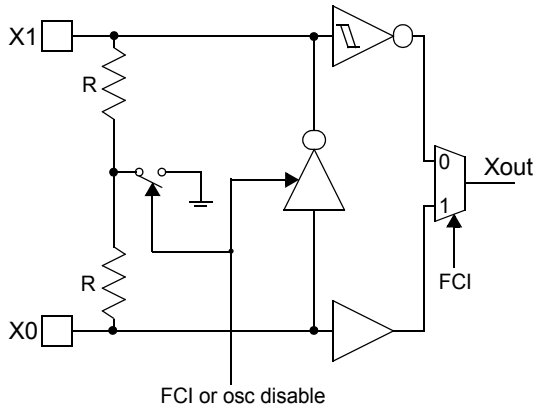
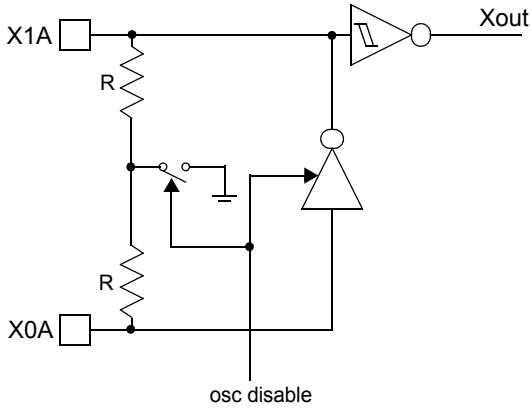
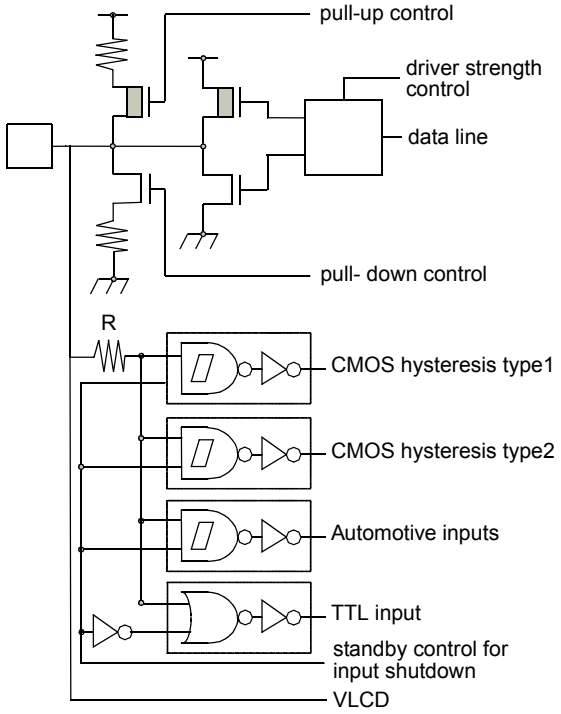
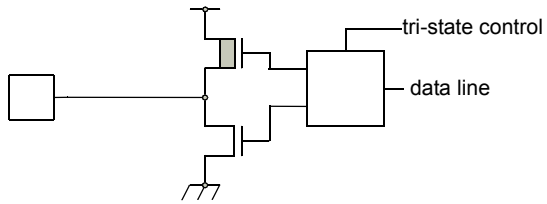
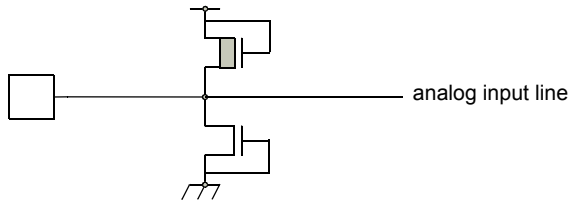
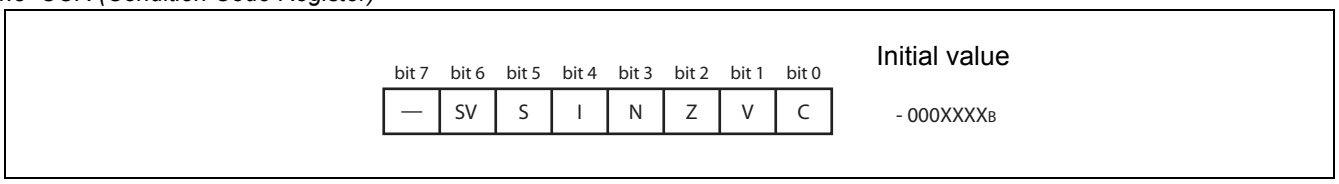
Type	Circuit	Remarks
J1		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: ■ Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

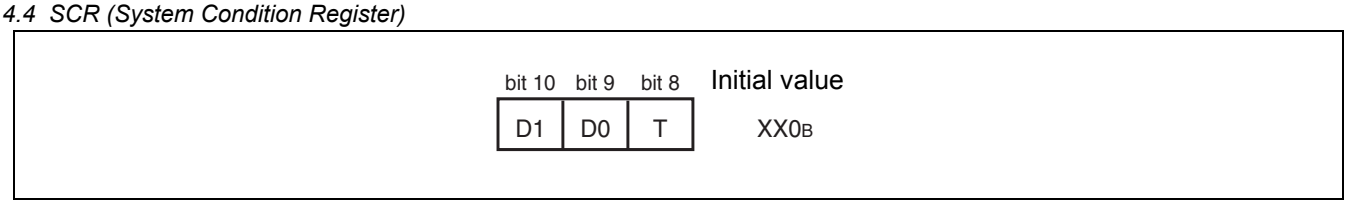
Type	Circuit	Remarks
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

8.4.3 CCR (Condition Code Register)



SV : Supervisor flag
S : Stack flag
I : Interrupt enable flag
N : Negative enable flag
Z : Zero flag
V : Overflow flag
C : Carry flag

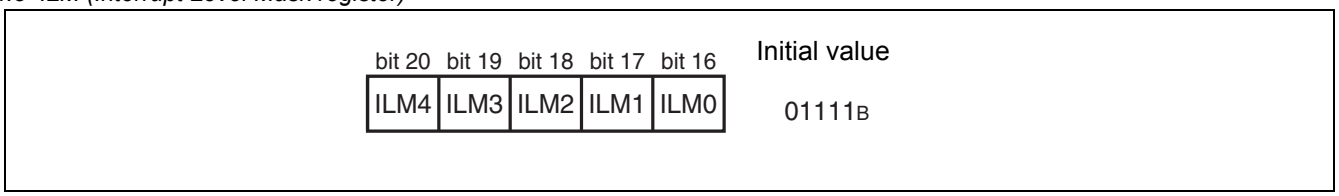
8.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

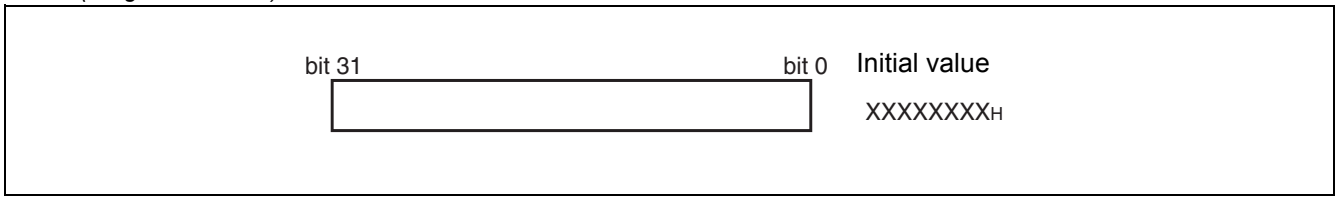
Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

8.4.5 ILM (Interrupt Level Mask register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.
The register is initialized to value “01111_B” at reset.

8.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.
The initial value at reset is undefined.

9.6 Flash Security

9.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

■ FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except INTVEC mode MD[2:0] = “000”)

■ FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

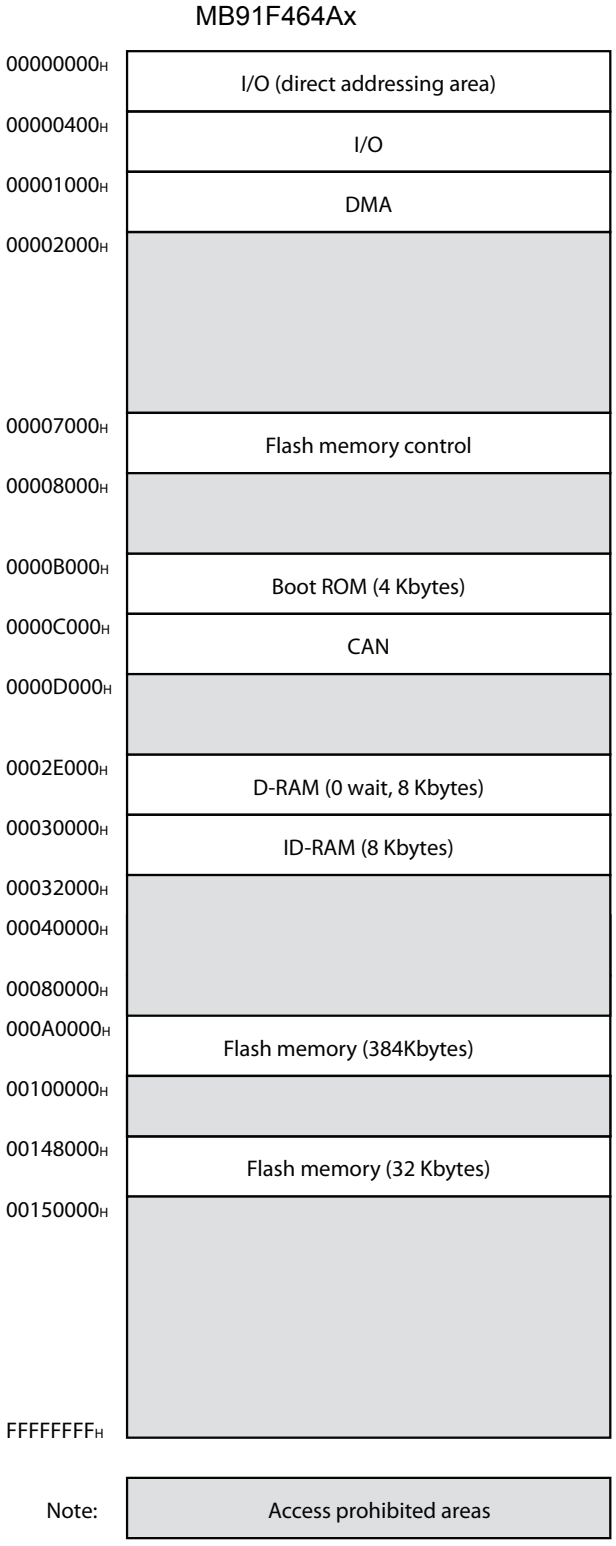
Explanation of the bits in the Flash Security Vector FSV1 [15:0]

MB91F464Ax

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	–	set to “0”	set to “1”	not available
FSV1[1]	–	set to “0”	set to “1”	not available
FSV1[2]	–	set to “0”	set to “1”	not available
FSV1[3]	–	set to “0”	set to “1”	not available
FSV1[4]	SA4	set to “0”	–	write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	

11. Memory Maps

■ **MB91F464Ax**



Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H to 000008_H	Reserved				R-bus Port Data Register
$00000C_H$	Reserved		PDR14 [R/W] XXXXXXXX	PDR15 [R/W] - - XXXXXX	
000010_H	PDR16 [R/W] X - - - - - XX	PDR17 [R/W] XXXXXXXX	Reserved	PDR19 [R/W] - - - - - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - XXX - XXX	PDR22 [R/W] - - XX - - XX	Reserved	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved		PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] - - - XXXXX	PDR29 [R/W] XXXXXXXX	Reserved		
000020_H to $00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External Interrupt (INT0 to INT7)
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External Interrupt (INT8 to INT15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay Interrupt
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] -00000XX	Reserved		
000048_H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] -00000XX	Reserved		
000050_H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000160_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H, $00019C_H$	Reserved				Reserved
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved				Reserved
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] - - XXXXXX	R-bus Port Data Direct Read Register
$000D10_H$	PDRD16 [R] X - - - - - XX	PDRD17 [R] XXXXXXXX	Reserved	PDRD19 [R] - - - - - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - XXX - XXX	PDRD22 [R] - - XX - - XX	Reserved	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved		PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] - - - XXXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$ to $000D48_H$	Reserved				Reserved
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] - - 000000	R-bus Port Direction Register
$000D50_H$	DDR16 [R/W] 0 - - - - - 00	DDR17 [R/W] 00000000	Reserved	DDR19 [R/W] - - - - - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - 000 - 000	DDR22 [R/W] - - 00 - - 00	Reserved	
$000D58_H$	DDR24 [R/W] 00000000	Reserved		DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] - - - 00000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D88_H$	Reserved				Reserved
$000D8C_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] - - 000000	R-bus Port Function Register
$000D90_H$	PFR16 [R/W] 0 - - - - - 00	PFR17 [R/W] 00000000	Reserved	PFR19 [R/W] - - - - - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] - - 00 - - 00	Reserved	
$000D98_H$	PFR24 [R/W] 00000000	Reserved		PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] - - - 00000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$ to $000DC8_H$	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E8C_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] - - 000000	R-bus Expansion Port Input Level Select Register
$000E90_H$	EPILR16 [R/W] 0 - - - - - 00	EPILR17 [R/W] 00000000	Reserved	EPILR19 [R/W] - - - - - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - 000 - 000	EPILR22 [R/W] - - 00 - - 00	Reserved	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved		EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] - - - 00000	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EC8_H$	Reserved				Reserved
$000ECC_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] - - 000000	R-bus Port Pull-Up/Down Enable Register
$000ED0_H$	PPER16 [R/W] 0 - - - - - 00	PPER17 [R/W] 00000000	Reserved	PPER19 [R/W] - - - - - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] - - 00 - - 00	Reserved	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved		PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] - - - 00000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000F08_H$	Reserved				Reserved
$000F0C_H$	Reserved		PPCR14 [R/W] 11111111	PPCR15 [R/W] - - 1111111	R-bus Port Pull-Up/Down Control Register
$000F10_H$	PPCR16 [R/W] 1- - - - - 11	PPCR17 [R/W] 11111111	Reserved	PPCR19 [R/W] - 1- - - 111	
$000F14_H$	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] - - 11 - - 11	Reserved	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved		PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] - - - 11111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved

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14.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 48MHz. Base clock frequencies above 48 MHz are not allowed on MB91F465Kx.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	*1
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	*1
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	*1
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	*1

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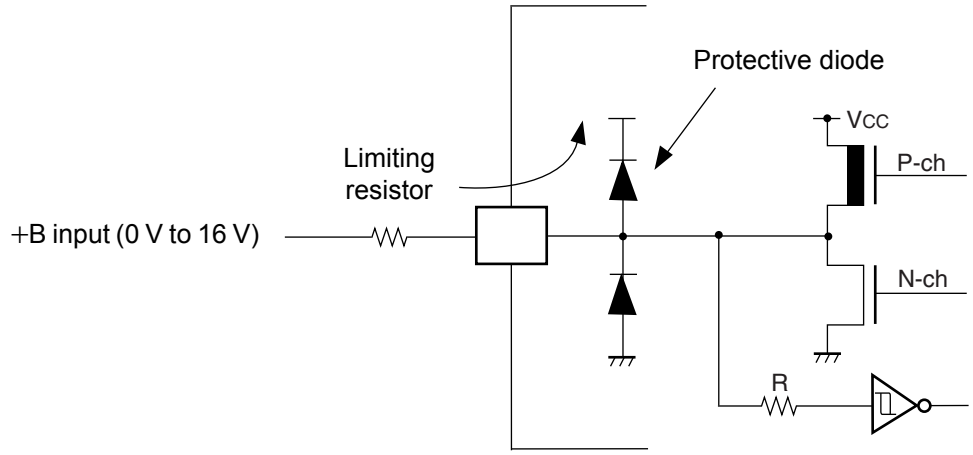
is input.

- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit :

- Input/output equivalent circuit



*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

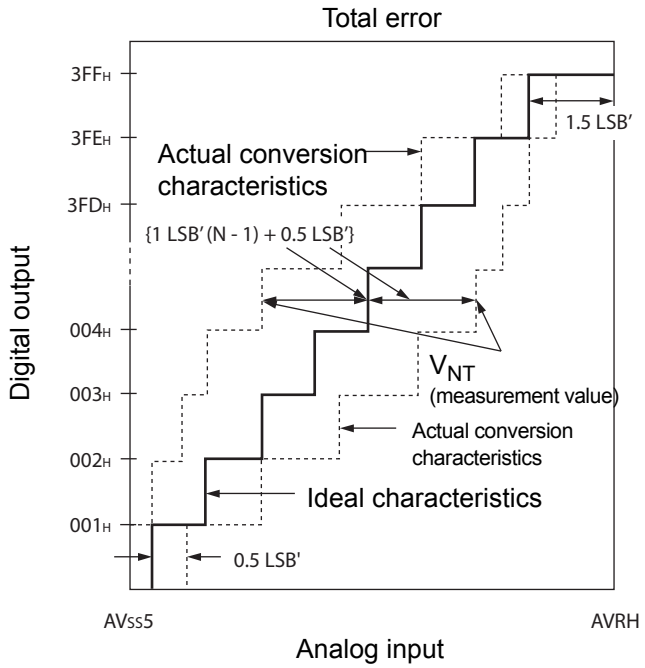
*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -2mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -1.6mA$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -5mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -3mA$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OH} = -3mA$	$V_{DD} - 0.5$	—	—	V	
Output “L“ voltage	V_{OL2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OL} = +2mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OL} = +1.6mA$	—	—	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OL} = +5mA$ $3.0V \le V_{DD} \le 4.5V$, $I_{OL} = +3mA$	—	—	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OL} = +3mA$	—	—	0.4	V	
Input leakage current	I_{IL}	Pnn_m *1	$3.0V \le V_{DD} \le 5.5V$ T_A=25 °C	−1	—	+1	µA	$V_{SS}5 < V_I < V_{DD}$
			$3.0V \le V_{DD} \le 5.5V$ T_A=105 °C	−3	—	+3	µA	
Analog input leakage current	I_{AIN}	ANn *2	$3.0V \le V_{DD} \le 5.5V$ T_A=25 °C	−1	—	+1	µA	$AV_{SS}5 < V_I < AV_{CC}5$, AVRH5
			$3.0V \le V_{DD} \le 5.5V$ T_A=105 °C	−3	—	+3	µA	

1. Pnn_m includes all GPIO pins. Analog (AN) channels and Pull Up/Pull Down are disabled.
2. ANn includes all pins where AN channels are enabled.



$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
V_{FST}' (ideal value) = AVRH − 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H

(Continued)

15.5 FLASH memory program/erase characteristics

15.5.1 MB91F464Ax

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	μs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

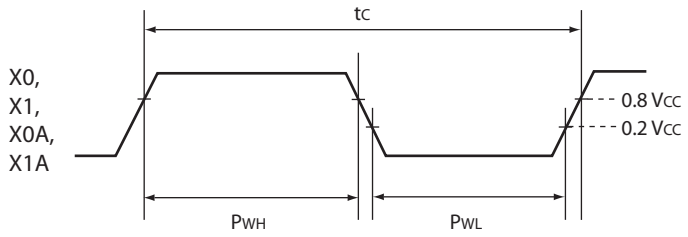
15.6 AC characteristics

15.6.1 Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

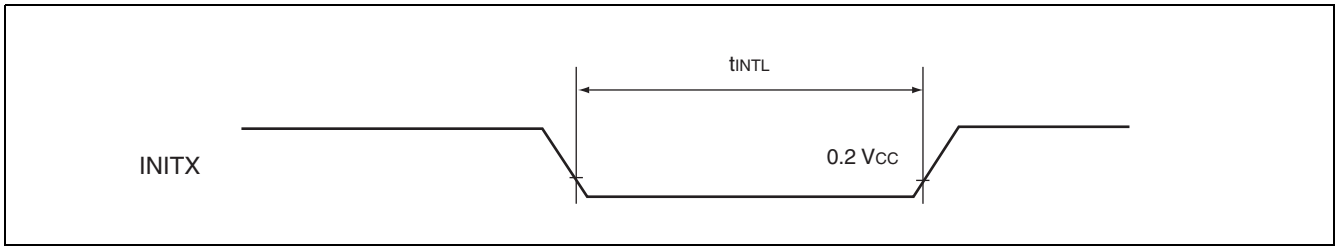
- Clock timing conditions



15.6.2 Reset input ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	–	10	–	ms
INITX input time (other than the above)				20	–	µs



15.6.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:

- ❒ IO_{drive} = 5 mA
- ❒ $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ $V_{SS}5$ = 0 V
- ❒ T_A = -40 °C to +105 °C
- ❒ C_l = 50 pF (load capacity value of pins when testing)
- ❒ VOL = 0.2 x $V_{DD}5$
- ❒ VOH = 0.8 x $V_{DD}5$
- ❒ EPILR = 0, PILR = 1 (Automotive Level == worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	–	4 t_{CLKP}	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		– 30	30	– 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} – 30*	–	m × t_{CLKP} – 20*	–	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	–	t_{CLKP} + 45	–	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	–	0	–	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	–	t_{CLKP} + 10	–	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	–	t_{CLKP} + 10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		–	2 t_{CLKP} + 55	–	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	–	10	–	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	–	t_{CLKP} + 10	–	ns
SCK rising time	t_{FE}	SCKn		–	20	–	20	ns
SCK falling time	t_{RE}	SCKn		–	20	–	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :

- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :

- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

15.6.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - T_A = − 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis V_{IL}/V_{IH} = 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	–	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	–	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	–	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	–	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	–	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	–	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	–	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	–	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.