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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16ce624-20i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-7Fh (Bank0) on the PIC16CE623/624 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16CE625 are General Purpose Registers implemented as static RAM. Some special purpose registers are mapped in Bank 1. In all three microcontrollers, address space F0h-FFh (Bank1) is mapped to 70-7Fh (Bank0) as common RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 96×8 in the PIC16CE623/624 and 128 x 8 in the PIC16CE625. Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

4.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 4-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the status register as 000uu1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any status bit. For other instructions, not affecting any status bits, see the "Instruction Set Summary".

Note 1:	The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16CE62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
Note 2:	The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 4-1: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
IRP bit7	RP1	RP0	TO	PD	Z	DC	C bit0	R = Readable bit W = Writable bit
								U = Unimplemented bit, read as '0'
								-n = Value at POR reset -x = Unknown at POR reset
bit 7:	IRP: The IF	RP bit is r	eserved or	the PIC1	6CE62X, a	lways mair	ntain this bit	t clear.
bit 6:5	RP<1:O>: 11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	Register 3 (180h - 2 (100h - 1 (80h - 1 0 (00h - 1 is 128 by	Bank Sele 1FFh) 17Fh) FFh) 7Fh) rtes. The R	ct bits (use P1 bit is re	ed for direc	t addressin ways maint	g) tain this bit d	clear.
bit 4:	TO : Time-o 1 = After po 0 = A WDT	out bit ower-up, ⁻ time-out	CLRWDT in	struction, o	or sleep ii	nstruction		
bit 3:	PD : Power- 1 = After po 0 = By exe	-down bit ower-up c cution of	or by the CI the SLEEP	LRWDT instruction	truction			
bit 2:	Z : Zero bit 1 = The res 0 = The res	sult of an sult of an	arithmetic arithmetic	or logic op or logic op	peration is a	zero not zero		
bit 1:	DC : Digit c 1 = A carry 0 = No carr	arry/borro v-out from ry-out fro	bw bit (ADD the 4th low m the 4th l	WF, ADDLW w order bit ow order b	of the result of the result	SUBWF instr ult occurred sult	uctions) (for I	or borrow the polarity is reversed)
bit 0:	C: Carry/bc 1 = A carry 0 = No carr Note: For b second ope the source	orrow bit -out from ry-out from porrow the erand. Fo register.	(ADDWF, AD the most s m the mos e polarity is r rotate (RH	DLW, SUB: significant t significan s reversed RF, RLF) in	LW, SUBWF bit of the ro t bit of the . A subtrac structions,	instructior esult occurr result occu tion is exec this bit is lo	ns) red urred suted by add baded with e	ding the two's complement of the either the high or low order bit of

4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

REGISTER 4-3: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	R = Readable bit
bit7							bit0	 W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR reset -x = Unknown at POR reset
bit 7:	GIE: Glob 1 = Enabl 0 = Disab	oal Interru les all un-r les all inte	ot Enable masked in errupts	bit terrupts				
bit 6:	PEIE: Per 1 = Enabl 0 = Disab	ripheral In les all un-r les all per	terrupt En masked pe ipheral int	able bit eripheral ir errupts	nterrupts			
bit 5:	TOIE : TMI 1 = Enabl 0 = Disab	R0 Overflo les the TM les the TM	ow Interrup 1R0 interru /IR0 interr	ot Enable I .pt upt	bit			
bit 4:	INTE: RB 1 = Enabl 0 = Disab	0/INT Exte les the RB les the RE	ernal Inter 30/INT exte 30/INT ext	rupt Enabl ərnal interr ernal inter	le bit rupt rupt			
bit 3:	RBIE : RB 1 = Enabl 0 = Disab	Port Cha les the RB les the RE	nge Intern 3 port char 3 port cha	upt Enable 1ge interru nge interrı	e bit pt ıpt			
bit 2:	TOIF : TMI 1 = TMRC 0 = TMRC	R0 Overflo) register l) register (ow Interrup has overflo did not ove	ot Flag bit owed (mus erflow	t be cleare	d in softwa	ire)	
bit 1:	INTF : RB 1 = The F 0 = The F	0/INT Exte }B0/INT ex }B0/INT ex	ernal Inter xternal inte xternal inte	rupt Flag b errupt occi errupt did i	oit urred (must not occur	be cleare	d in softwaı	are)
bit 0:	RBIF : RB 1 = When 0 = None	Port Cha at least c of the RB	nge Internone of the <a>	upt Flag bi RB<7:4> p s have cha	t bins change anged state	d state (m	ust be clea	ared in software)

4.2.2.4 PIE1 REGISTER

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4: PIE1 REGISTER (ADDRESS 8CH)



4.2.2.5 PIR1 REGISTER

This register contains the individual flag bit for the comparator interrupt.

Note:	Interrupt flag bits get set when an interrup						
	condition occurs, regardless of the state of						
	its corresponding enable bit or the global						
	enable bit, GIE (INTCON<7>). User						
	software should ensure the appropriate						
	interrupt flag bits are clear prior to enabling						
	an interrupt.						

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)



4.2.2.6 PCON REGISTER

The PCON register contains flag bits to differentiate between a Power-on Reset, an external $\overline{\text{MCLR}}$ reset, WDT reset or a Brown-out Reset.

Note:	BOD is unknown on Power-on Reset. It
	must then be set by the user and checked
	on subsequent resets to see if BOD is
	cleared, indicating a brown-out has
	occurred. The BOD status bit is a "don't
	care" and is not necessarily predictable if
	the brown-out circuit is disabled (by
	programming BODEN bit in the
	configuration word).

REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)



TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function			
RA0/AN0	bit0	ST	Input/output or comparator input			
RA1/AN1	bit1	ST	Input/output or comparator input			
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output			
RA3/AN3	bit3	ST	Input/output or comparator input/output			
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.			

Legend: ST = Schmitt Trigger input

TABLE 5-2:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
05h	PORTA	—	_	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	—	—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT		—	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged

Note: Shaded bits are not used by PORTA.







6.2 Device Addressing

After generating a START condition, the processor transmits a control byte consisting of a EEPROM address and a Read/Write bit that indicates what type of operation is to be performed. The EEPROM address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one, a read operation is selected, and when set to a zero, a write operation is selected. (Figure 6-3). The bus is monitored for its corresponding EEPROM address all the time. It generates an acknowledge bit if the EEPROM address was true and it is not in a programming mode.

FIGURE 6-3: CONTROL BYTE FORMAT







FIGURE 6-8: RANDOM READ

BUS ACTIVITY

. .

A C K

DATAn



DATAn + 1

DATAn + 2

N O

A C K

DATAn + X

7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

10.2 Oscillator Configurations

10.2.1 OSCILLATOR TYPES

The PIC16CE62X can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

10.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 10-1). The PIC16CE62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 10-2).

FIGURE 10-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 10-1 and Table 10-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 10-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 10-1: CERAMIC RESONATORS, PIC16CE62X

Ranges Tested: OSC2 Mode Freq OSC1 XT 455 kHz 68 - 100 pF 68 - 100 pF 15 - 68 pF 15 - 68 pF 2.0 MHz 4.0 MHz 15 - 68 pF 15 - 68 pF HS 10 - 68 pF 10 - 68 pF 8.0 MHz 16.0 MHz 10 - 22 pF 10 - 22 pF

These values are for design guidance only. See notes at bottom of page.

TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16CE62X

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2	
LP	32 kHz	33 pF	33 pF	
	200 kHz	15 pF	15 pF	
XT	200 kHz	47-68 pF	47-68 pF	
	1 MHz	15 pF	15 pF	
	4 MHz	15 pF	15 pF	
HS	4 MHz	15 pF	15 pF	
	8 MHz	15-33 pF	15-33 pF	
	20 MHz	15-33 pF	15-33 pF	

These values are for design guidance only. See notes at bottom of page.

- 1. Recommended values of C1 and C2 are identical to the ranges tested table.
- 2. Higher capacitance increases the stability of oscillator, but also increases the start-up time.
- 3. Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

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Bit Test f, Skip if Set							
[label] BTFSS f,b							
$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b < 7 \end{array}$							
skip if (f<	b>) = 1						
None							
01	11bb	bfff	ffff				
If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.							
1							
1(2)							
HERE BTFSS FLAG,1 FALSE GOTO PROCESS_CODE TRUE • •							
Before In	struction						
After Inst	PC = a ruction if FLAG<1> PC = a if FLAG<1> PC = a	ddress H r = 0, address F. r = 1, address T	ERE ALSE RUE				
	Bit Test 1 [label] B $0 \le f \le 12$ $0 \le b < 7$ skip if (f< None 1 If bit 'b' in r instruction If bit 'b' is ' fetched du execution, executed it two-cycle it 1 1(2) HERE FALSE TRUE Before In After Inst	Bit Test f, Skip if S [label] BTFSS f,t $0 \le f \le 127$ $0 \le b < 7$ skip if (f) = 1 None 1 11bb If bit 'b' in register 'f' is instruction is skipped. If bit 'b' is '1', then the fetched during the cur executed instead, ma two-cycle instruction. 1 1(2) HERE BTFSS FALSE GOTO TRUE • • • Before Instruction PC = a After Instruction PC = a if FLAG<1> PC = a if FLAG<1> PC = a	Bit Test f, Skip if Set[label] BTFSS f,b $0 \le f \le 127$ $0 \le b < 7$ skip if (f) = 1None111bit 'b' in register 'f' is '1' then the instruction is skipped.If bit 'b' is '1', then the next instru- fetched during the current instru- executed instead, making this a two-cycle instruction.11(2)HEREBTFSS FLAG, 1 FALSE GOTOHEREBTFSS FLAG, 1 FALSETRUE••				

CLRF	RF Clear f								
Syntax:	[label] ([<i>label</i>] CLRF f							
Operands:	$0 \le f \le 127$								
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$								
Status Affected: Z									
Encoding:	0 0	0001	lff	E	ffff				
Description:	The contents of register 'f' are cleared and the Z bit is set.								
Words:	1								
Cycles:	1								
Example	CLRF	FLAC	G_REG						
	Before Instruction								
	FLAG_REG = 0x5A								
	After Instruction								
		FLAG_RE	EG =	=	0x00				
		/	-	_	1				

CALL	Call Subroutine						
Syntax:	[<i>label</i>] CALL k						
Operands:	$0 \le k \le 2047$						
Operation:	(PC)+ 1 \rightarrow TOS, k \rightarrow PC<10:0>, (PCLATH<4:3>) \rightarrow PC<12:11>						
Status Affected:	None						
Encoding:	10 0kkk kkkk kkkk						
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruc- tion.						
Words:	1						
Cycles:	2						
Example	HERE CALL THERE						
	Before Instruction PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1						

CLRW	Clear W					
Syntax:	[label] CLRW					
Operands:	None					
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$					
Status Affected:	Z					
Encoding:	00 0001 0000 0011					
Description:	W register is cleared. Zero bit (Z) is set.					
Words:	1					
Cycles:	1					
Example	CLRW					
	Before Instruction W = 0x5A After Instruction W = 0x00 Z = 1					

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MPLIB is a librarian for pre-compiled code to be used with MPLINK. When a routine from a library is called from another source file, only the modules that contains that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. MPLIB manages the creation and modification of library files.

MPLINK features include:

- MPLINK works with MPASM and MPLAB-C17 and MPLAB-C18.
- MPLINK allows all memory areas to be defined as sections to provide link-time flexibility.

MPLIB features include:

- MPLIB makes linking easier because single libraries can be included instead of many smaller files.
- MPLIB helps keep code maintainable by grouping related modules together.
- MPLIB commands allow libraries to be created and modules to be added, listed, replaced, deleted, or extracted.

12.5 MPLAB-SIM Software Simulator

The MPLAB-SIM Software Simulator allows code development in a PC host environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file or user-defined key press to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPLAB-C18 and MPASM. The Software Simulator offers the flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

12.6 <u>MPLAB-ICE High Performance</u> <u>Universal In-Circuit Emulator with</u> <u>MPLAB IDE</u>

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of MPLAB-ICE is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support new PIC microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows 3.x/95/98 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE 2000 is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems use the same processor modules and will operate across the full operating speed range of the PIC MCU.

12.7 PICMASTER/PICMASTER CE

The PICMASTER system from Microchip Technology is a full-featured, professional quality emulator system. This flexible in-circuit emulator provides a high-quality, universal platform for emulating Microchip 8-bit PIC microcontrollers (MCUs). PICMASTER systems are sold worldwide, with a CE compliant model available for European Union (EU) countries.

12.8 <u>ICEPIC</u>

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X, and PIC16CXXX families of 8-bit one-timeprogrammable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

12.9 MPLAB-ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB-ICD, is a powerful, low-cost run-time development tool. This tool is based on the flash PIC16F877 and can be used to develop for this and other PIC microcontrollers from the PIC16CXXX family. MPLAB-ICD utilizes the In-Circuit Debugging capability built into the PIC16F87X. This feature, along with Microchip's In-Circuit Serial Programming protocol, offers cost-effective in-circuit flash programming and debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time. The MPLAB-ICD is also a programmer for the flash PIC16F87X family.

12.10 PRO MATE II Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In

and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

12.17 <u>SEEVAL Evaluation and Programming</u> <u>System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in tradeoff analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

12.18 <u>KEELOQ Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.





FIGURE 13-9: TIMER0 CLOCK TIMING



TABLE 13-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	_	_	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		<u>Tcy + 40</u> * N			ns	N = prescale value (1, 2, 4,, 256)

t

These parameters are characterized but not tested. Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

13.6 EEPROM Timing





Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks	
	Min. Max. Min. Max		Max.					
Clock frequency	FCLK		100		400	kHz		
Clock high time	Thigh	4000	—	600	_	ns		
Clock low time	TLOW	4700	—	1300	—	ns		
SDA and SCL rise time	TR	_	1000	—	300	ns	(Note 1)	
SDA and SCL fall time	TF	_	300	_	300	ns	(Note 1)	
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated	
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition	
Data input hold time	THD:DAT	0		0	—	ns	(Note 2)	
Data input setup time	TSU:DAT	250	—	100	_	ns		
STOP condition setup time	Tsu:sto	4000	—	600	_	ns		
Output valid from clock	ΤΑΑ	_	3500	_	900	ns	(Note 2)	
Bus free time	TBUF	4700		1300	_	ns	Time the bus must be free before a new transmission can start	
Output fall time from VIH minimum to VI∟ maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), $CB \le 100 \text{ pF}$	
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	_	50	ns	(Note 3)	
Write cycle time	Twr	—	10	_	10	ms	Byte or Page mode	
Endurance	_	10M 1M	-	10M 1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)	

TABLE 13-7: AC CHARACTERISTICS

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension Limits		MIN	MIN NOM		MIN	NOM	MAX	
Number of Pins n			20			20		
Pitch	р		.026			0.66		
Overall Height	A	.068	.073	.078	1.73	1.85	1.98	
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83	
Standoff	A1	.002	.006	.010	0.05	0.15	0.25	
Overall Width	E	.299	.309	.322	7.59	7.85	8.18	
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38	
Overall Length	D	.278	.284	.289	7.06	7.20	7.34	
Foot Length	L	.022	.030	.037	0.56	0.75	0.94	
Lead Thickness	с	.004	.007	.010	0.10	0.18	0.25	
Foot Angle	¢	0	4	8	0.00	101.60	203.20	
Lead Width	В	.010	.013	.015	0.25	0.32	0.38	
Mold Draft Angle Top	α	0	5	10	0	5	10	
Mold Draft Angle Bottom	β	0	5	10	0	5	10	

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150

Drawing No. C04-072

14.1 Package Marking Information

18-Lead PDIP



20-Lead SSOP



Example



Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available of or customer-specific information.

NOTES:

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