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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625-04-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CE62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CE62X uses a Harvard architecture in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM) and non-volatile memory (EEPROM) for each PIC16CE62X device.

Device	Program Memory	RAM Data Memory	EEPROM Data Memory
PIC16CE623	512x14	96x8	128x8
PIC16CE624	1Kx14	96x8	128x8
PIC16CE625	2Kx14	128x8	128x8

The PIC16CE62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CE62X family has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CE62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CE62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

4.3 PCL and PCLATH

The program counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-6 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 4-6: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CE62X family has an 8 level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.
- Note 2: There are no instruction/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
05h	PORTA	—	_	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	—	—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT		—	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged

Note: Shaded bits are not used by PORTA.

7.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the TOCS bit (OPTION<5>). In timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the TOSE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 <u>Timer0 Interrupt</u>

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.



FIGURE 7-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0 \rightarrow WDT)

1.BCF	STATUS, RPO	;Skip if already in
		; Bank 0
2.CLRWDT		;Clear WDT
3.CLRF	TMR0	;Clear TMR0 & Prescaler
4.BSF	STATUS, RPO	;Bank 1
5.MOVLW	'00101111'b	;These 3 lines (5, 6, 7)
6.MOVWF	OPTION	; are required only if
		; desired PS<2:0> are
7.CLRWDT		; 000 or 001
8.MOVLW	'00101xxx'b	;Set Postscaler to
9.MOVWF	OPTION	; desired WDT rate
10.BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 7-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 7-2: CHANGING PRESCALER (WDT \rightarrow TIMER0)

CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		;prescale value and
		;clock source
MOVWF	OPTION_REG	
BCF	STATUS, RPO	

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
01h	TMR0	Timer0	Fimer0 module register					xxxx xxxx	uuuu uuuu		
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_	_	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged.

Note: Shaded bits are not used by TMR0 module.

10.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC16CE62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

- 1. OSC selection
- 2. Reset

Power-on Reset (POR) Power-up Timer (PWRT) Oscillator Start-Up Timer (OST) Brown-out Reset (BOD)

- 3. Interrupts
- 4. Watchdog Timer (WDT)
- 5. SLEEP
- 6. Code protection
- 7. ID Locations
- 8. In-circuit serial programming

The PIC16CE62X has a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, and is designed to keep the part in reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which provides at least a 72 ms reset. With these three functions on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

10.3 <u>Reset</u>

The PIC16CE62X differentiates between various kinds of reset:

- a) Power-on reset (POR)
- b) MCLR reset during normal operation
- c) MCLR reset during SLEEP
- d) WDT reset (normal operation)
- e) WDT wake-up (SLEEP)
- f) Brown-out Reset (BOD)

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on reset, MCLR reset, WDT reset and MCLR reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different reset situations as indicated in Table 10-4. These bits are used in software to determine the nature of the reset. See Table 10-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 10-6.

The $\overline{\text{MCLR}}$ reset path has a noise filter to detect and ignore small pulses. See Table 13-5 for pulse width specification.



FIGURE 10-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

FIGURE 10-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



3: $R1 = 100\Omega$ to 1 k Ω will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 10-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
 - 2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

FIGURE 10-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \times \frac{R1}{R1 + R2} = 0.7 V$$

- **2:** Internal brown-out detection should be disabled when using this circuit.
- **3:** Resistors should be adjusted for the characteristics of the transistor.

FIGURE 10-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active reset pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

11.1 Instruction Descriptions

ADDLW	Add Literal a	nd \	w		
Syntax:	[label] ADD	[label] ADDLW k			
Operands:	$0 \le k \le 255$				
Operation:	$(W) + k \rightarrow (W)$	/)			
Status Affected:	C, DC, Z				
Encoding:	11 11	1x	kkkk	kkkk	
Description:	The contents o added to the ei result is placed	f the ght b in th	W register it literal 'k' ie W regist	are and the er.	
Words:	1				
Cycles:	1				
Example	ADDLW 0x	15			
	Before Instruc W After Instructi W	ction = on =	0x10 0x25		

ANDLW	AND Lite	ral with	w	
Syntax:	[label] A	ANDLW	k	
Operands:	$0 \le k \le 2\xi$	55		
Operation:	(W) .AND	0. (k) \rightarrow (W)	
Status Affected:	Z			
Encoding:	11	1001	kkkk	kkkk
Description:	The conter AND'ed wi result is pl	nts of W r th the eig aced in th	egister are ht bit literal le W regist	e I 'k'. The ter.
Words:	1			
Cycles:	1			
Example	ANDLW	0x5F		
	Before In After Inst	struction W = ruction W =	0xA3 0x03	

ADDWF	Add W a	nd f		
Syntax:	[label] ADDWF f,d			
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7		
Operation:	(W) + (f) -	\rightarrow (dest)		
Status Affected:	C, DC, Z			
Encoding:	0 0	0111	dfff	ffff
Description:	Add the co with registe stored in th result is sto	ntents of er 'f'. If 'd' ne W regi pred back	the W regi is 0, the re ster. If 'd' is in register	ster sult is 1, the r 'f'.
Words:	1			
Cycles:	1			
Example	ADDWF	FSR,	0	
	Before Inst	struction W = FSR = ruction W = FSR =	0x17 0xC2 0xD9 0xC2	

ANDWF	AND W with f
Syntax:	[label] ANDWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(W) .AND. (f) \rightarrow (dest)
Status Affected:	Z
Encoding:	00 0101 dfff ffff
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	ANDWF FSR, 1
	Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0x17 FSR = 0x02

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \end{array}$
Status Affected:	TO, PD
Encoding:	00 0000 0110 0100
Words:	Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set. 1
Cycles:	1
Example	CLRWDT
	Before Instruction WDT counter = ? After Instruction WDT counter = $0x00$ WDT prescaler = 0 TO = 1 PD = 1
COMF	Complement f
Syntax:	[<i>label</i>] COMF f,d

	$WDT counter = 0x00$ $WDT prescaler = 0$ $\overline{TO} = 1$ $\overline{PD} = 1$	
COMF	Complement f	DECFSZ
Syntax:	[label] COMF f,d	Syntax:
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$	Operand
Operation:	$(\bar{f}) \rightarrow (dest)$	Operatio
Status Affected:	Z	Status A
Encoding:	00 1001 dfff ffff	Encoding
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.	Descripti
Words:	1	
Cycles:	1	
Example	COMF REG1,0	
	Before Instruction REG1 = $0x13$ After Instruction REG1 = $0x13$ W = $0xEC$	Words: Cycles: Example

DECF	Decreme	ent f				
Syntax:	[label] DECF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$					
Operation:	(f) - 1 \rightarrow	(dest)				
Status Affected:	Z					
Encoding:	0 0	0011	dfi	Ef	ffff	
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in regis- ter 'f'.					
Words:	1					
Cycles:	1					
Example	DECF	CNT,	1			
	Before In	struction	-	0x01		
		Z	=	0		
	After Inst	ruction				
		CNT	=	0x00		
		Z	=	1		

DECFSZ	Decrement f, Skip if 0
Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (dest); skip if result = 0
Status Affected:	None
Encoding:	00 1011 dfff ffff
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.
Words:	1
Cycles:	1(2)
Example	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • •
	$\begin{array}{rcl} Before \ Instruction \\ PC &=& address \ {}_{HERE} \\ After \ Instruction \\ CNT &=& CNT - 1 \\ if \ CNT &=& 0, \\ PC &=& address \ CONTINUE \\ if \ CNT \neq& 0, \\ PC &=& address \ {}_{HERE+1} \\ \end{array}$

GOTO	Unconditiona	al Branch		INCFSZ	Incremen	t f, Skij	p if 0		
Syntax:	[<i>label</i>] GOTO k		Syntax:	[label] INCFSZ f,d					
Operands:	$0 \le k \le 2047$		Operands:	$0 \le f \le 127$					
Operation:	$k \rightarrow PC < 10:0 >$			$d \in [0,1]$					
	PCLATH<4:3>	\rightarrow PC<12:	11>	Operation:	(f) + 1 \rightarrow (dest), skip if result = 0)	
Status Affected:	None			Status Affected:	None				
Encoding:	10 1kł	k kkkk	kkkk	Encoding:	0 0	1111	dfff	fff	f
Description: Words:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>.Description:The content 			The conten incremente placed in th result is pla If the result which is alr A NOP is ex	ontents of register 'f' are nented. If 'd' is 0, the result is d in the W register. If 'd' is 1, the is placed back in register 'f'. result is 0, the next instruction, is already fetched, is discarded.				
Example	GOTO THERE				two-cycle ir	nstructio	n.		
	Aftor Instructiv	an		words.	1				
	PC = Address THERE	Cycles:	1(2)						
				Example	HERE CONTINU	INCF GOTO E	SZ (L	CNT, DOP	1

 $\begin{array}{rcl} Before \ Instruction \\ PC & = & address \ {\tt HERE} \\ After \ Instruction \\ CNT & = & CNT + 1 \\ if \ CNT = & 0, \\ PC & = & address \ CONTINUE \\ if \ CNT \neq & 0, \\ PC & = & address \ {\tt HERE} \ +1 \end{array}$

INCF	Increment f					
Syntax:	[label] INCF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$					
Operation:	(f) + 1 \rightarrow (dest)					
Status Affected:	Z					
Encoding:	00 1010 dfff ffff					
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.					
Words:	1					
Cycles:	1					
Example	INCF CNT, 1					
	$\begin{array}{rrrr} \text{Before Instruction} \\ & \text{CNT} & = & 0 \text{xFF} \\ & Z & = & 0 \end{array}$ After Instruction $\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$					

Inclusive OR Literal with W					
[<i>label</i>] IORLW k					
$0 \le k \le 255$					
(W) .OR. $k \rightarrow$ (W)					
Z					
11 1000 kkkk kkkk					
The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.					
1					
1					
IORLW 0x35					
Before Instruction W = 0x9A After Instruction W = 0xBF Z = 1					

SUBLW	Subtract W from Literal	SUBWF	Subtract W from f			
Syntax:	[<i>label</i>] SUBLW k	Syntax:	[<i>label</i>] SUBWF f,d			
Operands:	$0 \le k \le 255$	Operands:	$0 \le f \le 127$			
Operation:	$k - (W) \rightarrow (W)$		d ∈ [0,1]			
Status Affected:	C, DC, Z	Operation: Status	(f) - (W) \rightarrow (dest) C, DC, Z			
Encoding:	11 110x kkkk kkkk	Affected:				
Description:	The W register is subtracted (2's com- plement method) from the eight bit literal 'k'. The result is placed in the W register.	Encoding: Description:	00 0010 dfff ffff Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the			
Words:	1		result is stored in the W register. If 'd' is 1,			
Cycles:	1	Words [.]	1			
Example 1:	SUBLW 0x02	Cycles:	1			
	Before Instruction	Example 1	SUBWE REG1 1			
	W = 1 $C = ?$		Before Instruction			
	After Instruction W = 1 C = 1; result is positive		REG1 = 3 W = 2 C = ?			
Example 2:	Before Instruction		After Instruction			
	W = 2 C = ?		REG1 = 1 W = 2 C = 1; result is positive			
	After Instruction	Example 2:	Before Instruction			
Example 3:	W = 0 C = 1; result is zero Before Instruction		REG1 = 2 W = 2 C = ?			
	W = 3		After Instruction			
	C = ? After Instruction		REG1 = 0 W = 2 C = 1; result is zero			
	VV = 0XFF C = 0; result is nega-	Example 3:	Before Instruction			
	tive		REG1 = 1 W = 2 C = ?			
			After Instruction			
			REG1 = 0xFF W = 2 C = 0; result is negative			





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.





NOTES:

14.0 PACKAGING INFORMATION

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	INCHES*			N	IILLIMETERS	3	
Dimensior	1 Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

*Controlling Parameter JEDEC Equivalent: MO-036 Drawing No. C04-010

14.1 Package Marking Information

18-Lead PDIP



20-Lead SSOP



Example



Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available of or customer-specific information.

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