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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625-20-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 GENERAL DESCRIPTION

The PIC16CE62X are 18 and 20-Pin EPROM-based members of the versatile PIC[®] family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers with EEPROM data memory.

All PIC[®] microcontrollers employ an advanced RISC architecture. The PIC16CE62X family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single-cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CE62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16CE623 and PIC16CE624 have 96 bytes of RAM. The PIC16CE625 has 128 bytes of RAM. Each microcontroller contains a 128x8 EEPROM memory array for storing non-volatile information, such as calibration data or security codes. This memory has an endurance of 1,000,000 erase/write cycles and a retention of 40 plus years.

Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16CE62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low-cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16CE62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and reset. A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development, while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16CE62X mid-range microcontroller families.

A simplified block diagram of the PIC16CE62X is shown in Figure 3-1.

The PIC16CE62X series fits perfectly in applications ranging from multi-pocket battery chargers to low-power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16CE62X very versatile.

1.1 <u>Development Support</u>

The PIC16CE62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler is also available.

FIGURE 3-1: BLOCK DIAGRAM















FIGURE 6-8: RANDOM READ

BUS ACTIVITY

. .

A C K

DATAn



DATAn + 1

DATAn + 2

N O

A C K

DATAn + X





FIGURE 7-4: TIMER0 INTERRUPT TIMING



8.1 <u>Comparator Configuration</u>

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 8-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the comparator

mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 13-1.

Note: Comparator interrupts should be disabled during a comparator mode change, otherwise a false interrupt may occur.



FIGURE 8-1: COMPARATOR I/O OPERATING MODES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
1Fh	CMCON	C2OUT	C1OUT	_	—	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	_	—	—	_	—	—	-0	-0
8Ch	PIE1	—	CMIE	_	—	—	_	—	—	-0	-0
85h	TRISA		_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
Logondi	_ Unimn	lomontor	h rood oo	"0"	Linknown		hongod				

TABLE 8-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Legend: - = Unimplemented, read as "0", x = Unknown, u = unchanged

10.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 10-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 10-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 10-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 10-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



10.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 10-5 shows how the R/C combination is connected to the PIC16CE62X. For Rext values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high Rext values (i.e., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 14.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 14.0 for variation of oscillator frequency due to VDD for given Rext/Cext values, as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 10-5: RC OSCILLATOR MODE



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FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



FIGURE 10-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)



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10.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered; either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 10.8 for details on SLEEP and Figure 10-19 for timing of wake-up from SLEEP through RB0/INT interrupt.

10.5.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 7.0.

10.5.3 PORTB INTERRUPT

An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

10.5.4 COMPARATOR INTERRUPT

See Section 8.6 for complete description of comparator interrupts.



FIGURE 10-16: INT PIN INTERRUPT TIMING

FIGURE 10-17: WATCHDOG TIMER BLOCK DIAGRAM



FIGURE 10-18: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	—	BOREN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0

Legend: - = Unimplemented location, read as "0", + = Reserved for future use

Note: Shaded cells are not used by the Watchdog Timer.

IORWF	Inclusive OR W with f								
Syntax:	[<i>label</i>] IORWF f,d								
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$								
Operation:	(W) .OR. (f) \rightarrow (dest)								
Status Affected:	Z								
Encoding:	00 0100 dfff ffff								
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.								
Words:	1								
Cycles:	1								
Example	IORWF RESULT, 0								
	Before Instruction RESULT = 0x13 W = 0x91								
	After Instruction								
	RESULT = 0x13								
	VV = 0x93 $Z = 1$								

MOVF	Move f						
Syntax:	[label] MOVF f,d						
Operands:	$0 \le f \le 127$ $d \in [0,1]$						
Operation:	$(f) \rightarrow (dest)$						
Status Affected:	Z						
Encoding:	00 1000 dfff ffff						
	to a destination dependant upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.						
Words:	1						
Cycles:	1						
Example	MOVF FSR, 0						
	After Instruction W = value in FSR register Z = 1						

MOVLW	Move Literal to W						
Syntax:	[label]	MOVLW	/ k				
Operands:	$0 \le k \le 2$	55					
Operation:	$k \rightarrow (W)$						
Status Affected:	None						
Encoding:	11	00xx	kkkk	kkkk			
Description:	The eight register. T as 0's.	bit literal ' he don't c	k' is loaded ares will as	d into W ssemble			
Words:	1						
Cycles:	1						
Example	MOVLW	0x5A					
	After Inst	ruction W =	0x5A				

MOVWF	Move W	to f							
Syntax:	[label]	MOVW	= f						
Operands:	$0 \le f \le 12$	7							
Operation:	$(W) \rightarrow (f)$								
Status Affected:	None								
Encoding:	0 0	0000	1ff	f	ffff				
Description:	Move data 'f'.	from W r	egiste	er to r	register				
Words:	1								
Cycles:	1								
Example	MOVWF	OPT	TION						
	Before In:	struction OPTION W ruction OPTION W	= = =	0xFF 0x4F 0x4F 0x4F 0x4F	.				

SWAPF	Swap Nib	bles in	f		XORLW	Exclusiv	ve OR L	iteral wit	th W	
Syntax:	[label] S	SWAPF	f,d		Syntax:	[label]	XORL	Nk		
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				Operands:	$0 \le k \le 255$ (W) .XOR. $k \rightarrow$ (W) Z				
Operation:	$(f<3:0>) \rightarrow (dest<7:4>),$ $(f<7:4>) \rightarrow (dest<3:0>)$			Status Affected:						
Status Affected:	None				Encoding:	11	1010	kkkk	kkkk	
Encoding:	00 1110 dfff ffff Description:					The contents of the W register are				
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd'			f d' is 0, er. If 'd'	Words:	The result is placed in the W register.				
Marda	is 1, the res	sult is pla	ced in reg	ister 't'.	Cycles:	1				
Cycles:	1				Example:	XORLW	0xAF			
Example	SWAPF R	EG,	0			Before I	nstructio	n		
	Before Ins	truction					W =	0xB5		
		REG1	= 0x/	45		After Instruction				
	After Instru	uction					W =	0x1A		
		REG1 W	= 0x/ = 0x5	45 5A						

TRIS	Load TRIS Register						
Syntax:	[label] TRIS f						
Operands:	$5 \le f \le 7$						
Operation:	(W) \rightarrow TRIS register f;						
Status Affected:	None						
Encoding:	00 0000 0110 0fff						
Description: Words: Cycles: Example	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them. 1						
	To maintain upward compatibility with future PIC [®] MCU products, do not use this instruction.						

XORWF	Exclusive OR W with f								
Syntax:	[label]	XORWF	f,d						
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$								
Operation:	(W) .XOR. (f) \rightarrow (dest)								
Status Affected:	Z								
Encoding:	0 0	0110	dff	Ē	ffff				
Description:	Exclusive (W register the result is 'd' is 1, the ister 'f'.	OR the co with regis s stored ir result is s	ntents ster 'f'. In the V stored	s of t If 'd V reg bac	he ' is 0, gister. If k in reg-				
Words:	1								
Cycles:	1								
Example	XORWF	REG 3	1						
	Before In:	struction							
		REG W	= =	0xA 0xE	AF 35				
	After Inst	ruction							
		REG W	= =	Ox1 OxE	I A 35				

13.2 DC CHARACTERISTICS: F

PIC16LCE62X-04 (Commercial, Industrial)

		Standard Operating Conditions (unless otherwise stated)									
DC CH		STICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial and $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial and								
			$-40^{\circ}C \leq TA \leq +125^{\circ}C$ for extended								
Param	Sym	Characteristic	Min	Typ†	Max	Units	Conditions				
No.											
D001	Vdd	Supply Voltage	2.5	-	5.5	V	See Figure 13-1 through Figure 13-3				
D002	Vdr	RAM Data Retention Voltage (Note 1)	-	1.5*	-	V	Device in SLEEP mode				
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	-	V	See section on power-on reset for details				
D004	SVDD	VDD rise rate to ensure Power-on Reset	.05*	-	-	V/ms	See section on power-on reset for details				
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared				
D010	IDD	Supply Current (Note 2)	-	1.2	2.0	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled,				
							XT osc mode, (Note 4)*				
			-	_	1.1	mA	FOSC = 4 MHZ, $VDD = 2.5V$, WDT disabled, XT osc mode (Note 4)				
			_	35	70	μA	Fosc = 32 kHz , VDD = 2.5V, WDT disabled,				
						•	LP osc mode				
D020	IPD	Power Down Current (Note 3)	-	-	2.0	μA	VDD = 2.5V				
			-	-	2.2	μA	VDD = 3.0V*				
			-	-	9.0	μA	VDD = 5.5V				
Dooo	Alwor		_	-	10	μΑ					
D022	AIWDT	WDT Current (Note 5)	-	6.0	10	μΑ	VDD=4.0V (125°C)				
D022A	AIBOB	Brown-out Beset Current	_	75	125	μΑ	$\frac{(123)}{BOD}$ enabled, VDD = 5.0V				
	2.001	(Note 5)			0	po t					
D023	Δ ICOMP	Comparator Current for each	-	30	60	μA	VDD = 4.0V				
00004		Comparator (Note 5)		80	105	A	$V_{DD} = 4.0 V_{c}$				
DUZSA		Operating Current	_	80	135	μA mA	$V_{DD} = 4.0V$				
		Operating Current	_		3 1	mA	VCC = 5.5V, SCL = 400 KHZ				
		Standby Current	_		30	uА	$V_{CC} = 3.0V$. EE VDD = VCC				
	ΔIEE	Standby Current	-		100	μA	VCC = 3.0V, EE VDD = VCC				
1A	Fosc	LP Oscillator Operating Frequency	0		200	kHz	All temperatures				
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures				
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures				
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures				

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in k Ω .

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

13.5 <u>Timing Diagrams and Specifications</u>



FIGURE 13-5: EXTERNAL CLOCK TIMING

TABLE 13-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and RC osc mode, VDD=5.0V
		(Note 1)	DC	_	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode, VDD=5.0V
		(Note 1)	0.1	—	4	MHz	XT osc mode
			1	—	20	MHz	HS osc mode
			DC	-	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	—	—	ns	XT and RC osc mode
		(Note 1)	50	—	—	ns	HS osc mode
			5	—	—	μs	LP osc mode
		Oscillator Period	250	_	—	ns	RC osc mode
		(Note 1)	250	—	10,000	ns	XT osc mode
			50	—	1,000	ns	HS osc mode
			5	—	—	μs	LP osc mode
2	TCY	Instruction Cycle Time (Note 1)	200	_	DC	ns	Tcy=Fosc/4
3*	TosL,	External Clock in (OSC1) High or	100*	_	_	ns	XT oscillator, Tosc L/H duty cycle
	TosH	Low Time	2*	—	—	μs	LP oscillator, Tosc L/H duty cycle
			20*	—	—	ns	HS oscillator, Tosc L/H duty cycle
4*	TosR,	External Clock in (OSC1) Rise or	25*	_	_	ns	XT oscillator
	TosF	Fall Time	50*	—	—	ns	LP oscillator
			15*	—	—	ns	HS oscillator

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.66	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	с	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150

Drawing No. C04-072

18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013

Drawing No. C04-051

APPENDIX A: CODE FOR ACCESSING EEPROM DATA MEMORY

Please check our web site at www.microchip.com for code availability.

APPENDIX B:REVISION HISTORY

Revision D (January 2013)

Added a note to each package outline drawing.

NOTES:

Worldwide Sales and Service

AMERICAS

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