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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625-20i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625-20i-so</a>

## 1.0 GENERAL DESCRIPTION

The PIC16CE62X are 18 and 20-Pin EPROM-based members of the versatile PIC® family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers with EEPROM data memory.

All PIC® microcontrollers employ an advanced RISC architecture. The PIC16CE62X family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single-cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CE62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16CE623 and PIC16CE624 have 96 bytes of RAM. The PIC16CE625 has 128 bytes of RAM. Each microcontroller contains a 128x8 EEPROM memory array for storing non-volatile information, such as calibration data or security codes. This memory has an endurance of 1,000,000 erase/write cycles and a retention of 40 plus years.

Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16CE62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low-cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16CE62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV-erasable Cerdip-packaged version is ideal for code development, while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16CE62X mid-range microcontroller families.

A simplified block diagram of the PIC16CE62X is shown in Figure 3-1.

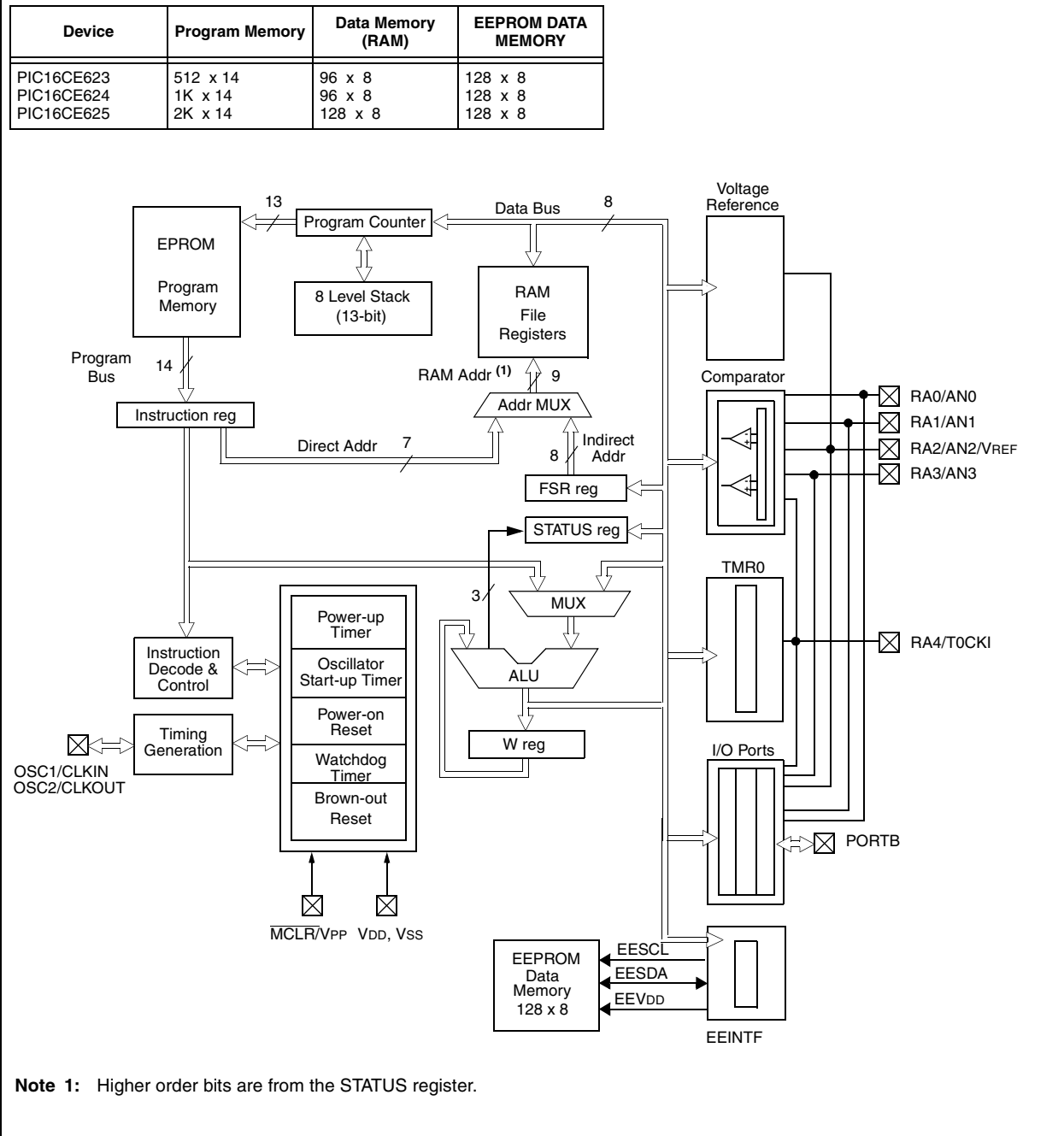
The PIC16CE62X series fits perfectly in applications ranging from multi-pocket battery chargers to low-power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16CE62X very versatile.

### 1.1 Development Support

The PIC16CE62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler is also available.

# PIC16CE62X

FIGURE 3-1: BLOCK DIAGRAM



# PIC16CE62X

## 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The special registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

**TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16CE62X**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other resets <sup>(1)</sup>
<b>Bank 0</b>											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									—	—
08h	Unimplemented									—	—
09h	Unimplemented									—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh-1Eh	Unimplemented									—	—
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
<b>Bank 1</b>											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									—	—
88h	Unimplemented									—	—
89h	Unimplemented									—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBF	0000 000x	0000 000u
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	Unimplemented									—	—
8Eh	PCON	—	—	—	—	—	—	POR	BOD	---- -00x	---- -uuq
8Fh-9Eh	Unimplemented									—	—
90h	EEINTF	—	—	—	—	—	EESCL	EESDA	EEVDD	---- -111	---- -111
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non power-up) resets include  $\overline{MCLR}$  reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

**Note 2:** IRP & RPI bits are reserved; always maintain these bits clear.

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## 4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT (PSA = 1).

### REGISTER 4-2: OPTION REGISTER (ADDRESS 81H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
-n = Value at POR reset  
-x = Unknown at POR reset

bit 7: **RBPU**: PORTB Pull-up Enable bit  
1 = PORTB pull-ups are disabled  
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit  
1 = Interrupt on rising edge of RB0/INT pin  
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit  
1 = Transition on RA4/T0CKI pin  
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit  
1 = Increment on high-to-low transition on RA4/T0CKI pin  
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit  
1 = Prescaler is assigned to the WDT  
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS<2:0>**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

## 4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

### REGISTER 4-3: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit7							bit0
<p>bit 7: <b>GIE:</b> Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts</p> <p>bit 6: <b>PEIE:</b> Peripheral Interrupt Enable bit 1 = Enables all un-masked peripheral interrupts 0 = Disables all peripheral interrupts</p> <p>bit 5: <b>TOIE:</b> TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt</p> <p>bit 4: <b>INTE:</b> RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt</p> <p>bit 3: <b>RBIE:</b> RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt</p> <p>bit 2: <b>TOIF:</b> TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow</p> <p>bit 1: <b>INTF:</b> RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur</p> <p>bit 0: <b>RBIF:</b> RB Port Change Interrupt Flag bit 1 = When at least one of the RB&lt;7:4&gt; pins changed state (must be cleared in software) 0 = None of the RB&lt;7:4&gt; pins have changed state</p>							
<p>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR reset -x = Unknown at POR reset</p>							

## 6.1 Bus Characteristics

In this section, the term “processor” refers to the portion of the PIC16CE62X that interfaces to the EEPROM through software manipulating the EEINTF register. The following **bus protocol** is to be used with the EEPROM data memory.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted by the EEPROM as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 6-1).

### 6.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

### 6.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 6.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

### 6.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the processor and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out fashion.

### 6.1.5 ACKNOWLEDGE

The EEPROM will generate an acknowledge after the reception of each byte. The processor must generate an extra clock pulse which is associated with this acknowledge bit.

<b>Note:</b> Acknowledge bits are not generated if an internal programming cycle is in progress.
--

When the EEPROM acknowledges, it pulls down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. The processor must signal an end of data to the EEPROM by not generating an acknowledge bit on the last byte that has been clocked out of the EEPROM. In this case, the EEPROM must leave the data line HIGH to enable the processor to generate the STOP condition (Figure 6-2).

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NOTES:



## EXAMPLE 9-1: VOLTAGE REFERENCE CONFIGURATION

```

MOVLW    0x02        ; 4 Inputs Muxed
MOVWF    CMCON        ; to 2 comps.
BSF      STATUS,RP0   ; go to Bank 1
MOVLW    0x07        ; RA3-RA0 are
MOVWF    TRISA        ; outputs
MOVLW    0xA6        ; enable VREF
MOVWF    VRCON        ; low range
                        ; set VR<3:0>=6

BCF      STATUS,RP0   ; go to Bank 0
CALL     DELAY10      ; 10µs delay
    
```

### 9.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 9-1) keep VREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The absolute accuracy of the Voltage Reference can be found in Table 13-2.

### 9.3 Operation During Sleep

When the device wakes up from sleep through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the Voltage Reference should be disabled.

### 9.4 Effects of a Reset

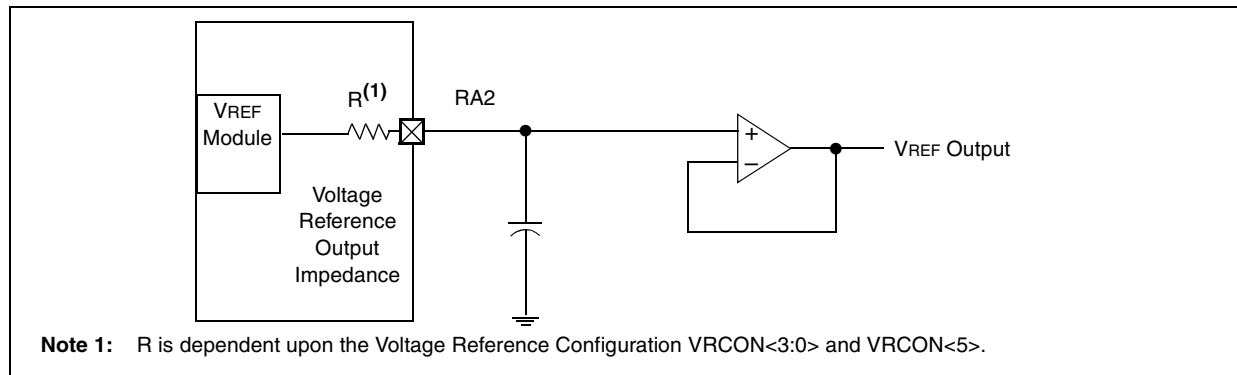
A device reset disables the Voltage Reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

### 9.5 Connection Considerations

The Voltage Reference Module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the Voltage Reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the Voltage Reference output for external connections to VREF. Figure 9-2 shows an example buffering technique.

**FIGURE 9-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE**



**TABLE 9-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR / BOD	Value On All Other Resets
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: - = Unimplemented, read as "0"

## CLRWDT Clear Watchdog Timer

Syntax:	[ <i>label</i> ] CLRWDT				
Operands:	None				
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$				
Status Affected:	$\overline{TO}$ , $\overline{PD}$				
Encoding:	<table border="1"><tr><td>00</td><td>0000</td><td>0110</td><td>0100</td></tr></table>	00	0000	0110	0100
00	0000	0110	0100		
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.				
Words:	1				
Cycles:	1				
Example	CLRWDT				

Before Instruction  
WDT counter = ?

After Instruction  
WDT counter = 0x00  
WDT prescaler = 0  
 $\overline{TO}$  = 1  
 $\overline{PD}$  = 1

## COMF Complement f

Syntax:	[ <i>label</i> ] COMF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	$(\bar{f}) \rightarrow (\text{dest})$			
Status Affected:	Z			
Encoding:	00	1001	dfff	ffff
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	COMF REG1, 0			

Before Instruction  
REG1 = 0x13

After Instruction  
REG1 = 0x13  
W = 0xEC

## DECf Decrement f

Syntax:	[ <i>label</i> ] DECf f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(f) - 1 $\rightarrow$ (dest)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>00</td><td>0011</td><td>dfff</td><td>ffff</td></tr></table>	00	0011	dfff	ffff
00	0011	dfff	ffff		
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	DECf CNT, 1				

Before Instruction  
CNT = 0x01  
Z = 0

After Instruction  
CNT = 0x00  
Z = 1

## DECFSZ Decrement f, Skip if 0

Syntax:	[ <i>label</i> ] DECFSZ f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(f) - 1 $\rightarrow$ (dest); skip if result = 0				
Status Affected:	None				
Encoding:	<table border="1"><tr><td>00</td><td>1011</td><td>dfff</td><td>ffff</td></tr></table>	00	1011	dfff	ffff
00	1011	dfff	ffff		
Description:	<p>The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.</p>				

Before Instruction  
PC = address HERE

After Instruction  
CNT = CNT - 1  
if CNT = 0,  
PC = address CONTINUE  
if CNT ≠ 0,  
PC = address HERE+1

IORWF		Inclusive OR W with f							
Syntax:	[ <i>label</i> ] IORWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	(W) .OR. (f) $\rightarrow$ (dest)								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>00</td><td>0100</td><td>dfff</td><td>ffff</td></tr></table>					00	0100	dfff	ffff
00	0100	dfff	ffff						
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.								
Words:	1								
Cycles:	1								
Example	IORWF                      RESULT, 0								
	Before Instruction								
	RESULT = 0x13								
	W = 0x91								
	After Instruction								
	RESULT = 0x13								
	W = 0x93								
	Z = 1								

MOVLW	Move Literal to W				
Syntax:	[ <i>label</i> ] MOVLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$k \rightarrow (W)$				
Status Affected:	None				
Encoding:	<table><tr><td>11</td><td>00xx</td><td>kkkk</td><td>kkkk</td></tr></table>	11	00xx	kkkk	kkkk
11	00xx	kkkk	kkkk		
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.				
Words:	1				
Cycles:	1				
Example	<pre>MOVLW      0x5A</pre> <p>After Instruction</p> <p>W = 0x5A</p>				

MOVf		Move f							
Syntax:	[ <i>label</i> ] MOVf f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	(f) → (dest)								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>00</td><td>1000</td><td>dfff</td><td>ffff</td></tr></table>					00	1000	dfff	ffff
00	1000	dfff	ffff						
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.								
Words:	1								
Cycles:	1								
Example	MOVf FSR, 0								
After Instruction									
W = value in FSR register									
Z = 1									

MOVWF		Move W to f							
Syntax:	[ <i>label</i> ] MOVWF f								
Operands:	$0 \leq f \leq 127$								
Operation:	(W) → (f)								
Status Affected:	None								
Encoding:	<table><tr><td>00</td><td>0000</td><td>1fff</td><td>ffff</td></tr></table>					00	0000	1fff	ffff
00	0000	1fff	ffff						
Description:	Move data from W register to register 'f'.								
Words:	1								
Cycles:	1								
Example	MOVWF OPTION								
	Before Instruction								
	OPTION = 0xFF								
	W = 0x4F								
	After Instruction								
	OPTION = 0x4F								
	W = 0x4F								

# PIC16CE62X

## RETURN Return from Subroutine

Syntax: [ *label* ] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Encoding: 

00	0000	0000	1000
----	------	------	------

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Example  
RETURN  
After Interrupt  
PC = TOS

## RRF Rotate Right f through Carry

Syntax: [ *label* ] RRF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

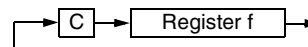
Operation: See description below

Status Affected: C

Encoding: 

00	1100	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example RRF REG1, 0

Before Instruction

REG1 = 1110 0110  
C = 0

After Instruction

REG1 = 1110 0110  
W = 0111 0011  
C = 0

## RLF Rotate Left f through Carry

Syntax: [ *label* ] RLF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

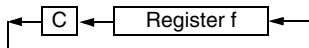
Operation: See description below

Status Affected: C

Encoding: 

00	1101	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example RLF REG1, 0  
Before Instruction  
REG1 = 1110 0110  
C = 0  
After Instruction  
REG1 = 1110 0110  
W = 1100 1100  
C = 1

## SLEEP

Syntax: [ *label* ] SLEEP

Operands: None

Operation: 00h → WDT,  
0 → WDT prescaler,  
1 →  $\overline{\text{TO}}$ ,  
0 →  $\overline{\text{PD}}$

Status Affected:  $\overline{\text{TO}}$ ,  $\overline{\text{PD}}$

Encoding: 

00	0000	0110	0011
----	------	------	------

Description: The power-down status bit,  $\overline{\text{PD}}$  is cleared. Time-out status bit,  $\overline{\text{TO}}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 10.8 for more details.

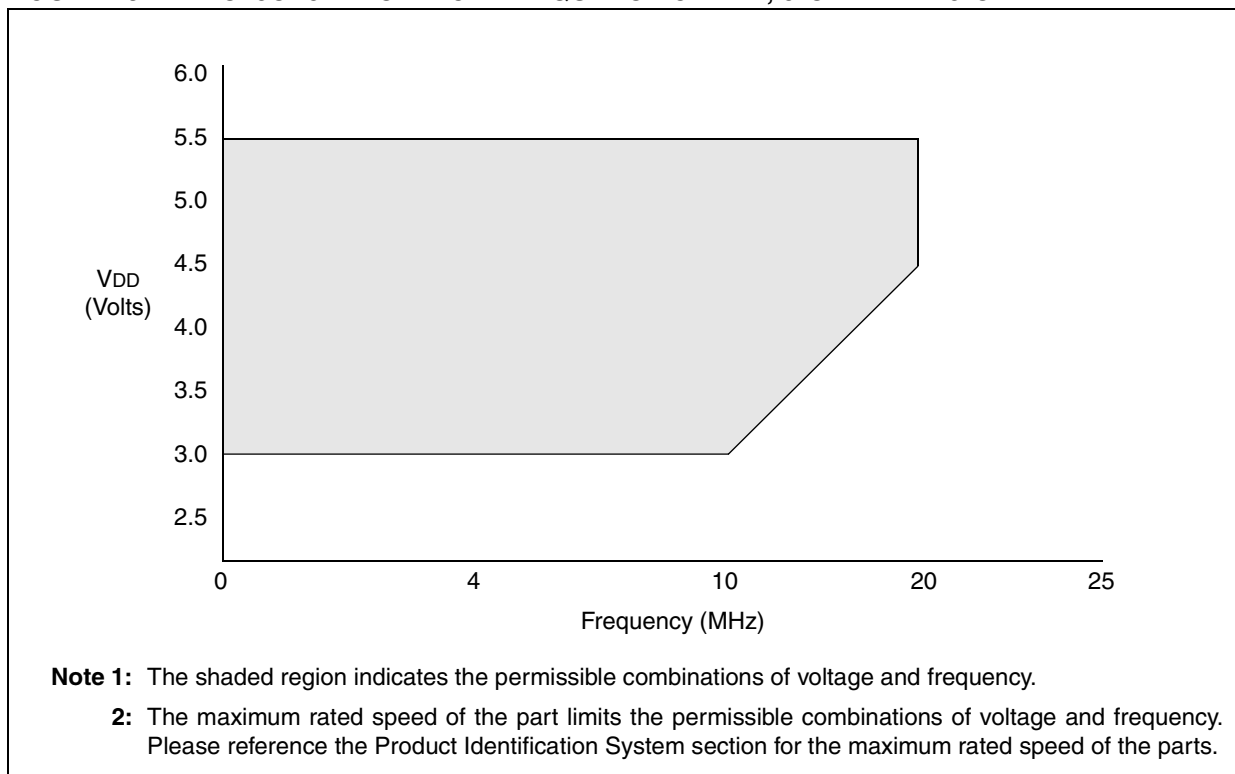
Words: 1

Cycles: 1

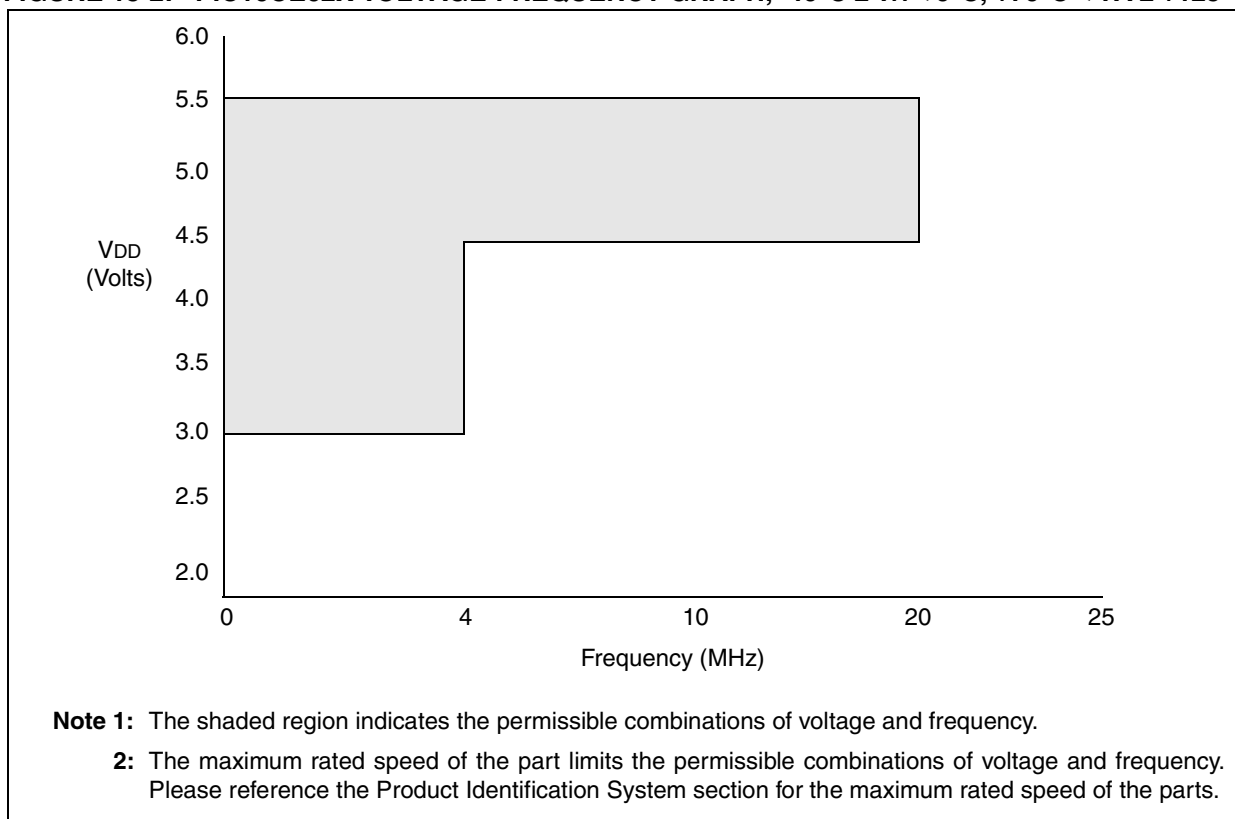
Example: SLEEP

# PIC16CE62X

**FIGURE 13-1: PIC16CE62X VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 13-2: PIC16CE62X VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A < 0^{\circ}\text{C}$ ,  $+70^{\circ}\text{C} < T_A \leq +125^{\circ}\text{C}$**



# PIC16CE62X

## 13.1 DC CHARACTERISTICS:

PIC16CE62X-04 (Commercial, Industrial, Extended)

PIC16CE62X-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature				
			-40°C ≤ TA ≤ +85°C for industrial and				
			0°C ≤ TA ≤ +70°C for commercial and				
			-40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	—	5.5	V	See Figure 13-1 through Figure 13-3
D002	VDR	RAM Data Retention Voltage (Note 1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on power-on reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D010	IDD	Supply Current (Note 2, 4)	—	1.2	2.0	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT osc mode, (Note 4)*
			—	0.4	1.2	mA	FOSC = 4 MHz, VDD = 3.0V, WDT disabled, XT osc mode, (Note 4)
			—	1.0	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, WDT disabled, HS osc mode, (Note 6)
			—	4.0	6.0	mA	FOSC = 20 MHz, VDD = 4.5V, WDT disabled, HS osc mode
			—	4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WDT disabled*, HS osc mode
			—	35	70	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP osc mode
D020	IPD	Power Down Current (Note 3)	—	—	2.2	μA	VDD = 3.0V
			—	—	5.0	μA	VDD = 4.5V*
			—	—	9.0	μA	VDD = 5.5V
			—	—	15	μA	VDD = 5.5V Extended
D022	ΔI <sub>WDT</sub>	WDT Current (Note 5)	—	6.0	10	μA	VDD = 4.0V (125°C)
D022A	ΔI <sub>BOR</sub>	Brown-out Reset Current (Note 5)	—	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔI <sub>COMP</sub>	Comparator Current for each Comparator (Note 5)	—	30	60	μA	VDD = 4.0V
D023A	ΔI <sub>VREF</sub>	VREF Current (Note 5)	—	80	135	μA	VDD = 4.0V
	ΔI <sub>EE Write</sub>	Operating Current	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ΔI <sub>EE Read</sub>	Operating Current	—	—	1	mA	
	ΔI <sub>EE</sub>	Standby Current	—	—	30	μA	VCC = 3.0V, EE VDD = VCC
	ΔI <sub>EE</sub>	Standby Current	—	—	100	μA	VCC = 3.0V, EE VDD = VCC
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = VDD/2R_{ext}$  (mA) with Rext in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

## 13.2 DC CHARACTERISTICS: PIC16LCE62X-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature				
			$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.5	—	5.5	V	See Figure 13-1 through Figure 13-3
D002	VDR	RAM Data Retention Voltage (Note 1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	.05*	—	—	V/ms	See section on power-on reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D010	IDD	Supply Current (Note 2)	—	1.2	2.0	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT osc mode, (Note 4)*
			—	—	1.1	mA	FOSC = 4 MHz, VDD = 2.5V, WDT disabled, XT osc mode, (Note 4)
			—	35	70	μA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP osc mode
D020	IPD	Power Down Current (Note 3)	—	—	2.0	μA	VDD = 2.5V
			—	—	2.2	μA	VDD = 3.0V*
			—	—	9.0	μA	VDD = 5.5V
			—	—	15	μA	VDD = 5.5V Extended
D022	ΔIWD	WDT Current (Note 5)	—	6.0	10	μA	VDD=4.0V (125°C)
D022A	ΔIBOR	Brown-out Reset Current (Note 5)	—	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator (Note 5)	—	30	60	μA	VDD = 4.0V
D023A	ΔIVREF	VREF Current (Note 5)	—	80	135	μA	VDD = 4.0V
	ΔIEE Write	Operating Current	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ΔIEE Read	Operating Current	—	—	1	mA	
	ΔIEE	Standby Current	—	—	30	μA	VCC = 3.0V, EE VDD = VCC
	ΔIEE	Standby Current	—	—	100	μA	VCC = 3.0V, EE VDD = VCC
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

# PIC16CE62X

## 13.3 DC CHARACTERISTICS:

**PIC16CE62X-04 (Commercial, Industrial, Extended)**  
**PIC16CE62X-20 (Commercial, Industrial, Extended)**  
**PIC16LCE62X (Commercial, Industrial)**

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended				
			Operating voltage $\text{VDD}$ range as described in DC spec Table 13-1				
Parm No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	VIL	<b>Input Low Voltage</b> I/O ports with TTL buffer	VSS	–	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V, Otherwise
D031		with Schmitt Trigger input	VSS	–	0.2VDD	V	
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	VSS	–	0.2VDD	V	Note1
D033		OSC1 (in XT and HS)	VSS	–	0.3VDD	V	
		OSC1 (in LP)	VSS	–	0.6VDD - 1.0	V	
D040	VIH	<b>Input High Voltage</b> I/O ports with TTL buffer	2.0V .25VDD + 0.8V	–	VDD VDD	V	VDD = 4.5V to 5.5V, Otherwise
D041		with Schmitt Trigger input	0.8VDD	–	VDD	V	
D042		MCLR RA4/T0CKI	0.8VDD	–	VDD	V	
D043		OSC1 (XT, HS and LP)	0.7VDD	–	VDD	V	
D043A		OSC1 (in RC mode)	0.9VDD	–			Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS
D060	IIL	<b>Input Leakage Current</b> (Notes 2, 3) I/O ports (Except PORTA)	–	–	±1.0	μA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D061		PORTA	–	–	±0.5	μA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D063		RA4/T0CKI	–	–	±1.0	μA	VSS ≤ VPIN ≤ VDD
		OSC1, MCLR	–	–	±5.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
D080	VOL	<b>Output Low Voltage</b> I/O ports	–	–	0.6	V	IOL=8.5 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			–	–	0.6	V	IOL=7.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	–	–	0.6	V	IOL=1.6 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			–	–	0.6	V	IOL=1.2 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D090	VOH	<b>Output High Voltage</b> (Note 3) I/O ports (Except RA4)	VDD-0.7	–	–	V	IOH=-3.0 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			VDD-0.7	–	–	V	IOH=-2.5 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D092		OSC2/CLKOUT (RC only)	VDD-0.7	–	–	V	IOH=-1.3 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			VDD-0.7	–	–	V	IOH=-1.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$
*D150	VOD	<b>Open-Drain High Voltage</b>			8.5	V	RA4 pin
D100	COSC2	<b>Capacitive Loading Specs on Output Pins</b> OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	Cio	All I/O pins/OSC2 (in RC mode)			50	pF	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16CE62X be driven with external clock in RC mode.

**2:** The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.



# PIC16CE62X

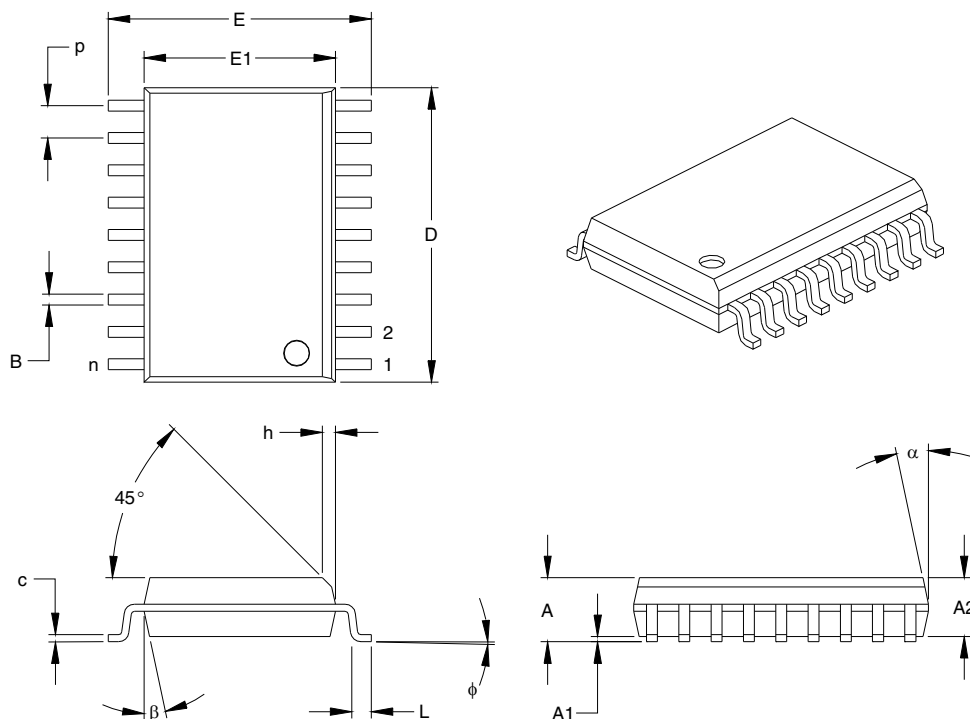
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NOTES:

# PIC16CE62X

## 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	P		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
JEDEC Equivalent: MS-013  
Drawing No. C04-051

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NOTES: