

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625t-04i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16ce625t-04i-so</a>

## 4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-7Fh (Bank0) on the PIC16CE623/624 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16CE625 are General Purpose Registers implemented as static RAM. Some special purpose registers are mapped in Bank 1. In all three microcontrollers, address space F0h-FFh (Bank1) is mapped to 70-7Fh (Bank0) as common RAM.

### 4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 96 x 8 in the PIC16CE623/624 and 128 x 8 in the PIC16CE625. Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

# PIC16CE62X

## 4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT (PSA = 1).

### REGISTER 4-2: OPTION REGISTER (ADDRESS 81H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0
<div><div>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR reset -x = Unknown at POR reset</div></div>							
bit 7:	<b>RBPU</b> : PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values						
bit 6:	<b>INTEDG</b> : Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin						
bit 5:	<b>T0CS</b> : TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)						
bit 4:	<b>T0SE</b> : TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin						
bit 3:	<b>PSA</b> : Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module						
bit 2-0:	<b>PS&lt;2:0&gt;</b> : Prescaler Rate Select bits						
	Bit Value	TMR0 Rate	WDT Rate				
	000	1 : 2	1 : 1				
	001	1 : 4	1 : 2				
	010	1 : 8	1 : 4				
	011	1 : 16	1 : 8				
	100	1 : 32	1 : 16				
	101	1 : 64	1 : 32				
	110	1 : 128	1 : 64				
	111	1 : 256	1 : 128				

## 4.2.2.6 PCON REGISTER

The PCON register contains flag bits to differentiate between a Power-on Reset, an external  $\overline{\text{MCLR}}$  reset, WDT reset or a Brown-out Reset.

**Note:**  $\overline{\text{BOD}}$  is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if  $\overline{\text{BOD}}$  is cleared, indicating a brown-out has occurred. The  $\overline{\text{BOD}}$  status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by programming BODEN bit in the configuration word).

### REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	POR	$\overline{\text{BOD}}$
bit7						bit0	

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **POR:** Power-on Reset Status bit  
 1 = No Power-on Reset occurred  
 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0:  **$\overline{\text{BOD}}$ :** Brown-out Reset Status bit  
 1 = No Brown-out Reset occurred  
 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

R = Readable bit  
 W = Writable bit  
 U = Unimplemented bit, read as '0'  
 -n = Value at POR reset  
 -x = Unknown at POR reset

## 4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-7. However, IRP is not used in the PIC16CE62X.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-1.

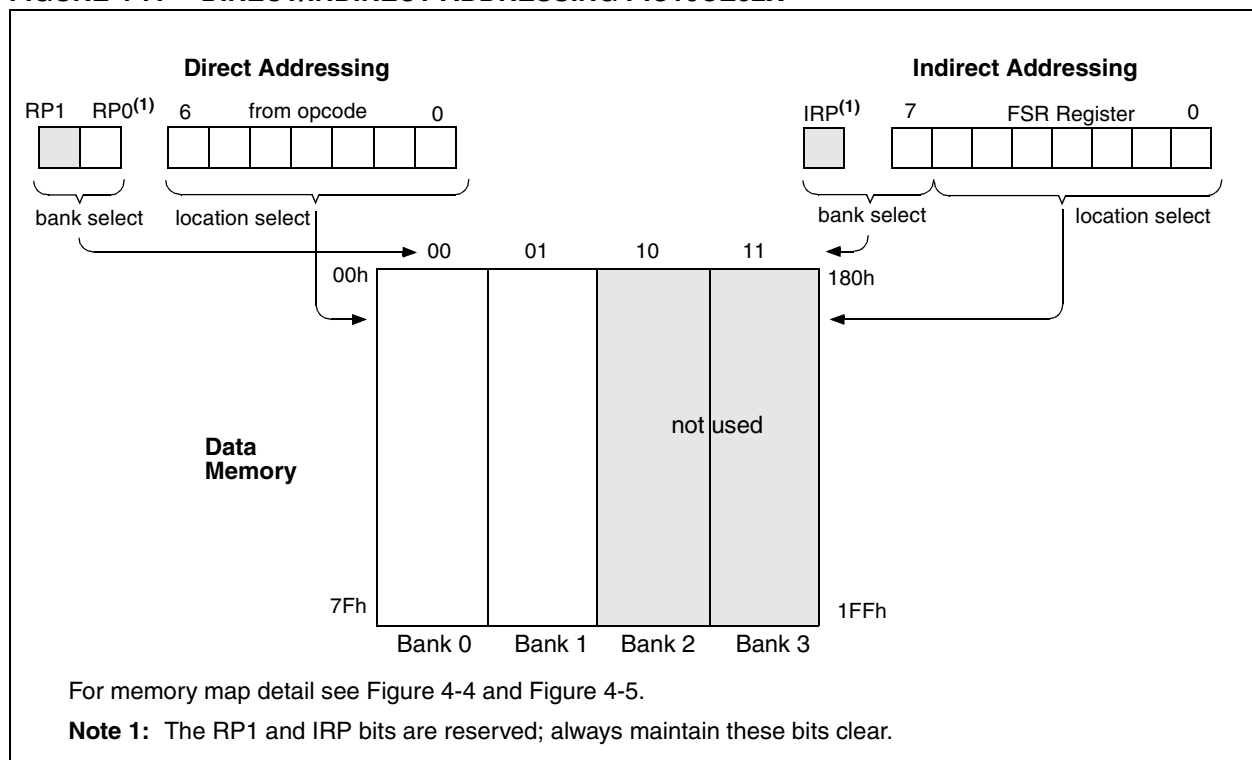
### EXAMPLE 4-1: INDIRECT ADDRESSING

```

movlw 0x20    ;initialize pointer
movwf FSR     ;to RAM
NEXT         clrfs INDF ;clear INDF register
             incf FSR   ;inc pointer
             btfss FSR,4 ;all done?
             goto NEXT ;no clear next
                     ;yes continue
CONTINUE:

```

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING PIC16CE62X



## 6.3 Write Operations

### 6.3.1 BYTE WRITE

Following the start signal from the processor, the device code (4 bits), the don't care bits (3 bits), and the R/W bit, which is a logic low, is placed onto the bus by the processor. This indicates to the EEPROM that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the processor is the word address and will be written into the address pointer of the EEPROM. After receiving another acknowledge signal from the EEPROM, the processor will transmit the data word to be written into the addressed memory location. The EEPROM acknowledges again and the processor generates a stop condition. This initiates the internal write cycle, and during this time, the EEPROM will not generate acknowledge signals (Figure 6-5).

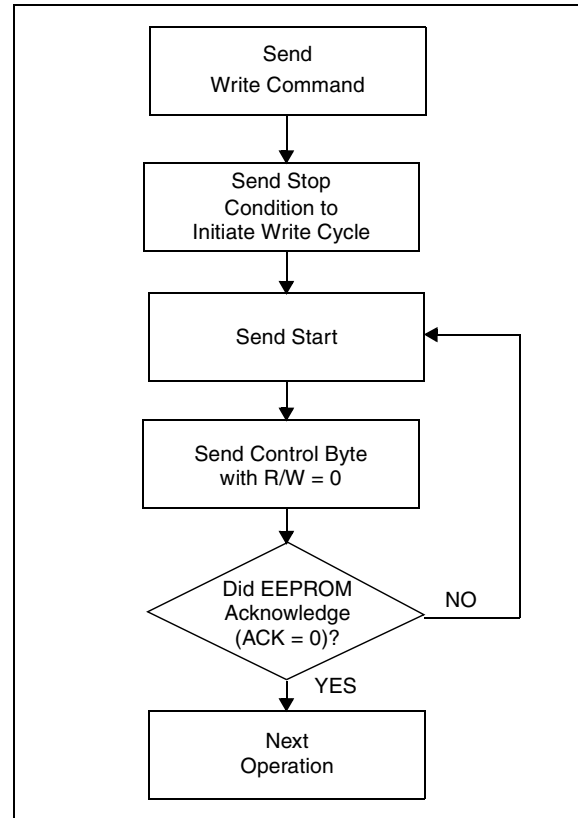
### 6.3.2 PAGE WRITE

The write control byte, word address and the first data byte are transmitted to the EEPROM in the same way as in a byte write. But instead of generating a stop condition, the processor transmits up to eight data bytes to the EEPROM, which are temporarily stored in the on-chip page buffer and will be written into the memory after the processor has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the processor should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-6).

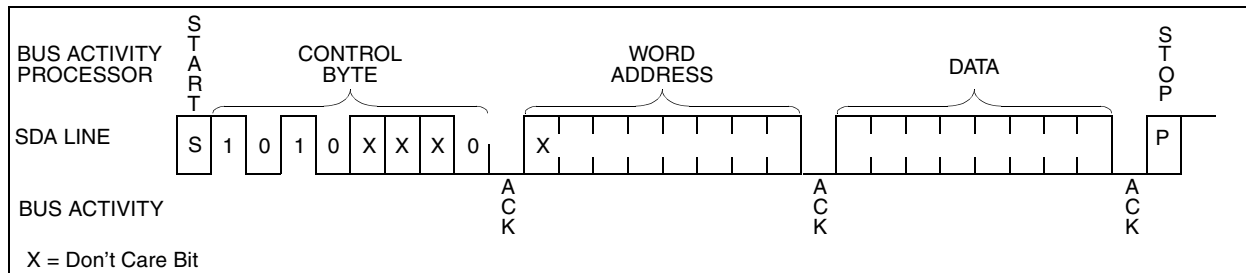
## 6.4 Acknowledge Polling

Since the EEPROM will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the processor, the EEPROM initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the processor sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the processor can then proceed with the next read or write command. See Figure 6-4 for flow diagram.

**FIGURE 6-4: ACKNOWLEDGE POLLING FLOW**



**FIGURE 6-5: BYTE WRITE**



## 8.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

**Note:** If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of CMCON. This will end the mismatch condition.
- Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

## 8.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will

wake-up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

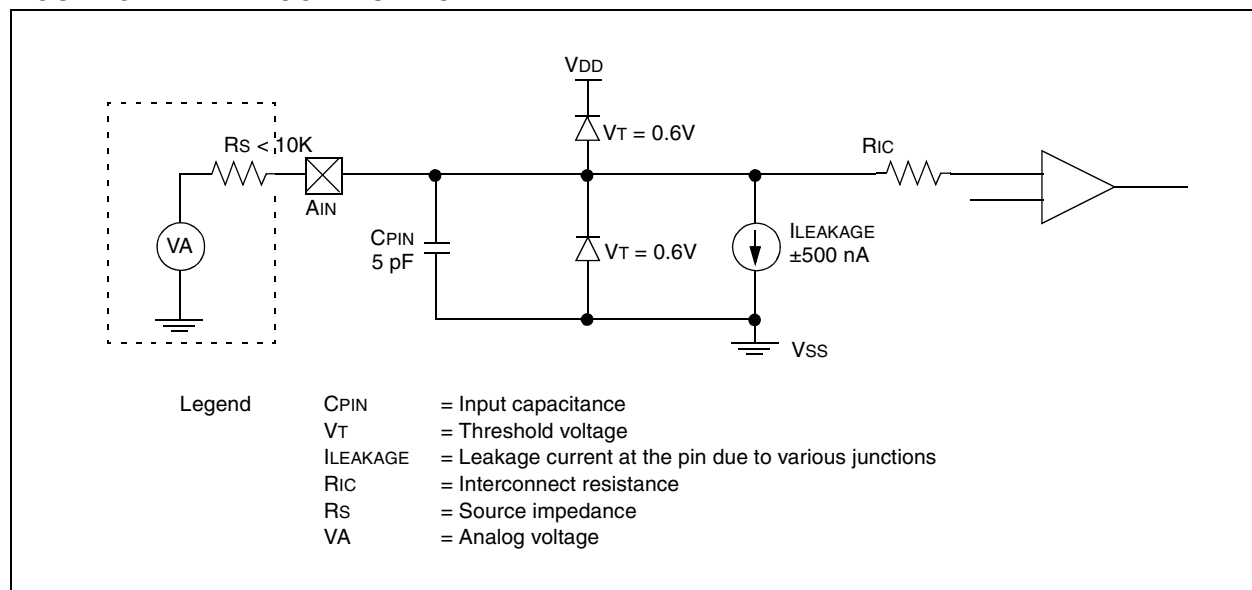
## 8.8 Effects of a RESET

A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

## 8.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 8-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

**FIGURE 8-4: ANALOG INPUT MODEL**



## 10.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 10-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

**FIGURE 10-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT**

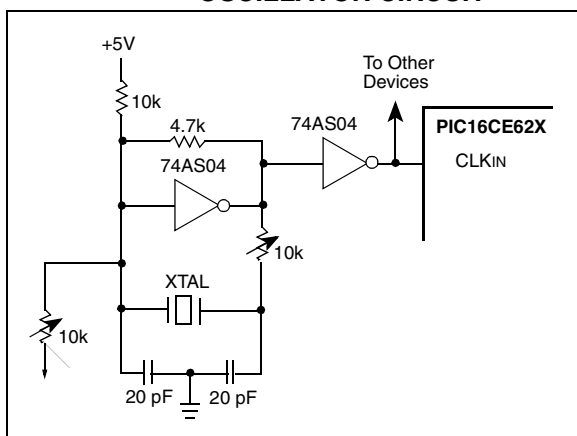
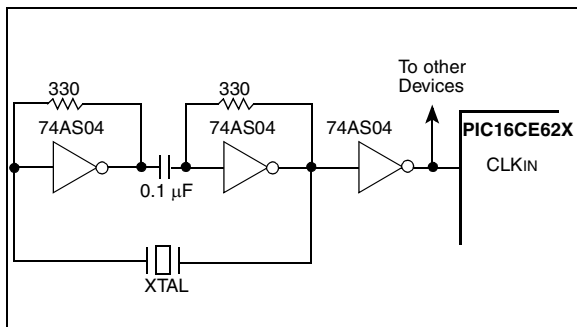


Figure 10-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

**FIGURE 10-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT**



## 10.2.4 RC OSCILLATOR

For timing insensitive applications the “RC” device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor ( $R_{ext}$ ) and capacitor ( $C_{ext}$ ) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low  $C_{ext}$  values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 10-5 shows how the R/C combination is connected to the PIC16CE62X. For  $R_{ext}$  values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high  $R_{ext}$  values (i.e., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep  $R_{ext}$  between 3 kΩ and 100 kΩ.

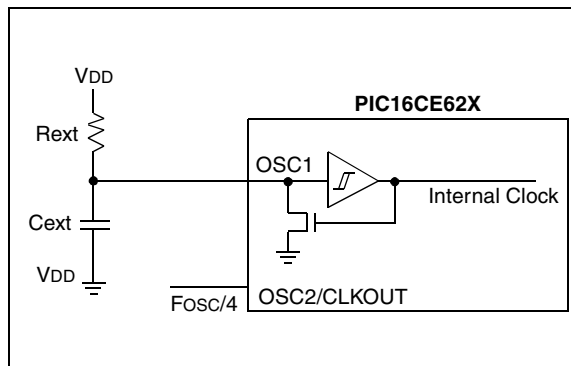
Although the oscillator will operate with no external capacitor ( $C_{ext} = 0$  pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 14.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 14.0 for variation of oscillator frequency due to  $V_{DD}$  for given  $R_{ext}/C_{ext}$  values, as well as frequency variation due to operating temperature for given R, C, and  $V_{DD}$  values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

**FIGURE 10-5: RC OSCILLATOR MODE**





## 10.3 Reset

The PIC16CE62X differentiates between various kinds of reset:

- Power-on reset (POR)
- $\overline{\text{MCLR}}$  reset during normal operation
- $\overline{\text{MCLR}}$  reset during SLEEP
- WDT reset (normal operation)
- WDT wake-up (SLEEP)
- Brown-out Reset (BOD)

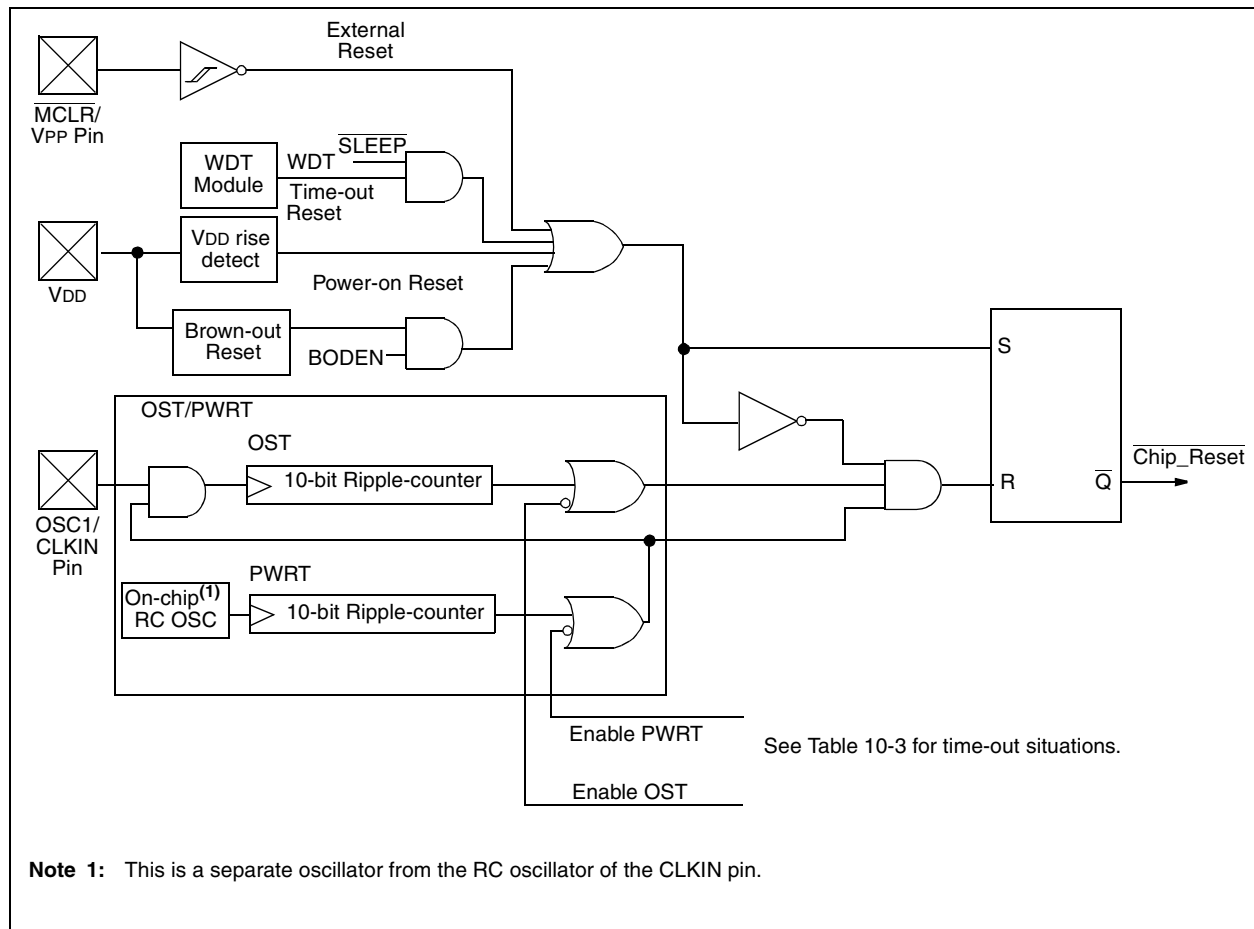
Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset

state" on Power-on reset,  $\overline{\text{MCLR}}$  reset, WDT reset and  $\overline{\text{MCLR}}$  reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation.  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different reset situations as indicated in Table 10-4. These bits are used in software to determine the nature of the reset. See Table 10-6 for a full description of reset states of all registers.

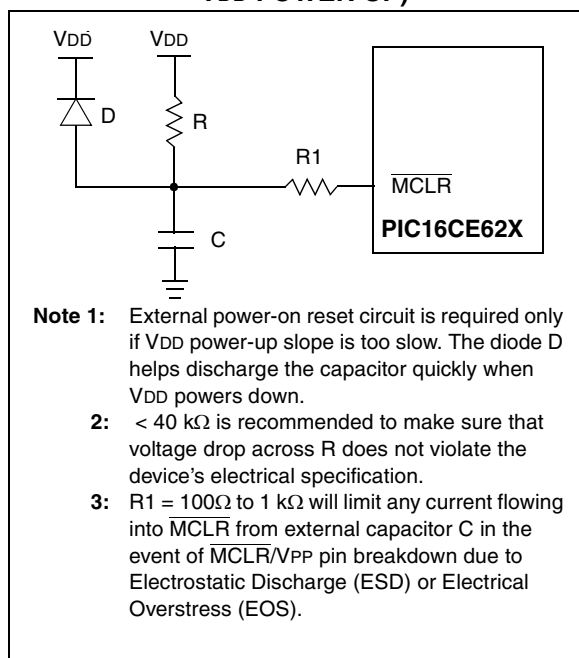
A simplified block diagram of the on-chip reset circuit is shown in Figure 10-6.

The  $\overline{\text{MCLR}}$  reset path has a noise filter to detect and ignore small pulses. See Table 13-5 for pulse width specification.

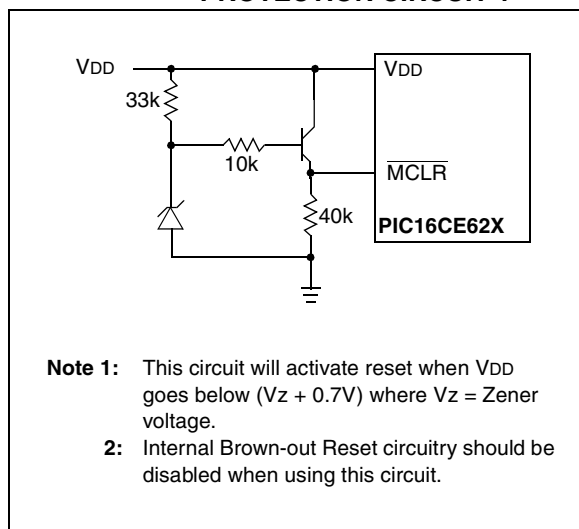
**FIGURE 10-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



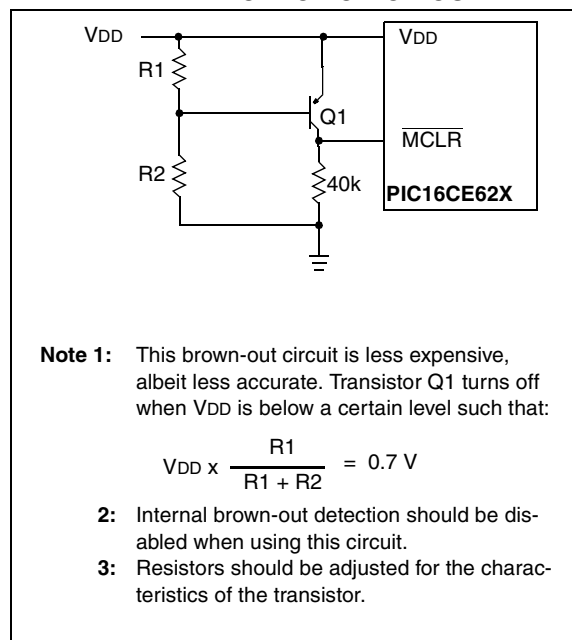
**FIGURE 10-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V<sub>DD</sub> POWER-UP)**



**FIGURE 10-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1**



**FIGURE 10-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2**



**FIGURE 10-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3**

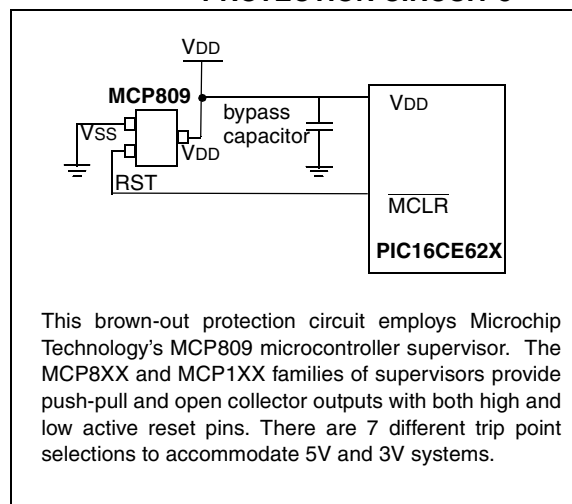


FIGURE 10-17: WATCHDOG TIMER BLOCK DIAGRAM

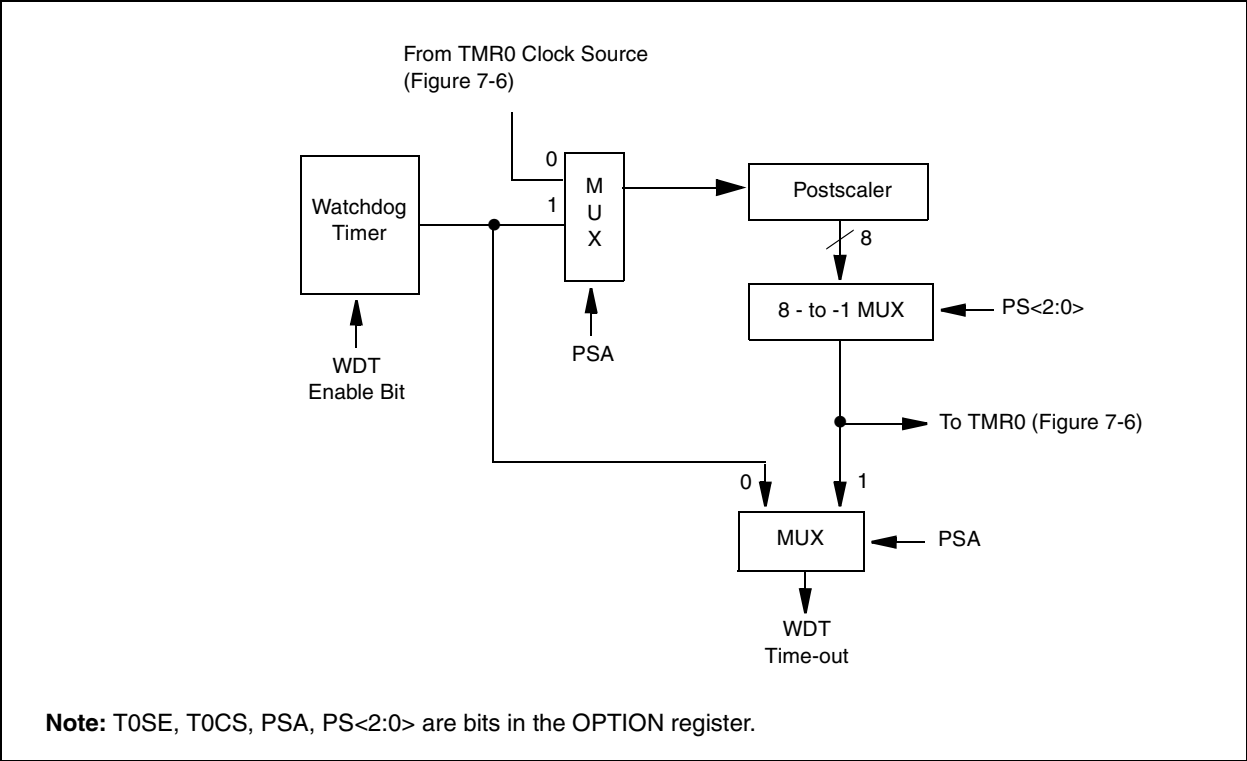


FIGURE 10-18: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	—	BOREN	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
81h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: – = Unimplemented location, read as “0”, + = Reserved for future use

**Note:** Shaded cells are not used by the Watchdog Timer.

## BTFSS Bit Test f, Skip if Set

Syntax: [ *label* ] BTFSS *f*,*b*

Operands:  $0 \leq f \leq 127$   
 $0 \leq b < 7$

Operation: skip if (*f*<*b*>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff
----	------	------	------

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.  
 If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example

```

HERE    BTFSS  FLAG, 1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
  
```

Before Instruction

PC = address HERE

After Instruction

```

if FLAG<1> = 0,
PC = address FALSE
if FLAG<1> = 1,
PC = address TRUE
  
```

## CALL Call Subroutine

Syntax: [ *label* ] CALL *k*

Operands:  $0 \leq k \leq 2047$

Operation: (PC)+ 1 → TOS,  
*k* → PC<10:0>,  
 (PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk
----	------	------	------

Description: Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example

```

HERE    CALL   THERE
  
```

Before Instruction

PC = Address HERE

After Instruction

```

PC = Address THERE
TOS = Address HERE+1
  
```

## CLRF Clear f

Syntax: [ *label* ] CLRF *f*

Operands:  $0 \leq f \leq 127$

Operation: 00h → (*f*)  
 1 → Z

Status Affected: Z

Encoding:

00	0001	1fff	ffff
----	------	------	------

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example

```

CLRF    FLAG_REG
  
```

Before Instruction

FLAG\_REG = 0x5A

After Instruction

```

FLAG_REG = 0x00
Z        = 1
  
```

## CLRW Clear W

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W)  
 1 → Z

Status Affected: Z

Encoding:

00	0001	0000	0011
----	------	------	------

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example

```

CLRW
  
```

Before Instruction

W = 0x5A

After Instruction

```

W = 0x00
Z = 1
  
```

GOTO		Unconditional Branch							
Syntax:	[ <i>label</i> ] GOTO k								
Operands:	$0 \leq k \leq 2047$								
Operation:	$k \rightarrow PC<10:0>$ $PCLATH<4:3> \rightarrow PC<12:11>$								
Status Affected:	None								
Encoding:	<table><tr><td>10</td><td>1kkk</td><td>kkkk</td><td>kkkk</td></tr></table>					10	1kkk	kkkk	kkkk
10	1kkk	kkkk	kkkk						
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.								
Words:	1								
Cycles:	2								
Example	GOTO THERE								
	After Instruction								
	PC = Address THERE								

INCFSZ		Increment f, Skip if 0						
Syntax:	[ <i>label</i> ] INCFSZ f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	$(f) + 1 \rightarrow (\text{dest})$ , skip if result = 0							
Status Affected:	None							
Encoding:	<table border="1"><tr><td>00</td><td>1111</td><td>dfff</td><td>ffff</td></tr></table>				00	1111	dfff	ffff
00	1111	dfff	ffff					
Description:	<p>The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.</p>							
Words:	1							
Cycles:	1(2)							
Example	HERE INCFSZ CNT, 1							

Before Instruction  
 PC = address HERE  
 After Instruction  
 CNT = CNT + 1  
 if CNT= 0,  
 PC = address CONTINUE  
 if CNT≠ 0,  
 PC = address HERE +1

INCF		Increment f								
Syntax:	[ <i>label</i> ] INCF f,d									
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$									
Operation:	$(f) + 1 \rightarrow (\text{dest})$									
Status Affected:	Z									
Encoding:	<table><tr><td>00</td><td>1010</td><td>dfff</td><td>ffff</td></tr></table>						00	1010	dfff	ffff
00	1010	dfff	ffff							
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.									
Words:	1									
Cycles:	1									
Example	INCF CNT, 1									
	Before Instruction									
	CNT	=	0xFF							
	Z	=	0							
	After Instruction									
	CNT	=	0x00							
	Z	=	1							

IORLW		Inclusive OR Literal with W						
Syntax:	[ <i>label</i> ] IORLW k							
Operands:	$0 \leq k \leq 255$							
Operation:	$(W) .OR. k \rightarrow (W)$							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>11</td><td>1000</td><td>kkkk</td><td>kkkk</td></tr></table>				11	1000	kkkk	kkkk
11	1000	kkkk	kkkk					
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.							
Words:	1							
Cycles:	1							
Example	IORLW 0x35							
	Before Instruction							
	W = 0x9A							
	After Instruction							
	W = 0xBF							
	Z = 1							

## SUBLW Subtract W from Literal

Syntax: [ *label* ] SUBLW *k*

Operands:  $0 \leq k \leq 255$

Operation:  $k - (W) \rightarrow (W)$

Status C, DC, Z

Affected:

Encoding:

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1: SUBLW 0x02

Before Instruction

W = 1  
C = ?

After Instruction

W = 1  
C = 1; result is positive

Example 2: Before Instruction

W = 2  
C = ?

After Instruction

W = 0  
C = 1; result is zero

Example 3: Before Instruction

W = 3  
C = ?

After Instruction

W = 0xFF  
C = 0; result is negative

## SUBWF Subtract W from f

Syntax: [ *label* ] SUBWF *f,d*

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(f) - (W) \rightarrow (\text{dest})$

Status

C, DC, Z

Affected:

Encoding:

00	0010	dfff	ffff
----	------	------	------

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1, 1

Before Instruction

REG1 = 3  
W = 2  
C = ?

After Instruction

REG1 = 1  
W = 2  
C = 1; result is positive

Example 2: Before Instruction

REG1 = 2  
W = 2  
C = ?

After Instruction

REG1 = 0  
W = 2  
C = 1; result is zero

Example 3: Before Instruction

REG1 = 1  
W = 2  
C = ?

After Instruction

REG1 = 0xFF  
W = 2  
C = 0; result is negative

## 12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER®/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - SIMICE
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - SEEVAL®
  - KEELOQ®

### 12.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

### 12.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PIC MCUs. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

### 12.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

### 12.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with pre-compiled libraries using directives from a linker script.

and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

## **12.17 SEEVAL Evaluation and Programming System**

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

## **12.18 KEELOQ Evaluation and Programming Tools**

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.



## 13.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings †

Ambient Temperature under bias .....	-40° to +125°C
Storage Temperature .....	-65° to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$ ).....	-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS .....	0 to +7.0V
Voltage on RA4 with respect to VSS.....	8.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS (Note 2).....	0 to +14V
Voltage on RA4 with respect to VSS.....	8.5V
Total power Dissipation (Note 1) .....	1.0W
Maximum Current out of VSS pin.....	300 mA
Maximum Current into VDD pin .....	250 mA
Input Clamp Current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD) .....	±20 mA
Output Clamp Current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD).....	±20 mA
Maximum Output Current sunk by any I/O pin .....	25 mA
Maximum Output Current sourced by any I/O pin.....	25 mA
Maximum Current sunk by PORTA and PORTB .....	200 mA
Maximum Current sourced by PORTA and PORTB .....	200 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

**2:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 $\Omega$  should be used when applying a "low" level to the  $\overline{\text{MCLR}}$  pin rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC16CE62X

## 13.3 DC CHARACTERISTICS:

**PIC16CE62X-04 (Commercial, Industrial, Extended)**  
**PIC16CE62X-20 (Commercial, Industrial, Extended)**  
**PIC16LCE62X (Commercial, Industrial)**

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended				
			Operating voltage $\text{VDD}$ range as described in DC spec Table 13-1				
Parm No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	VIL	<b>Input Low Voltage</b> I/O ports with TTL buffer	VSS	–	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V, Otherwise
D031		with Schmitt Trigger input	VSS		0.2VDD	V	
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	VSS	–	0.2VDD	V	Note1
D033		OSC1 (in XT and HS)	VSS	–	0.3VDD	V	
		OSC1 (in LP)	VSS	–	0.6VDD - 1.0	V	
D040	VIH	<b>Input High Voltage</b> I/O ports with TTL buffer	2.0V .25VDD + 0.8V	–	VDD VDD	V	VDD = 4.5V to 5.5V, Otherwise
D041		with Schmitt Trigger input	0.8VDD		VDD	V	
D042		MCLR RA4/T0CKI	0.8VDD	–	VDD	V	
D043		OSC1 (XT, HS and LP)	0.7VDD	–	VDD	V	
D043A		OSC1 (in RC mode)	0.9VDD				Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS
	IIL	<b>Input Leakage Current</b> (Notes 2, 3) I/O ports (Except PORTA)			±1.0	μA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	–	–	±0.5	μA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	–	–	±1.0	μA	VSS ≤ VPIN ≤ VDD
D063		OSC1, MCLR	–	–	±5.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
D080	VOL	<b>Output Low Voltage</b> I/O ports	–	–	0.6	V	IOL=8.5 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			–	–	0.6	V	IOL=7.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	–	–	0.6	V	IOL=1.6 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			–	–	0.6	V	IOL=1.2 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D090	VOH	<b>Output High Voltage</b> (Note 3) I/O ports (Except RA4)	VDD-0.7	–	–	V	IOH=-3.0 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			VDD-0.7	–	–	V	IOH=-2.5 mA, VDD=4.5V, $+125^{\circ}\text{C}$
D092		OSC2/CLKOUT (RC only)	VDD-0.7	–	–	V	IOH=-1.3 mA, VDD=4.5V, $-40^{\circ}$ to $+85^{\circ}\text{C}$
			VDD-0.7	–	–	V	IOH=-1.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$
*D150	VOD	<b>Open-Drain High Voltage</b>			8.5	V	RA4 pin
		<b>Capacitive Loading Specs on Output Pins</b>					
D100	COSC2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	Cio	All I/O pins/OSC2 (in RC mode)			50	pF	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16CE62X be driven with external clock in RC mode.

**2:** The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

**TABLE 13-1: COMPARATOR SPECIFICATIONS**

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C. .

Param No.	Characteristics	Sym	Min	Typ	Max	Units	Comments
D300	Input offset voltage	VIOFF		± 5.0	± 10	mV	
D301	Input common mode voltage	VICM	0		VDD - 1.5	V	
D302	CMRR	CMRR	+55*			db	
300	Response Time <sup>(1)</sup>	TRESP		150*	400*	ns	PIC16CE62X
301	Comparator Mode Change to Output Valid	TMC2OV			10*	µs	

\* These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD.

**TABLE 13-2: VOLTAGE REFERENCE SPECIFICATIONS**

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C.

Param No.	Characteristics	Sym	Min	Typ	Max	Units	Comments
D310	Resolution	VRES	VDD/24		VDD/32	LSB	
D311	Absolute Accuracy	VRAA			±1/4 ±1/2	LSB LSB	Low Range (VRR=1) High Range (VRR=0)
D312	Unit Resistor Value (R)	VRUR		2K*		Ω	Figure 9-1
310	Settling Time <sup>(1)</sup>	TSET			10*	µs	

\* These parameters are characterized but not tested.

**Note 1:** Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

## **APPENDIX A: CODE FOR ACCESSING EEPROM DATA MEMORY**

Please check our web site at [www.microchip.com](http://www.microchip.com) for code availability.

## **APPENDIX B: REVISION HISTORY**

Revision D (January 2013)

Added a note to each package outline drawing.

NOTES: