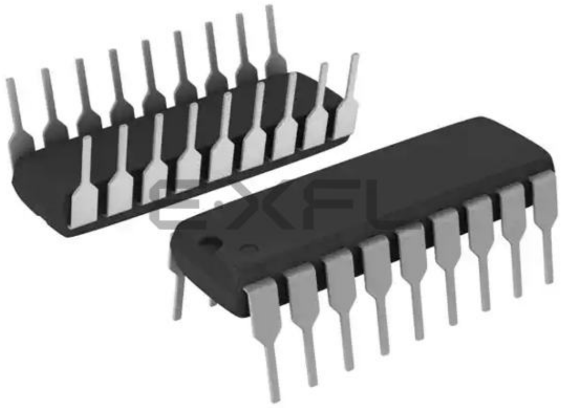

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623-04-p

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CE62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CE62X uses a Harvard architecture in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM) and non-volatile memory (EEPROM) for each PIC16CE62X device.

Device	Program Memory	RAM Data Memory	EEPROM Data Memory
PIC16CE623	512x14	96x8	128x8
PIC16CE624	1Kx14	96x8	128x8
PIC16CE625	2Kx14	128x8	128x8

The PIC16CE62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CE62X family has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CE62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CE62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit respectively, bit in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

4.2.2.6 PCON REGISTER

The PCON register contains flag bits to differentiate between a Power-on Reset, an external $\overline{MCLR}$ reset, WDT reset or a Brown-out Reset.

> **Note:** $\overline{BOD}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOD}$ is cleared, indicating a brown-out has occurred. The $\overline{BOD}$ status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by programming BODEN bit in the configuration word).

REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOD}$
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR reset
-x = Unknown at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **$\overline{BOD}$**: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

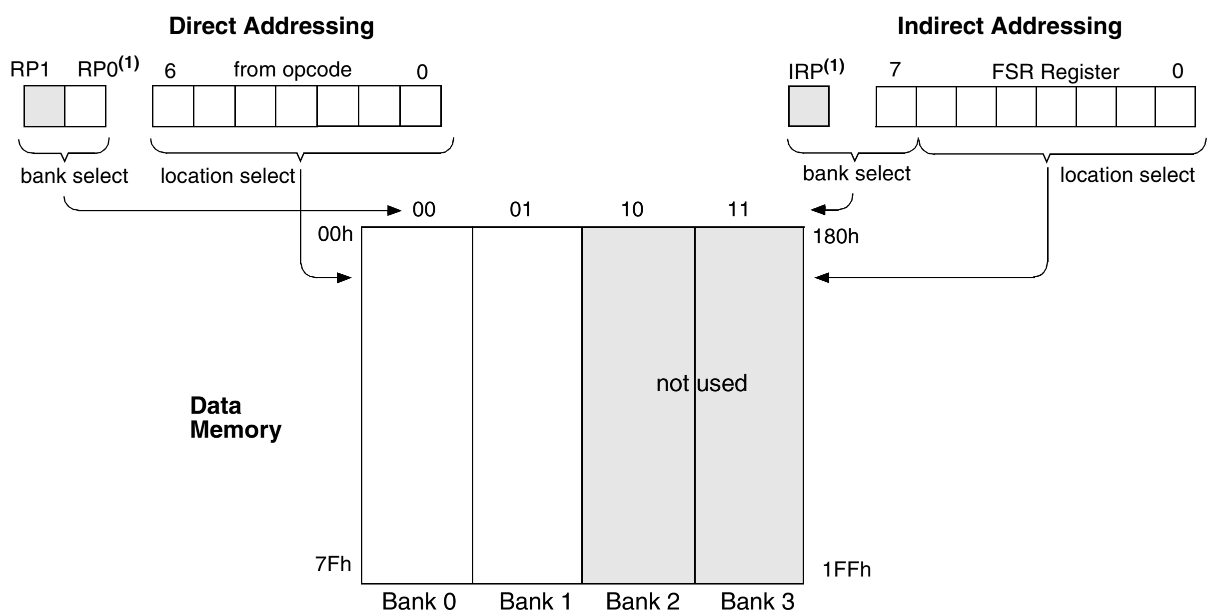
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-7. However, IRP is not used in the PIC16CE62X.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```
          movlw   0x20     ;initialize pointer
          movwf   FSR      ;to RAM
NEXT      clrf    INDF     ;clear INDF register
          incf    FSR      ;inc pointer
          btfss   FSR,4    ;all done?
          goto    NEXT     ;no clear next
                           ;yes continue
CONTINUE:
```

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING PIC16CE62X



For memory map detail see Figure 4-4 and Figure 4-5.

Note 1: The RP1 and IRP bits are reserved; always maintain these bits clear.

TABLE 5-3: PORTB FUNCTIONS

Name	Bit #	Buffer Type	Function
RB0/INT	bit0	TTL/ST(1)	Input/output or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock pin.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data pin.

Legend: ST = Schmitt Trigger, TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: u = unchanged, x = unknown

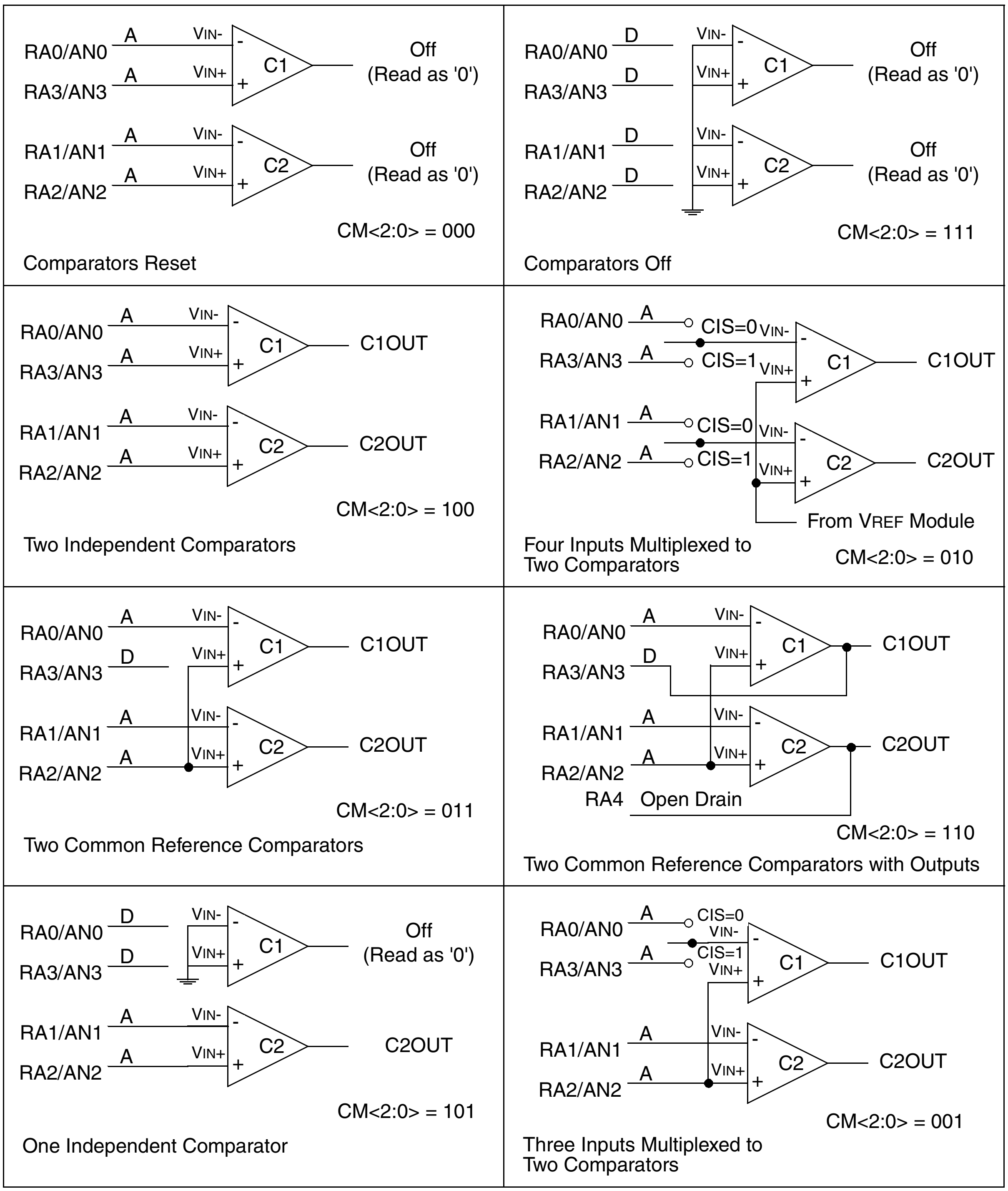
Note: Shaded bits are not used by PORTB.

8.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 8-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 13-1.

Note:	Comparator interrupts should be disabled during a comparator mode change, otherwise a false interrupt may occur.

FIGURE 8-1: COMPARATOR I/O OPERATING MODES



A = Analog Input, Port Reads Zeros Always
D = Digital Input
CIS = CMCON<3>, Comparator Input Switch

8.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs, otherwise the maximum delay of the comparators should be used (Table 13-1 **).**

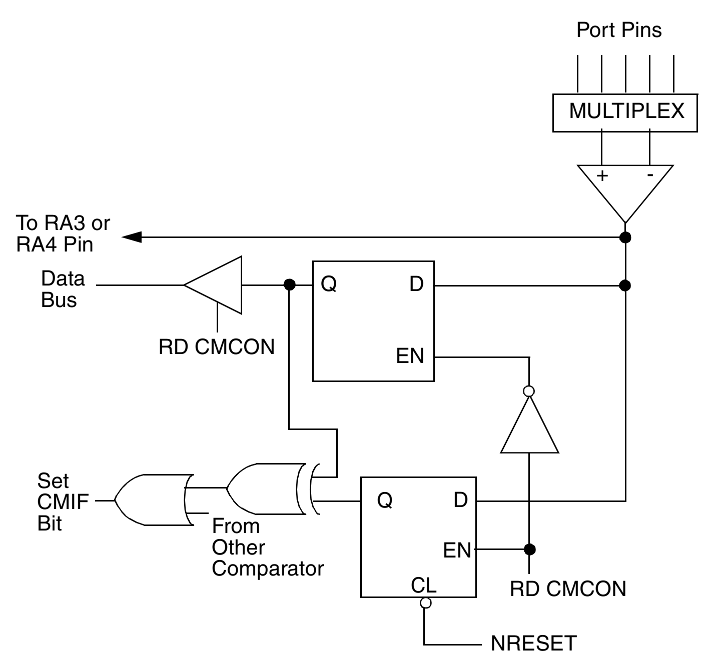
8.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 8-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

Note 1:	When reading the PORT register, all pins configured as analog inputs will read as a ‘0’. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
2:	Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 8-3: COMPARATOR OUTPUT BLOCK DIAGRAM



10.2 Oscillator Configurations

10.2.1 OSCILLATOR TYPES

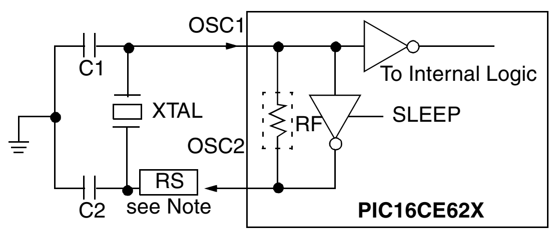
The PIC16CE62X can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

10.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 10-1). The PIC16CE62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 10-2).

FIGURE 10-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 10-1 and Table 10-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 10-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

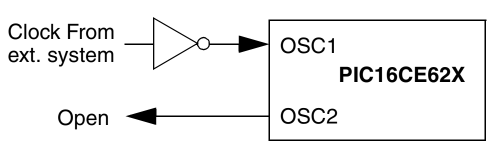


TABLE 10-1: CERAMIC RESONATORS, PIC16CE62X

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF
These values are for design guidance only. See notes at bottom of page.			

TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16CE62X

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
These values are for design guidance only. See notes at bottom of page.			

1. Recommended values of C1 and C2 are identical to the ranges tested table.
2. Higher capacitance increases the stability of oscillator, but also increases the start-up time.
3. Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

11.1 Instruction Descriptions

ADDLW — Add Literal and W

Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Encoding:	`11` `111x` `kkkk` `kkkk`
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.
Words:	1
Cycles:	1
Example	`ADDLW 0x15`

Before Instruction
W = 0x10
After Instruction
W = 0x25

ANDLW — AND Literal with W

Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Encoding:	`11` `1001` `kkkk` `kkkk`
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example	`ANDLW 0x5F`

Before Instruction
W = 0xA3
After Instruction
W = 0x03

ADDWF — Add W and f

Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (dest)
Status Affected:	C, DC, Z
Encoding:	`00` `0111` `dfff` `ffff`
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	`ADDWF FSR, 0`

Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

ANDWF — AND W with f

Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (dest)
Status Affected:	Z
Encoding:	`00` `0101` `dfff` `ffff`
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	`ANDWF FSR, 1`

Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

NOP	No Operation			
Syntax:	[*label*] NOP			
Operands:	None			
Operation:	No operation			
Status Affected:	None			
Encoding:	00	0000	0xx0	0000
Description:	No operation.			
Words:	1			
Cycles:	1			
Example	`NOP`			

OPTION	Load Option Register			
Syntax:	[*label*] OPTION			
Operands:	None			
Operation:	(W) → OPTION			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.			
Words:	1			
Cycles:	1			
Example				

To maintain upward compatibility with future PIC® MCU products, do not use this instruction.

RETFIE	Return from Interrupt			
Syntax:	[*label*] RETFIE			
Operands:	None			
Operation:	TOS → PC, 1 → GIE			
Status Affected:	None			
Encoding:	00	0000	0000	1001
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.			
Words:	1			
Cycles:	2			
Example	`RETFIE`			

After Interrupt
PC = TOS
GIE = 1

RETLW	Return with Literal in W			
Syntax:	[*label*] RETLW k			
Operands:	$0 \le k \le 255$			
Operation:	k → (W); TOS → PC			
Status Affected:	None			
Encoding:	11	01xx	kkkk	kkkk
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.			
Words:	1			
Cycles:	2			

Example

```
      CALL TABLE   ;W contains table
                   ;offset value
      •            ;W now has table
      value
      •
TABLE •
      ADDWF PC     ;W = offset
      RETLW k1     ;Begin table
      RETLW k2     ;
      •
      •
      •
      RETLW kn     ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)
Status Affected:	None
Encoding:	00 | 1110 | dfff | ffff
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.
Words:	1
Cycles:	1
Example	`SWAPF REG, 0` Before Instruction REG1 = 0xA5 After Instruction REG1 = 0xA5 W = 0x5A

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	$5 \leq f \leq 7$
Operation:	(W) → TRIS register f;
Status Affected:	None
Encoding:	00 | 0000 | 0110 | 0fff
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.
Words:	1
Cycles:	1
Example	

To maintain upward compatibility with future PIC® MCU products, do not use this instruction.

XORLW	Exclusive OR Literal with W
Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Encoding:	11 | 1010 | kkkk | kkkk
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`XORLW 0xAF` Before Instruction W = 0xB5 After Instruction W = 0x1A

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (dest)
Status Affected:	Z
Encoding:	00 | 0110 | dfff | ffff
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	`XORWF REG 1` Before Instruction REG = 0xAF W = 0xB5 After Instruction REG = 0x1A W = 0xB5

12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER®/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - SIMICE
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - SEEVAL®
  - KEELOQ®

12.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PIC MCU tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip’s simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

12.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PIC MCUs. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

12.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI ‘C’ compilers and integrated development environments for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with precompiled libraries using directives from a linker script.

13.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias .... -40° to +125°C

Storage Temperature .... -65° to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$).......... -0.6V to V_{DD} +0.6V

Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.0V

Voltage on RA4 with respect to V_{SS}.......... 8.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2).......... 0 to +14V

Voltage on RA4 with respect to V_{SS}.......... 8.5V

Total power Dissipation (Note 1) 1.0W

Maximum Current out of V_{SS} pin.......... 300 mA

Maximum Current into V_{DD} pin .... 250 mA

Input Clamp Current, I_{IK} (V_I <0 or V_I> V_{DD}).......... ±20 mA

Output Clamp Current, I_{OK} (V_O <0 or V_O>V_{DD}).......... ±20 mA

Maximum Output Current sunk by any I/O pin .... 25 mA

Maximum Output Current sourced by any I/O pin.......... 25 mA

Maximum Current sunk by PORTA and PORTB .... 200 mA

Maximum Current sourced by PORTA and PORTB.......... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100¾ should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† **NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.2 DC CHARACTERISTICS: PIC16LCE62X-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.5	–	5.5	V	See Figure 13-1 through Figure 13-3
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	.05*	–	–	V/ms	See section on power-on reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D010	IDD	Supply Current (Note 2)	– – –	1.2 – 35	2.0 1.1 70	mA mA μA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT osc mode, (Note 4)* FOSC = 4 MHz, VDD = 2.5V, WDT disabled, XT osc mode, (Note 4) FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP osc mode
D020	IPD	Power Down Current (Note 3)	– – – –	– – – –	2.0 2.2 9.0 15	μA μA μA μA	VDD = 2.5V VDD = 3.0V* VDD = 5.5V VDD = 5.5V Extended
D022	ΔIWDT	WDT Current (Note 5)	–	6.0	10 12	μA μA	VDD=4.0V (125°C)
D022A	ΔIBOR	Brown-out Reset Current (Note 5)	–	75	125	μA	$\overline{\text{BOD}}$ enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator (Note 5)	–	30	60	μA	VDD = 4.0V
D023A	ΔIVREF	VREF Current (Note 5)	–	80	135	μA	VDD = 4.0V
	ΔIEE Write ΔIEE Read ΔIEE ΔIEE	Operating Current Operating Current Standby Current Standby Current	– – – –		3 1 30 100	mA mA μA μA	VCC = 5.5V, SCL = 400 kHz VCC = 3.0V, EE VDD = VCC VCC = 3.0V, EE VDD = VCC
1A	FOSC	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0	— — — —	200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

FIGURE 13-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

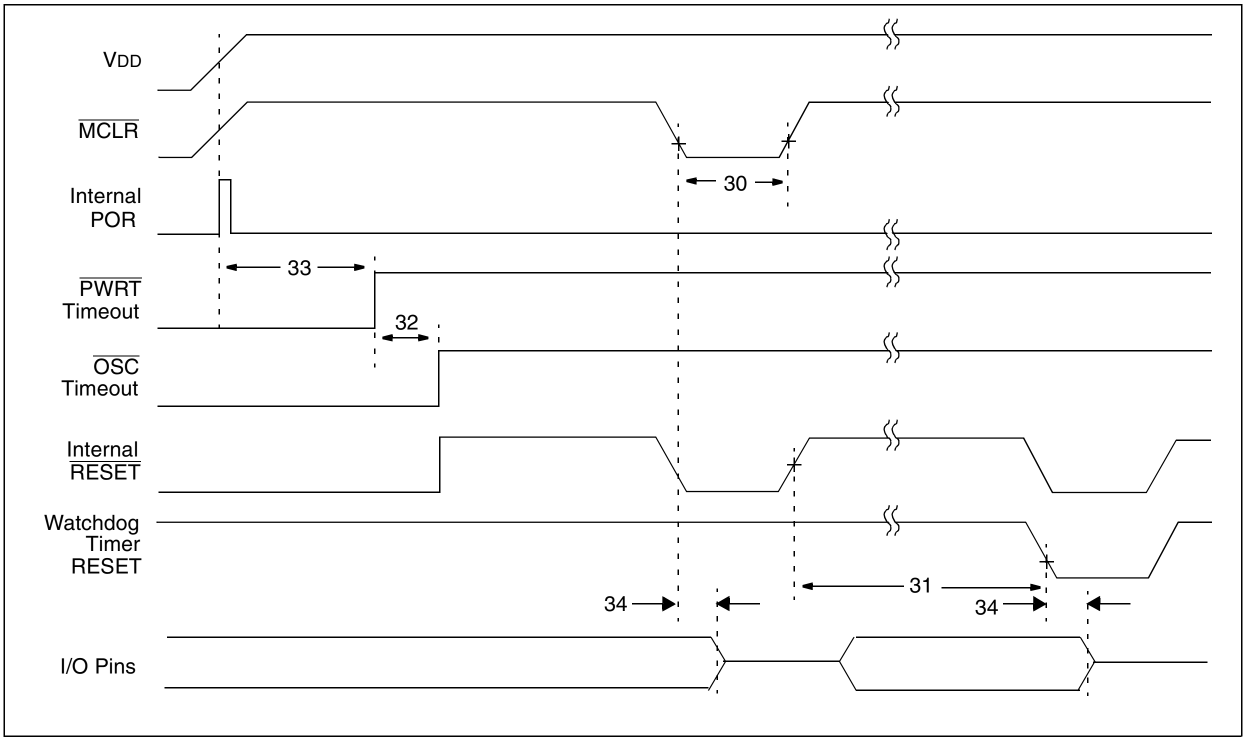


FIGURE 13-8: BROWN-OUT RESET TIMING

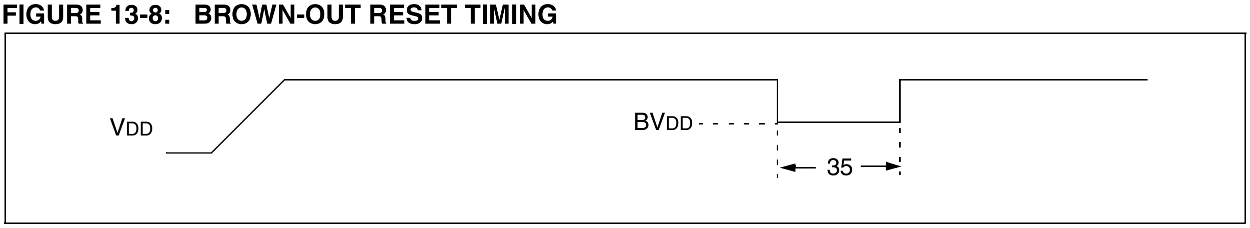


TABLE 13-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	TIOZ	I/O hi-impedance from MCLR low		—	2.0	μs	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	μs	3.7V ≤ VDD ≤ 4.3V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

13.6 EEPROM Timing

FIGURE 13-10: BUS TIMING DATA

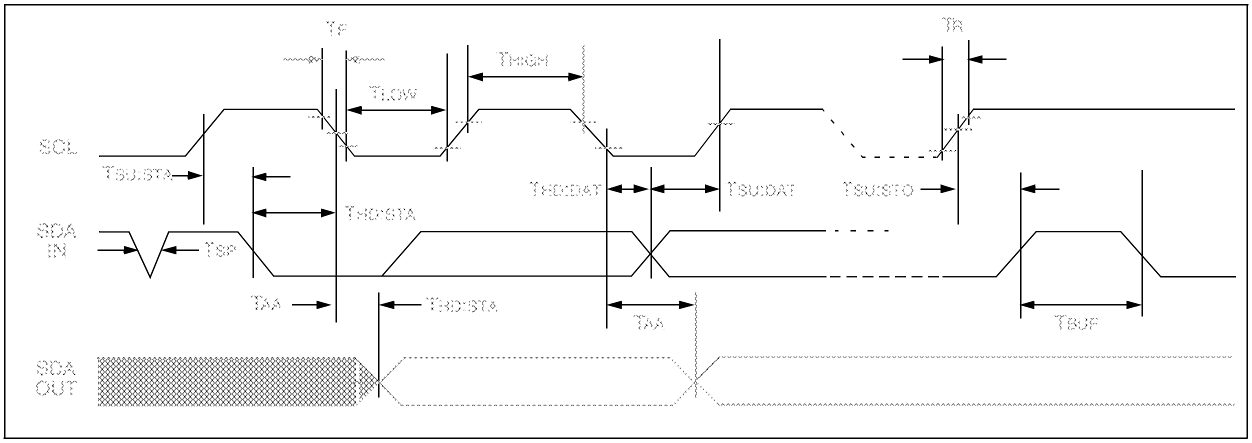


TABLE 13-7: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	10M 1M	—	10M 1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

NOTES:

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PIC16CE62X PRODUCT IDENTIFICATION SYSTEM

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PART NO. -XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank otherwise)		
Package:	P	=	PDIP
	SO	=	SOIC (Gull Wing, 300 mil body)
	SS	=	SSOP (209 mil)
	JW*	=	Windowed CERDIP
Temperature Range:	-	=	0°C to +70°C
	I	=	–40°C to +85°C
	E	=	–40°C to +125°C
Frequency Range:	04	=	200kHz (LP osc)
	04	=	4 MHz (XT and RC osc)
	20	=	20 MHz (HS osc)
Device:	PIC16CE62X :VDD range 3.0V to 5.5V		
	PIC16CE62XT:VDD range 3.0V to 5.5V (Tape and Reel)		

Examples:

a) PIC16CE623-04/P301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.

b) PIC16CE623-04I/SO = Industrial temp., SOIC package, 4MHz, industrial VDD limits.

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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