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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623-04-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623-04-so</a>

## 2.0 PIC16CE62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in the PIC16CE62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

### 2.1 UV Erasable Devices

The UV erasable version, offered in the CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16CE62X.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

### 2.3 Quick-Turn-Programming (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turn-Programming (SQTP<sup>SM</sup>) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

# PIC16CE62X

## 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The special registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

**TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16CE62X**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other resets <sup>(1)</sup>
<b>Bank 0</b>											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									—	—
08h	Unimplemented									—	—
09h	Unimplemented									—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh-1Eh	Unimplemented									—	—
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
<b>Bank 1</b>											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION	RBP <sub>U</sub>	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									—	—
88h	Unimplemented									—	—
89h	Unimplemented									—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBF	0000 000x	0000 000u
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	Unimplemented									—	—
8Eh	PCON	—	—	—	—	—	—	POR	BOD	---- -00x	---- -uuq
8Fh-9Eh	Unimplemented									—	—
90h	EEINTF	—	—	—	—	—	EESCL	EESDA	EEVDD	---- -111	---- -111
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non power-up) resets include  $\overline{MCLR}$  reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

**Note 2:** IRP & RPI bits are reserved; always maintain these bits clear.

## 4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

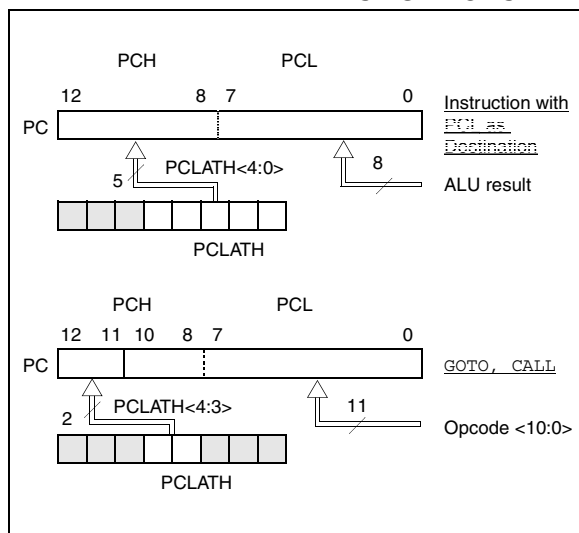
### REGISTER 4-3: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit7							bit0
<p>bit 7: <b>GIE:</b> Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts</p> <p>bit 6: <b>PEIE:</b> Peripheral Interrupt Enable bit 1 = Enables all un-masked peripheral interrupts 0 = Disables all peripheral interrupts</p> <p>bit 5: <b>TOIE:</b> TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt</p> <p>bit 4: <b>INTE:</b> RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt</p> <p>bit 3: <b>RBIE:</b> RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt</p> <p>bit 2: <b>TOIF:</b> TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow</p> <p>bit 1: <b>INTF:</b> RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur</p> <p>bit 0: <b>RBIF:</b> RB Port Change Interrupt Flag bit 1 = When at least one of the RB&lt;7:4&gt; pins changed state (must be cleared in software) 0 = None of the RB&lt;7:4&gt; pins have changed state</p>							
<p>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR reset -x = Unknown at POR reset</p>							

## 4.3 PCL and PCLATH

The program counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-6 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

**FIGURE 4-6: LOADING OF PC IN DIFFERENT SITUATIONS**



### 4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, "Implementing a Table Read" (AN556).

### 4.3.2 STACK

The PIC16CE62X family has an 8 level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

**Note 1:** There are no STATUS bits to indicate stack overflow or stack underflow conditions.

**Note 2:** There are no instruction/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

**TABLE 5-1: PORTA FUNCTIONS**

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged

**Note:** Shaded bits are not used by PORTA.

## 6.0 EEPROM PERIPHERAL OPERATION

The PIC16CE623/624/625 each have 128 bytes of EEPROM data memory. The EEPROM data memory supports a bi-directional, 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), and are mapped to bit1 and bit2, respectively, of the EEINTF register (SFR 90h). In addition, the power to the EEPROM can be controlled using bit0 (EEVDD) of the EEINTF register. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;   Inputs: EEPROM Address      EEADDR
;           EEPROM Data         EEDATA
;   Outputs: Return 01 in W if OK, else
;           return 00 in W
;
; Read_Current: Read EEPROM at address
;               currently held by EE device.
;   Inputs: NONE
;   Outputs: EEPROM Data         EEDATA
;           Return 01 in W if OK, else
;           return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
; address
;   Inputs: EEPROM Address      EEADDR
;   Outputs: EEPROM Data         EEDATA
;           Return 01 in W if OK,
;           else return 00 in W
;
```

The code for these functions is available on our web site ([www.microchip.com](http://www.microchip.com)). The code will be accessed by either including the source code FL62XINC.ASM or by linking FLASH62X.ASM. FLASH62.IMC provides external definition to the calling program.

### 6.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the memory.

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

### 6.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer to and from the memory.

### 6.0.3 EEINTF REGISTER

The EEINTF register (SFR 90h) controls the access to the EEPROM. Register 6-1 details the function of each bit. User code must generate the clock and data signals.

**REGISTER 6-1: EEINTF REGISTER (ADDRESS 90h)**

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	EESCL	EESDA	EEVDD
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

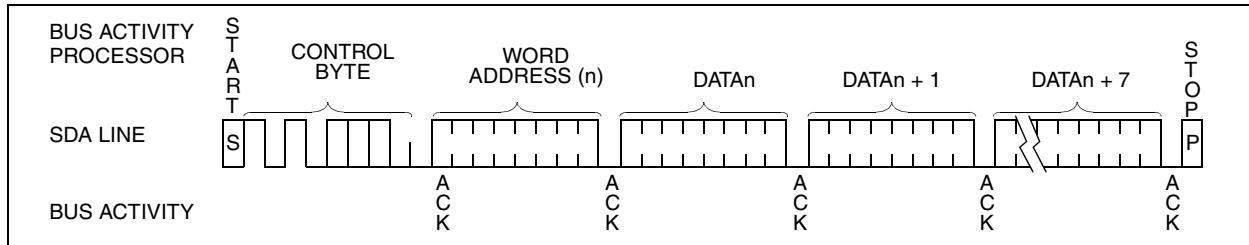
bit 2: **EESCL:** Clock line to the EEPROM  
1 = Clock high  
0 = Clock low

bit 1: **EESDA:** Data line to EEPROM  
1 = Data line is high (pin is tri-stated, line is pulled high by a pull-up resistor)  
0 = Data line is low

bit 0: **EEVDD:** VDD control bit for EEPROM  
1 = VDD is turned on to EEPROM  
0 = VDD is turned off to EEPROM (all pins are tri-stated and the EEPROM is powered down)

**Note:** EESDA, EESCL and EEVDD will read '0' if EEVDD is turned off.

**FIGURE 6-6: PAGE WRITE**



## 6.5 Read Operation

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the EEPROM address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

### 6.6 Current Address Read

The EEPROM contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address  $n$ , the next current address read operation would access data from address  $n + 1$ . Upon receipt of the EEPROM address with R/W bit set to one, the EEPROM issues an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-7).

### 6.7 Random Read

Random read operations allow the processor to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the EEPROM as part of a write operation. After the word address is sent, the processor generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the processor issues the control byte again, but with the R/W bit set to a one. The EEPROM will then issue an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-8).

## 6.8 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the EEPROM transmits the first data byte, the processor issues an acknowledge as opposed to a stop condition in a random read. This directs the EEPROM to transmit the next sequentially addressed 8-bit word (Figure 6-9).

To provide sequential reads, the EEPROM contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

## 6.9 Noise Protection

The EEPROM employs a  $V_{CC}$  threshold detector circuit, which disables the internal erase/write logic if the  $V_{CC}$  is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits, which suppress noise spikes to assure proper device operation even on a noisy bus.

## 8.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs, otherwise the maximum delay of the comparators should be used (Table 13-1).

## 8.5 Comparator Outputs

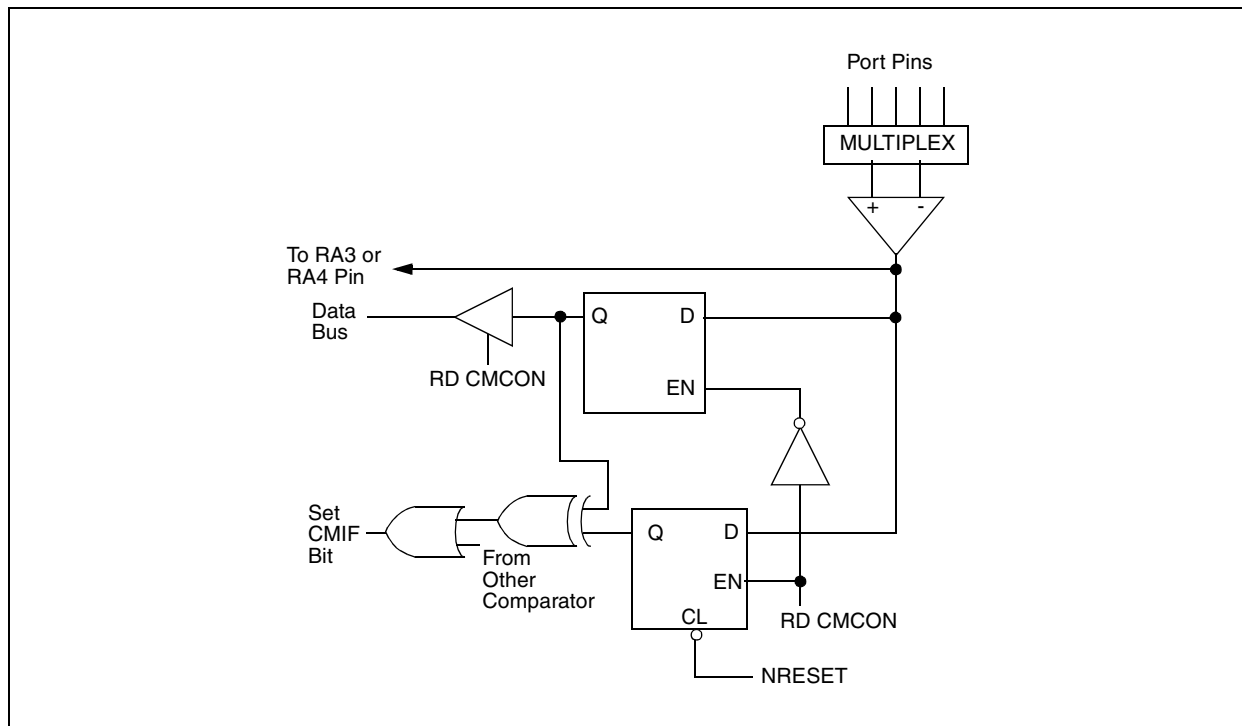
The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 8-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

**Note 1:** When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

**2:** Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

**FIGURE 8-3: COMPARATOR OUTPUT BLOCK DIAGRAM**



# PIC16CE62X

## 10.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

### REGISTER 10-1: CONFIGURATION WORD

CP1	CP0 <sup>(2)</sup>	CP1	CP0 <sup>(2)</sup>	CP1	CP0 <sup>(2)</sup>	—	BODEN <sup>(1)</sup>	CP1	CP0 <sup>(2)</sup>	PWRT <sup>(1)</sup>	WDTE	FOSC1	FOSC0	CONFIG Address REGISTER: 2007h
bit13													bit0	
bit 13-8, <b>CP1:CP0 Pairs:</b> Code protection bit pairs <sup>(2)</sup>														
5-4: <b>Code protection for 2K program memory</b>														
11 = Program memory code protection off														
10 = 0400h-07FFh code protected														
01 = 0200h-07FFh code protected														
00 = 0000h-07FFh code protected														
<b>Code protection for 1K program memory</b>														
11 = Program memory code protection off														
10 =Program memory code protection on														
01 = 0200h-03FFh code protected														
00 = 0000h-03FFh code protected														
<b>Code protection for 0.5K program memory</b>														
11 = Program memory code protection off														
10 = Program memory code protection off														
01 = Program memory code protection off														
00 = 0000h-01FFh code protected														
bit 7: <b>Unimplemented:</b> Read as '1'														
bit 6: <b>BODEN:</b> Brown-out Reset Enable bit <sup>(1)</sup>														
1 = BOD enabled														
0 = BOD disabled														
bit 3: <b>PWRT:</b> Power-up Timer Enable bit <sup>(1)</sup>														
1 = PWRT disabled														
0 = PWRT enabled														
bit 2: <b>WDTE:</b> Watchdog Timer Enable bit														
1 = WDT enabled														
0 = WDT disabled														
bit 1-0: <b>FOSC1:FOSC0:</b> Oscillator Selection bits														
11 = RC oscillator														
10 = HS oscillator														
01 = XT oscillator														
00 = LP oscillator														
<b>Note 1:</b> Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit <u>PWRT</u> . Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.														
<b>2:</b> All of the CP<1:0> pairs have to be given the same value to enable the code protection scheme listed.														

## 10.3 Reset

The PIC16CE62X differentiates between various kinds of reset:

- Power-on reset (POR)
- $\overline{\text{MCLR}}$  reset during normal operation
- $\overline{\text{MCLR}}$  reset during SLEEP
- WDT reset (normal operation)
- WDT wake-up (SLEEP)
- Brown-out Reset (BOD)

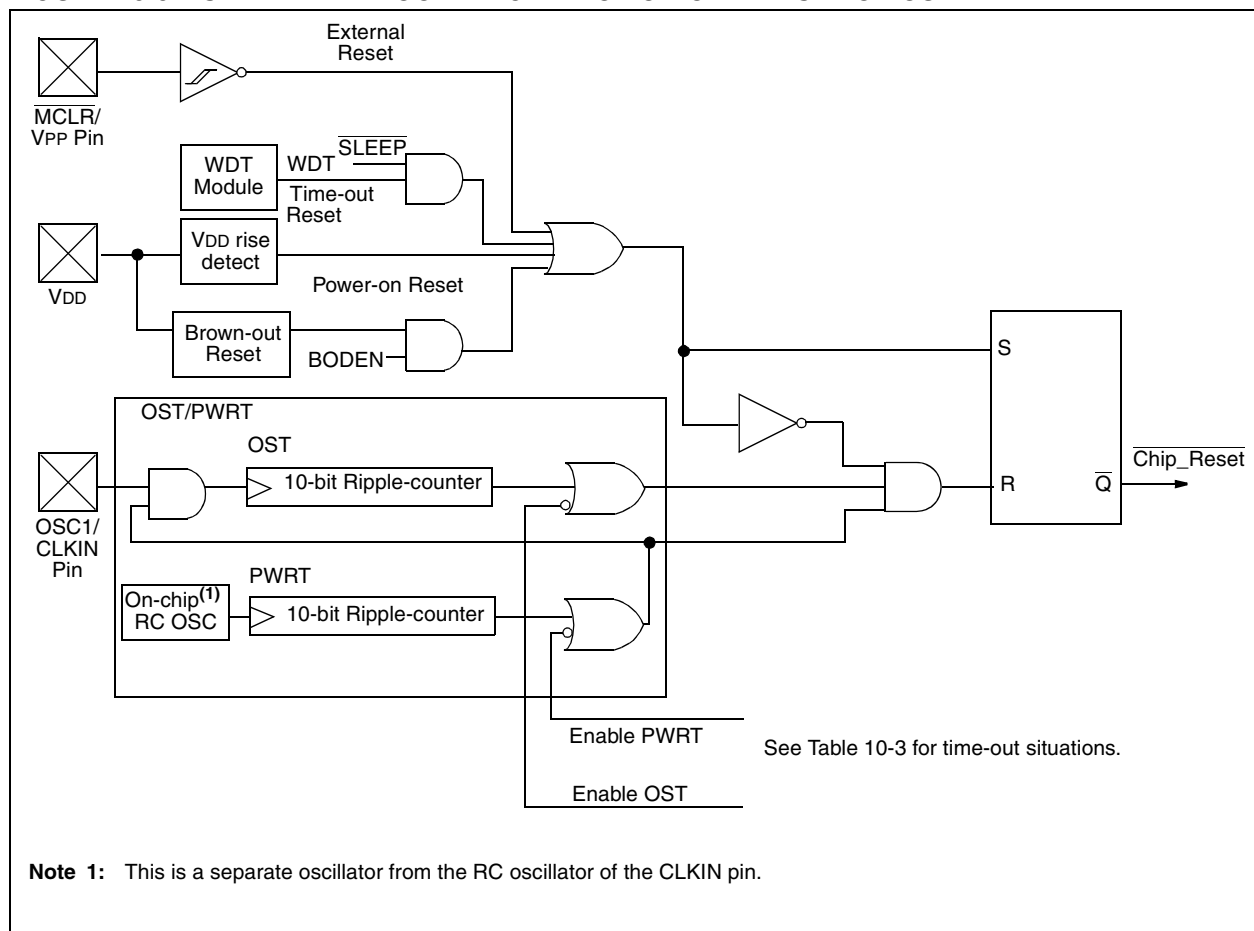
Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset

state" on Power-on reset,  $\overline{\text{MCLR}}$  reset, WDT reset and  $\overline{\text{MCLR}}$  reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation.  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different reset situations as indicated in Table 10-4. These bits are used in software to determine the nature of the reset. See Table 10-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 10-6.

The  $\overline{\text{MCLR}}$  reset path has a noise filter to detect and ignore small pulses. See Table 13-5 for pulse width specification.

**FIGURE 10-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



## 10.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the  $\overline{PD}$  bit in the STATUS register is cleared, the  $\overline{TO}$  bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin, and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The  $\overline{MCLR}$  pin must be at a logic high level ( $V_{IHMC}$ ).

**Note:** It should be noted that a RESET generated by a WDT time-out does not drive  $\overline{MCLR}$  pin low.

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The  $\overline{TO}$  and  $\overline{PD}$  bits in the STATUS register can be used to determine the cause of device reset.  $\overline{PD}$  bit, which is set on power-up is cleared when SLEEP is invoked.  $\overline{TO}$  bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from sleep. The sleep instruction is completely executed.

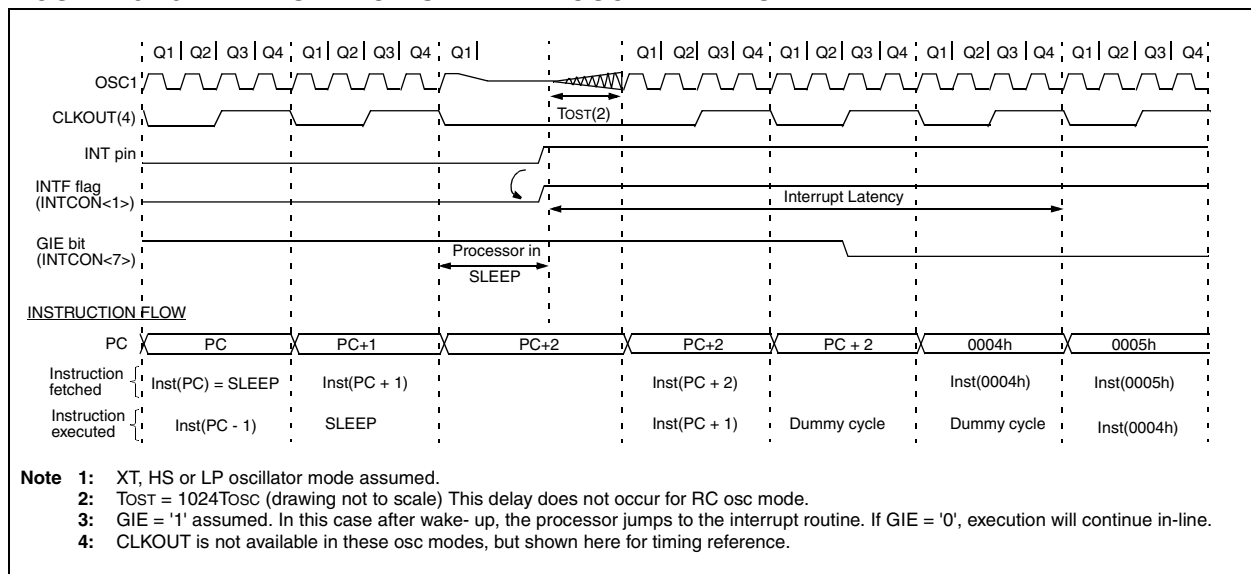
### 10.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External reset input on  $\overline{MCLR}$  pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

**FIGURE 10-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT**



## 11.1 Instruction Descriptions

### ADDLW Add Literal and W

Syntax:	[ <i>label</i> ] ADDLW    k				
Operands:	$0 \leq k \leq 255$				
Operation:	$(W) + k \rightarrow (W)$				
Status Affected:	C, DC, Z				
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>	11	111x	kkkk	kkkk
11	111x	kkkk	kkkk		
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	<div>ADDLW    0x15</div> <div>Before Instruction</div> <div>W    =    0x10</div> <div>After Instruction</div> <div>W    =    0x25</div>				

### ANDLW AND Literal with W

Syntax:	[ <i>label</i> ] ANDLW <i>k</i>				
Operands:	$0 \leq k \leq 255$				
Operation:	(W) .AND. (k) $\rightarrow$ (W)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>	11	1001	kkkk	kkkk
11	1001	kkkk	kkkk		
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	<div>ANDLW    0x5F</div> <div>Before Instruction</div> <div>W    =    0xA3</div> <div>After Instruction</div> <div>W    =    0x03</div>				

### ADDWF Add W and f

Syntax:	[ <i>label</i> ] ADDWF <i>f</i> , <i>d</i>			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	$(W) + (f) \rightarrow (dest)$			
Status Affected:	C, DC, Z			
Encoding:	00	0111	dfff	ffff
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	ADDWF    FSR,    0			
	Before Instruction			
	W    =    0x17			
	FSR =    0xC2			
	After Instruction			
	W    =    0xD9			
	FSR =    0xC2			

### ANDWF AND W with f

Syntax:	[ <i>label</i> ] ANDWF <i>f</i> , <i>d</i>				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(W) .AND. (f) $\rightarrow$ (dest)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>	00	0101	dfff	ffff
00	0101	dfff	ffff		
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	<pre>           ANDWF    FSR, 1  Before Instruction            W  =    0x17            FSR =    0xC2  After Instruction            W  =    0x17            FSR =    0x02</pre>				

SWAPF		Swap Nibbles in f						
Syntax:	[ <i>label</i> ] SWAPF f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	$(f<3:0>) \rightarrow (dest<7:4>),$ $(f<7:4>) \rightarrow (dest<3:0>)$							
Status Affected:	None							
Encoding:	<table><tr><td>00</td><td>1110</td><td>dfff</td><td>ffff</td></tr></table>				00	1110	dfff	ffff
00	1110	dfff	ffff					
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.							
Words:	1							
Cycles:	1							
Example	SWAPF REG, 0							
Before Instruction								
REG1 = 0xA5								
After Instruction								
REG1 = 0xA5								
W = 0x5A								

TRIS	Load TRIS Register				
Syntax:	[ <i>label</i> ] TRIS f				
Operands:	$5 \leq f \leq 7$				
Operation:	(W) → TRIS register f;				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0fff</td></tr></table>	00	0000	0110	0fff
00	0000	0110	0fff		
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.				
Words:	1				
Cycles:	1				
Example	<div><b>To maintain upward compatibility with future PIC® MCU products, do not use this instruction.</b></div>				

XORLW	Exclusive OR Literal with W				
Syntax:	[ <i>label</i> ] XORLW k				
Operands:	0 ≤ k ≤ 255				
Operation:	(W) .XOR. k → (W)				
Status Affected:	Z				
Encoding:	<table><tr><td>11</td><td>1010</td><td>kkkk</td><td>kkkk</td></tr></table>	11	1010	kkkk	kkkk
11	1010	kkkk	kkkk		
Description:	<p>The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.</p>				
Words:	1				
Cycles:	1				
Example:	<p>XORLW 0xAF</p> <p>Before Instruction</p> <p>W = 0xB5</p> <p>After Instruction</p> <p>W = 0x1A</p>				

XORWF	Exclusive OR W with f												
Syntax:	[ <i>label</i> ] XORWF f,d												
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$												
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)												
Status Affected:	Z												
Encoding:	<table><tr><td>00</td><td>0110</td><td>dfff</td><td>ffff</td></tr></table>	00	0110	dfff	ffff								
00	0110	dfff	ffff										
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.												
Words:	1												
Cycles:	1												
Example	<pre>XORWF REG 1</pre> <p>Before Instruction</p> <table><tr><td>REG</td><td>=</td><td>0xAF</td></tr><tr><td>W</td><td>=</td><td>0xB5</td></tr></table> <p>After Instruction</p> <table><tr><td>REG</td><td>=</td><td>0x1A</td></tr><tr><td>W</td><td>=</td><td>0xB5</td></tr></table>	REG	=	0xAF	W	=	0xB5	REG	=	0x1A	W	=	0xB5
REG	=	0xAF											
W	=	0xB5											
REG	=	0x1A											
W	=	0xB5											

stand-alone mode the PRO MATE II can read, verify or program PIC devices. It can also set code-protect bits in this mode.

## **PICSTART Plus Entry Level Development System**

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

PICSTART Plus supports all PIC devices with up to 40 pins. Larger pin count devices such as the PIC16C92X, and PIC17C76X may be supported with an adapter socket. PICSTART Plus is CE compliant.

## **SIMICE Entry-Level Hardware Simulator**

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PIC 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

## **PICDEM-1 Low-Cost PIC MCU Demonstration Board**

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

## **PICDEM-2 Low-Cost PIC16CXX Demonstration Board**

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I<sup>2</sup>C bus and separate headers for connection to an LCD module and a keypad.

## **PICDEM-3 Low-Cost PIC16CXXX Demonstration Board**

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

## **PICDEM-17**

The PICDEM-17 is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756, PIC17C762, and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE II or PICSTART Plus device programmers and easily debug

and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

## **12.17 SEEVAL Evaluation and Programming System**

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

## **12.18 KEELOQ Evaluation and Programming Tools**

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

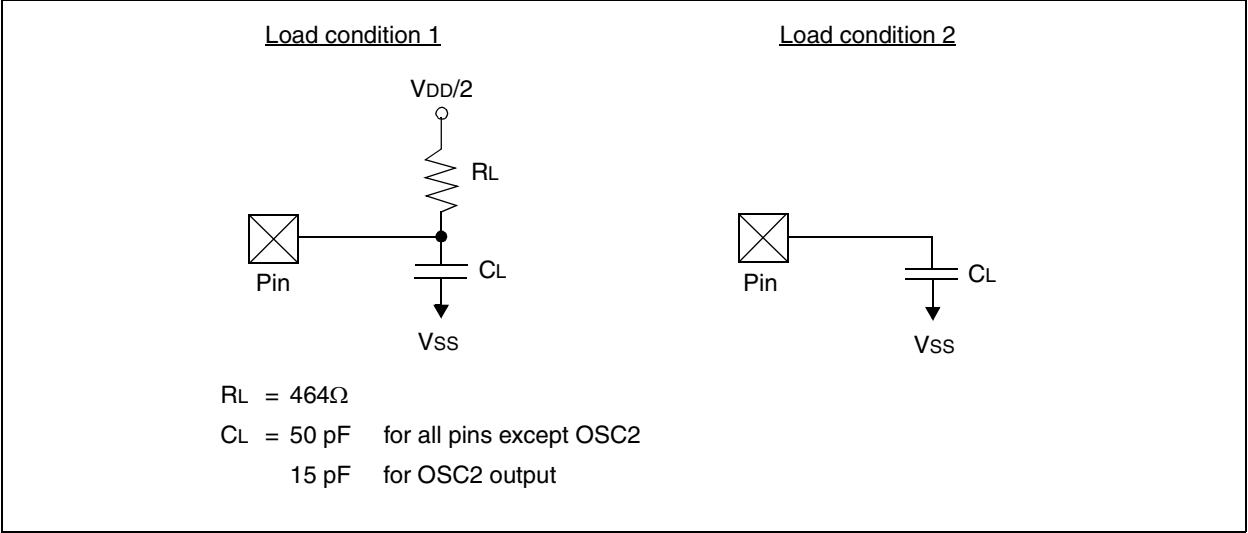
13.4 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

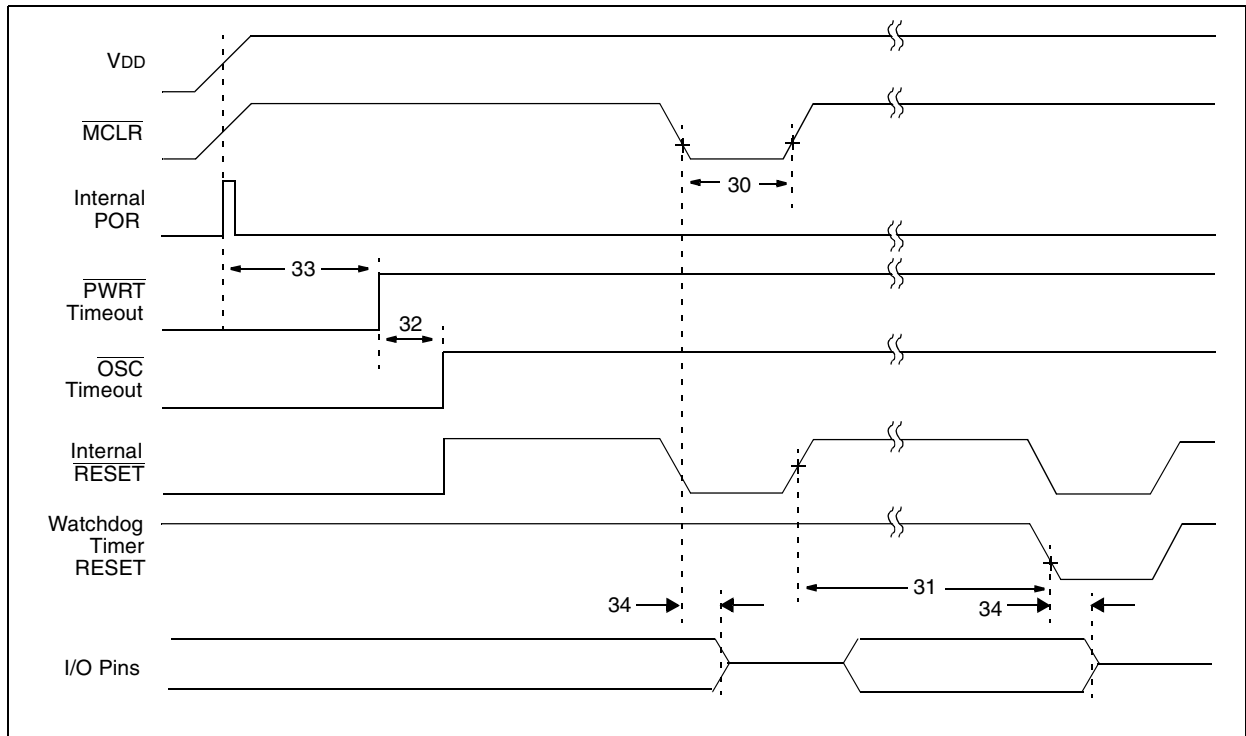
- 1. TppS2ppS
- 2. TppS

<b>T</b>			
F	Frequency	T	Time
Lowercase subscripts (pp) and their meanings:			
<b>pp</b>			
ck	CLKOUT	osc	OSC1
io	I/O port	t0	T0CKI
mc	MCLR		
Uppercase letters and their meanings:			
<b>S</b>			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

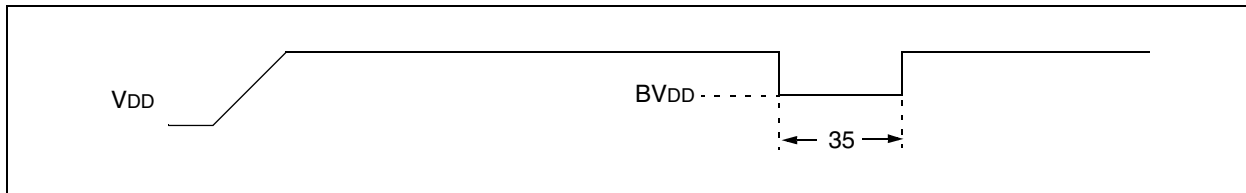
FIGURE 13-4: LOAD CONDITIONS



**FIGURE 13-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 13-8: BROWN-OUT RESET TIMING**



**TABLE 13-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	Tioz	I/O hi-impedance from MCLR low	—	—	2.0	μs	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	μs	3.7V ≤ VDD ≤ 4.3V

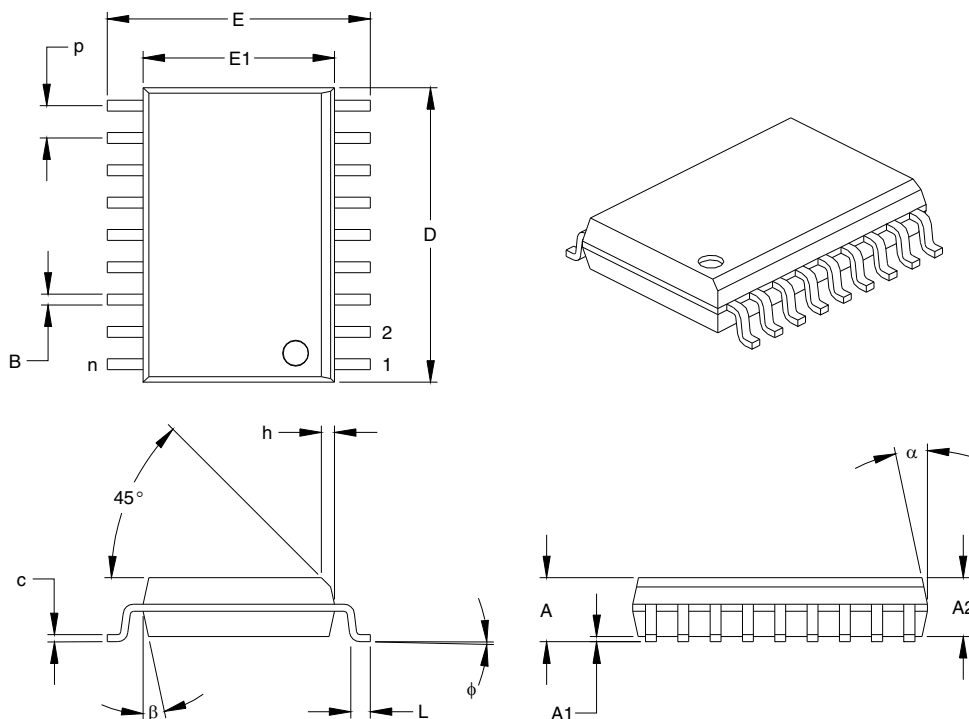
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16CE62X

## 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	P		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
JEDEC Equivalent: MS-013  
Drawing No. C04-051

# PIC16CE62X

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NOTES:

