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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623-04i-so

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PIC16CE62X

FIGURE 3-1: BLOCK DIAGRAM



3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (i.e., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-2: CLOCK/INSTRUCTION CYCLE





All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

4.3 PCL and PCLATH

The program counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-6 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 4-6: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CE62X family has an 8 level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.
- Note 2: There are no instruction/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

6.1 Bus Characteristics

In this section, the term "processor" refers to the portion of the PIC16CE62X that interfaces to the EEPROM through software manipulating the EEINTF register. The following **bus protocol** is to be used with the EEPROM data memory.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted by the EEPROM as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 6-1).

6.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

6.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

6.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

6.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the processor and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out fashion.

6.1.5 ACKNOWLEDGE

The EEPROM will generate an acknowledge after the reception of each byte. The processor must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	Acknowledge bits are not generated if an
	internal programming cycle is in progress.

When the EEPROM acknowledges, it pulls down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. The processor must signal an end of data to the EEPROM by not generating an acknowledge bit on the last byte that has been clocked out of the EEPROM. In this case, the EEPROM must leave the data line HIGH to enable the processor to generate the STOP condition (Figure 6-2).



6.5 <u>Read Operation</u>

Read operations are initiated in the same way as write operations with the exception that the R/\overline{W} bit of the EEPROM address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.6 Current Address Read

The EEPROM contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the EEPROM address with R/W bit set to one, the EEPROM issues an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-7).

6.7 Random Read

Random read operations allow the processor to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the EEPROM as part of a write operation. After the word address is sent, the processor generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the processor issues the control byte again, but with the R/W bit set to a one. The EEPROM will then issue an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-8).

6.8 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the EEPROM transmits the first data byte, the processor issues an acknowledge as opposed to a stop condition in a random read. This directs the EEPROM to transmit the next sequentially addressed 8-bit word (Figure 6-9).

To provide sequential reads, the EEPROM contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.9 Noise Protection

The EEPROM employs a Vcc threshold detector circuit, which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits, which suppress noise spikes to assure proper device operation even on a noisy bus.





FIGURE 6-8: RANDOM READ

BUS ACTIVITY

. .

A C K

DATAn



DATAn + 1

DATAn + 2

N O

A C K

DATAn + X

7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

8.1 <u>Comparator Configuration</u>

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 8-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the comparator

mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 13-1.

Note: Comparator interrupts should be disabled during a comparator mode change, otherwise a false interrupt may occur.



FIGURE 8-1: COMPARATOR I/O OPERATING MODES

The code example in Example 8-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

EXAMPLE 8-1: INITIALIZING COMPARATOR MODULE

FLAG_REG	EQU	0X20
CLRF	FLAG_REG	;Init flag register
CLRF	PORTA	;Init PORTA
MOVF	CMCON,W	;Move comparator contents to W
ANDLW	0xC0	;Mask comparator bits
IORWF	FLAG_REG,F	;Store bits in flag register
MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON, F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON,GIE	;Global interrupt enable

8.2 Comparator Operation

A single comparator is shown in Figure 8-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN–, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN–, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 8-2 represent the uncertainty due to input offsets and response time.

8.3 <u>Comparator Reference</u>

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN– is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 8-2).

FIGURE 8-2: SINGLE COMPARATOR



8.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD and can be applied to either pin of the comparator(s).

8.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 13, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 8-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

8.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
- b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

8.7 <u>Comparator Operation During SLEEP</u>

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

8.8 Effects of a RESET

A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

8.9 <u>Analog Input Connection</u> <u>Considerations</u>

A simplified circuit for an analog input is shown in Figure 8-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.



FIGURE 8-4: ANALOG INPUT MODEL

10.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

REGISTER 10-1: CONFIGURATION WORD

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

lr		1
CP1 CF	P0 ⁽²⁾ CP1 CP0 ⁽²⁾ CP1 CP0 ⁽²⁾ BODEN ⁽¹⁾ CP1 CP0 ⁽²⁾ PWRTE ⁽¹⁾ WDTE F0SC1 F0SC0 CONFIG A	ddress 2007b
		200711
bit 13-8,	CP1:CP0 Pairs: Code protection bit pairs ^C	
5-4.	11 = Program memory code protection off	
	10 = 0400h-07FFh code protected	
	01 = 0200h-07FFh code protected	
	00 = 0000h-07FFh code protected	
	Code protection for 1K program memory	
	11 = Program memory code protection off	
	10 =Program memory code protection on	
	01 = 0200 - 03FFh code protected	
	Code protection for 0.5K program memory	
	11 = Program memory code protection off	
	10 = Program memory code protection off	
	01 = Program memory code protection off	
	00 = 0000h-01FFh code protected	
bit 7:	Unimplemented: Read as '1'	
bit 6:	BODEN: Brown-out Reset Enable bit ⁽¹⁾	
	1 = BOD enabled	
	0 = BOD disabled	
bit 3:	PWRTE : Power-up Timer Enable bit ⁽¹⁾	
	1 = PWRT disabled	
	0 = PWRT enabled	
bit 2:	WDTE: Watchdog Timer Enable bit	
	1 = WDT enabled	
	0 = WDT disabled	
bit 1-0:	FOSC1:FOSC0: Oscillator Selection bits	
	11 = RC oscillator	
	10 = HS oscillator	
	01 = X I OSCIIIATOR	
Note 1:	Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWRTE	
	Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.	
2:	All of the CP<1:0> pairs have to be given the same value to enable the code protection scheme listed.	

10.2 Oscillator Configurations

10.2.1 OSCILLATOR TYPES

The PIC16CE62X can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

10.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 10-1). The PIC16CE62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 10-2).

FIGURE 10-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 10-1 and Table 10-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 10-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 10-1: CERAMIC RESONATORS, PIC16CE62X

Ranges Tested: OSC2 Mode Freq OSC1 XT 455 kHz 68 - 100 pF 68 - 100 pF 15 - 68 pF 15 - 68 pF 2.0 MHz 4.0 MHz 15 - 68 pF 15 - 68 pF HS 10 - 68 pF 10 - 68 pF 8.0 MHz 16.0 MHz 10 - 22 pF 10 - 22 pF

These values are for design guidance only. See notes at bottom of page.

TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16CE62X

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

These values are for design guidance only. See notes at bottom of page.

- 1. Recommended values of C1 and C2 are identical to the ranges tested table.
- 2. Higher capacitance increases the stability of oscillator, but also increases the start-up time.
- 3. Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

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10.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit in the STATUS register is cleared, the \overline{TO} bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin, and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated					
	by a WDT time-out does not drive MCLF					
	pin low.					

10.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External reset input on MCLR pin
- 2. Watchdog Timer Wake-up (if WDT was enabled)
- 3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The \overline{TO} and \overline{PD} bits in the STATUS register can be used to determine the cause of device reset. \overline{PD} bit, which is set on power-up is cleared when SLEEP is invoked. \overline{TO} bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the SLEEP instruction after the instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

If the global interrupts are disabled (GIE is
cleared), but any interrupt source has both
its interrupt enable bit and the correspond-
ing interrupt flag bits set, the device will
immediately wake-up from sleep. The
sleep instruction is completely executed.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

; a1 a2 a3 a4 ; a1 a2 a3 a osc1////////////////////////////////////	4 Q1	a1 a2 a3 a4	a1 a2 a3 a4	; a1 a2 a3 a4 /~	; a1 a2 a3 a4; ////////////////////////////////////
CLKOUT(4)	Tost(2)		\/	<u>\</u> /	\ł
INT pin INTF flag (INTCON<1>) GIE bit (INTCON<7>)	Processor in SLEEP		Interrupt Latency		
INSTRUCTION FLOW			I I	I I	
PC PC PC+1	PC+2	X PC+2	X PC + 2	X 0004h	X 0005h
$\begin{array}{l} \mbox{Instruction} \\ \mbox{fetched} \end{array} \left\{ \begin{array}{l} \mbox{Inst(PC)} = \mbox{SLEEP} & \mbox{Inst(PC + 1)} \end{array} \right.$		Inst(PC + 2)	1 1 1	Inst(0004h)	Inst(0005h)
Instruction { Inst(PC - 1) SLEEP	1 1 1	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)

FIGURE 10-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT

Note 1: XT, HS or LP oscillator mode assumed.

2: TOST = 1024TOSC (drawing not to scale) This delay does not occur for RC osc mode.

3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these osc modes, but shown here for timing reference.

PIC16CE62X

RETURN	Return from Subroutine	RRF	Rotate Right f through Carry			
Syntax:	[label] RETURN	Syntax:	[<i>label</i>] RRF f,d			
Operands:	None	Operands:	$0 \leq f \leq 127$			
Operation:	$TOS \rightarrow PC$		$d \in [0,1]$			
Status Affected:	None	Operation:	See description below			
Encoding:	00 0000 0000 1000	Status Affected:	С			
Description:	Return from subroutine. The stack is	Encoding:	00 1100 dfff ffff			
Words:	POPed and the top of the stack (TOS) Description: is loaded into the program counter. This is a two cycle instruction. 1		The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is			
Cycles:	2					
Example	RETURN					
	After Interrupt	Words:	1			
	PC = TOS	Cycles:	1			
		Example	RRF REG1,0			
			Before Instruction			
			REG1 = 1110 0110 C = 0			
			After Instruction			
			$\begin{array}{rcl} \mathbf{REG1} &=& 1110 & 0110 \\ \mathbf{W} &=& 0111 & 0011 \end{array}$			
			C = 0			

RLF	Rotate	Rotate Left f through Carry					
Syntax:	[label]	RLF	f,d				
Operands:	0 ≤ f ≤ 1 d ∈ [0,1	27]					
Operation:	See des	See description below					
Status Affected:	С						
Encoding:	0 0	1101	df	ff	ffff		
	one bit to Flag. If 'c the W res stored ba	the left the left the gister. If 'c ack in regi	result 'is 1, ster 'f'.	the C is plac the res	Carry ced in sult is		
Words:	1						
Cycles:	1						
Example	RLF	RE	G1,0				
	Before I	Before Instruction					
		REG1	=	1110	0110		
	A ft a v lua e	C	=	0			
	Alterins			1110	0110		
		W	=	1100	1100		
		C	=	1	1100		

SLEEP

Syntax:	[label]	SLEEP)			
Operands:	None					
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$					
Status Affected:	TO, PD					
Encoding:	00 0000 0110 0011					
Description:	The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 10.8 for more details					
Words:	1					
Cycles:	1					
Example:	SLEEP					

13.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.0V
Voltage on RA4 with respect to Vss	8.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	8.5V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into Vod pin	250 mA
Input Clamp Current, Iк (Vi <0 or Vi> VDD)	±20 mA
Output Clamp Current, Iок (Vo <0 or Vo>VDD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA and PORTB	200 mA
Maximum Current sourced by PORTA and PORTB	200 mA
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum {(VD	D-VOH) x IOH} + \sum (VOI x IOL)

2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100³/₄ should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.2 DC CHARACTERISTICS: F

PIC16LCE62X-04 (Commercial, Industrial)

DC CHARACTERISTICS				Standard Operating Conditions (unless otherwise stated)						
				Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial and $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial and						
				-40° C \leq TA \leq +125°C for extended						
Param	Sym	Characteristic	Min	Typ†	Max	Units	Inits Conditions			
No.										
D001	Vdd	Supply Voltage	2.5	-	5.5	V	See Figure 13-1 through Figure 13-3			
D002	Vdr	RAM Data Retention Voltage (Note 1)	-	1.5*	-	V	Device in SLEEP mode			
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	-	V	See section on power-on reset for details			
D004	SVDD	VDD rise rate to ensure Power-on Reset	.05*	-	-	V/ms	See section on power-on reset for details			
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared			
D010	IDD	Supply Current (Note 2)	-	1.2	2.0	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled,			
							XT osc mode, (Note 4)*			
			_	_	1.1	mA	FOSC = 4 MIHZ, $VDD = 2.5$ V, WDT disabled, XT osc mode (Note 4)			
			_	35	70	μA	Fosc = 32 kHz , VDD = 2.5V, WDT disabled,			
						•	LP osc mode			
D020	IPD	Power Down Current (Note 3)	-	-	2.0	μA	VDD = 2.5V			
			-	-	2.2	μA	VDD = 3.0V*			
			-	-	9.0	μA A	VDD = 5.5V			
D000	ALWET	WDT Ourrent (Note 5)	_	-	10	μΑ				
D022	ΔIWDT	WDT Current (Note 5)	-	6.0	10	μΑ	VDD=4.0V (125°C)			
D022A	ΔIBOR	Brown-out Reset Current	_	75	125	μA μA	$\frac{(123)}{BOD}$ enabled. VDD = 5.0V			
		(Note 5)				P				
D023		Comparator Current for each	-	30	60	μA	VDD = 4.0V			
00224		Comparator (Note 5)		80	125		$V_{DD} = 4.0 V$			
DUZSA		Operating Current	_	80	2	μA mA	$V_{00} = 4.0V$			
		Operating Current	_		1	mA	VCC = 5.5V, SCL = 400 KHz			
		Standby Current	_		30	μA	VCC = 3.0V, EE VDD = VCC			
	ΔIEE	Standby Current	-		100	μΑ	VCC = 3.0V, EE VDD = VCC			
1A	Fosc	LP Oscillator Operating Frequency	0		200	kHz	All temperatures			
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures			
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures			
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in k Ω .

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

13.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

Т					
F	Frequency	Т	Time		
Lowerca	ase subscripts (pp) and their meanings:				
рр					
ck	CLKOUT	OSC	OSC1		
io	I/O port	t0	TOCKI		
mc	MCLR				
Uppercase letters and their meanings:					
S					
F	Fall	Р	Period		
Н	High	R	Rise		
I	Invalid (Hi-impedance)	V	Valid		
L	Low	Z	Hi-Impedance		

FIGURE 13-4: LOAD CONDITIONS



PIC16CE62X

FIGURE 13-9: TIMER0 CLOCK TIMING



TABLE 13-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	_	_	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		<u>Tcy + 40</u> * N			ns	N = prescale value (1, 2, 4,, 256)

t

These parameters are characterized but not tested. Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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