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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 13 |
| Program Memory Size | 896B (512 x 14) |
| Program Memory Type | OTP |
| EEPROM Size | 128 x 8 |
| RAM Size | 96 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623-04i-ss |

2.0 PIC16CE62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in the PIC16CE62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in the Cerdip package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16CE62X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turn-Programming (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

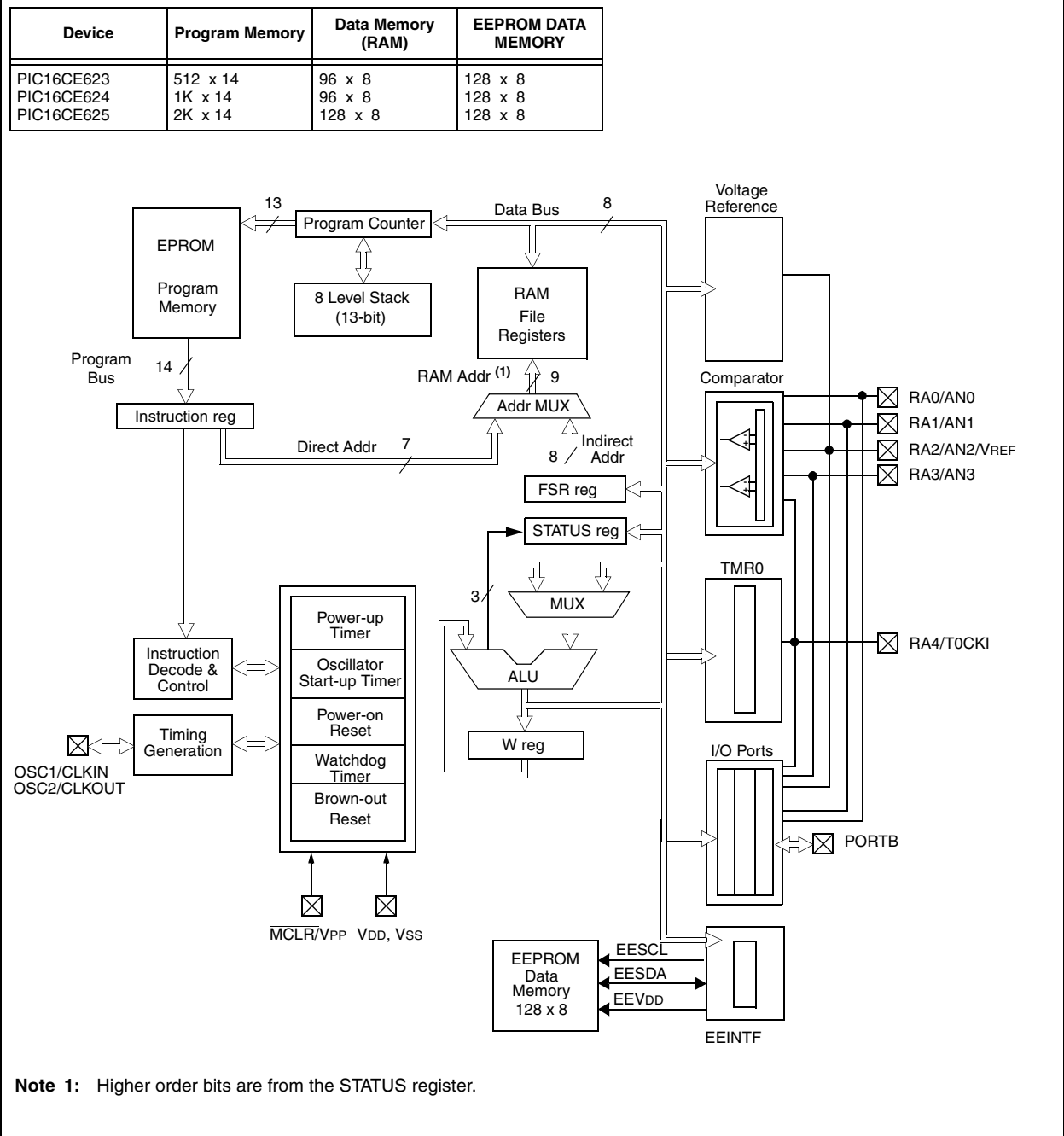
2.4 Serialized Quick-Turn-Programming (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

PIC16CE62X

FIGURE 3-1: BLOCK DIAGRAM



4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-7Fh (Bank0) on the PIC16CE623/624 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16CE625 are General Purpose Registers implemented as static RAM. Some special purpose registers are mapped in Bank 1. In all three microcontrollers, address space F0h-FFh (Bank1) is mapped to 70-7Fh (Bank0) as common RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 96 x 8 in the PIC16CE623/624 and 128 x 8 in the PIC16CE625. Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

6.0 EEPROM PERIPHERAL OPERATION

The PIC16CE623/624/625 each have 128 bytes of EEPROM data memory. The EEPROM data memory supports a bi-directional, 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), and are mapped to bit1 and bit2, respectively, of the EEINTF register (SFR 90h). In addition, the power to the EEPROM can be controlled using bit0 (EEVDD) of the EEINTF register. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;   Inputs: EEPROM Address      EEADDR
;           EEPROM Data         EEDATA
;   Outputs: Return 01 in W if OK, else
;           return 00 in W
;
; Read_Current: Read EEPROM at address
;               currently held by EE device.
;   Inputs: NONE
;   Outputs: EEPROM Data        EEDATA
;           Return 01 in W if OK, else
;           return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
; address
;   Inputs: EEPROM Address      EEADDR
;   Outputs: EEPROM Data        EEDATA
;           Return 01 in W if OK,
;           else return 00 in W
;
```

The code for these functions is available on our web site (www.microchip.com). The code will be accessed by either including the source code FL62XINC.ASM or by linking FLASH62X.ASM. FLASH62.IMC provides external definition to the calling program.

6.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the memory.

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

6.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer to and from the memory.

6.0.3 EEINTF REGISTER

The EEINTF register (SFR 90h) controls the access to the EEPROM. Register 6-1 details the function of each bit. User code must generate the clock and data signals.

REGISTER 6-1: EEINTF REGISTER (ADDRESS 90h)

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 |
|------|-----|-----|-----|-----|-------|-------|-------|
| — | — | — | — | — | EESCL | EESDA | EEVDD |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2: **EESCL:** Clock line to the EEPROM
1 = Clock high
0 = Clock low

bit 1: **EESDA:** Data line to EEPROM
1 = Data line is high (pin is tri-stated, line is pulled high by a pull-up resistor)
0 = Data line is low

bit 0: **EEVDD:** VDD control bit for EEPROM
1 = VDD is turned on to EEPROM
0 = VDD is turned off to EEPROM (all pins are tri-stated and the EEPROM is powered down)

Note: EESDA, EESCL and EEVDD will read '0' if EEVDD is turned off.

7.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control

bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 Timer0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM

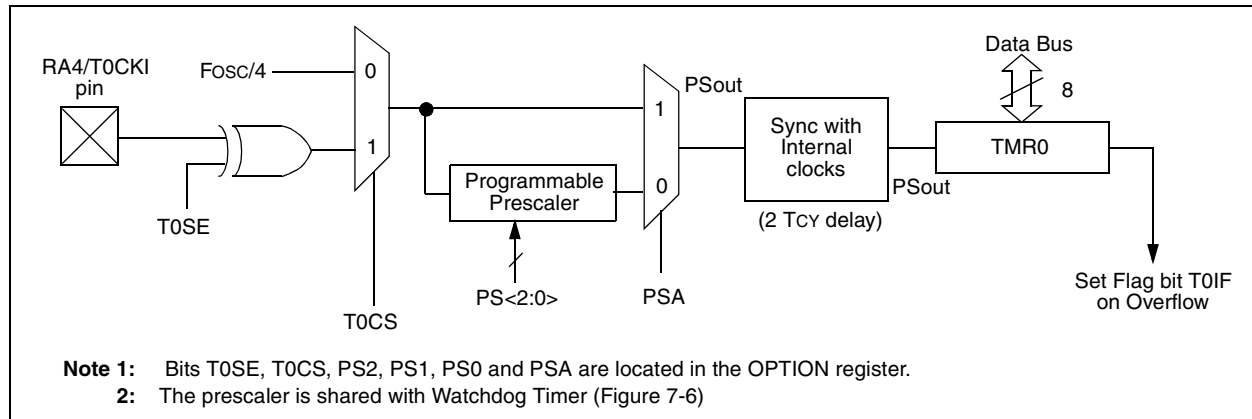
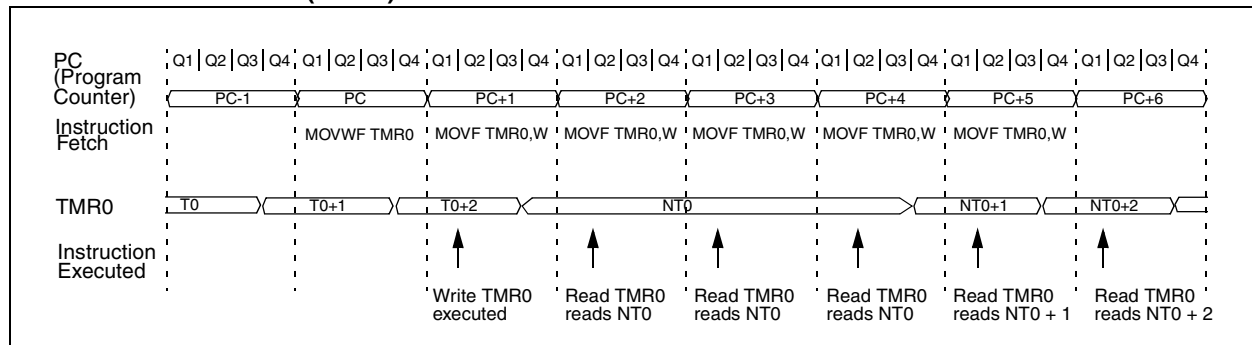


FIGURE 7-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER



PIC16CE62X

NOTES:

8.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
- b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

8.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will

wake-up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

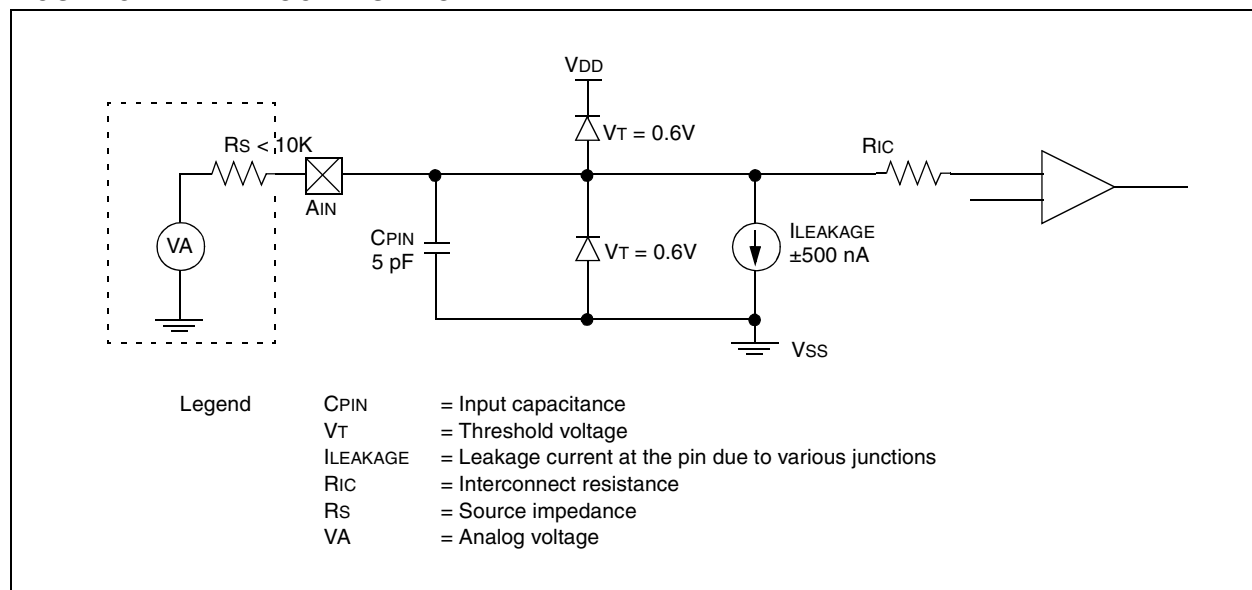
8.8 Effects of a RESET

A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

8.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 8-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 8-4: ANALOG INPUT MODEL



9.0 VOLTAGE REFERENCE MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 9-1. The block diagram is given in Figure 9-1.

9.1 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range.

The equations used to calculate the output of the Voltage Reference are as follows:

$$\text{if } VRR = 1: VREF = (VR<3:0>/24) \times VDD$$

$$\text{if } VRR = 0: VREF = (VDD \times 1/4) + (VR<3:0>/32) \times VDD$$

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 13-1). Example 9-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

REGISTER 9-1: VRCON REGISTER (ADDRESS 9Fh)

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-----|-------|-------|-------|-------|
| VREN | VROE | VRR | — | VR3 | VR2 | VR1 | VR0 |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **VREN:** VREF Enable
1 = VREF circuit powered on
0 = VREF circuit powered down, no IDD drain

bit 6: **VROE:** VREF Output Enable
1 = VREF is output on RA2 pin
0 = VREF is disconnected from RA2 pin

bit 5: **VRR:** VREF Range selection
1 = Low Range
0 = High Range

bit 4: **Unimplemented:** Read as '0'

bit 3-0: **VR<3:0>:** VREF value selection $0 \leq VR[3:0] \leq 15$
when VRR = 1: $VREF = (VR<3:0>/24) \times VDD$
when VRR = 0: $VREF = 1/4 \times VDD + (VR<3:0>/32) \times VDD$

FIGURE 9-1: VOLTAGE REFERENCE BLOCK DIAGRAM

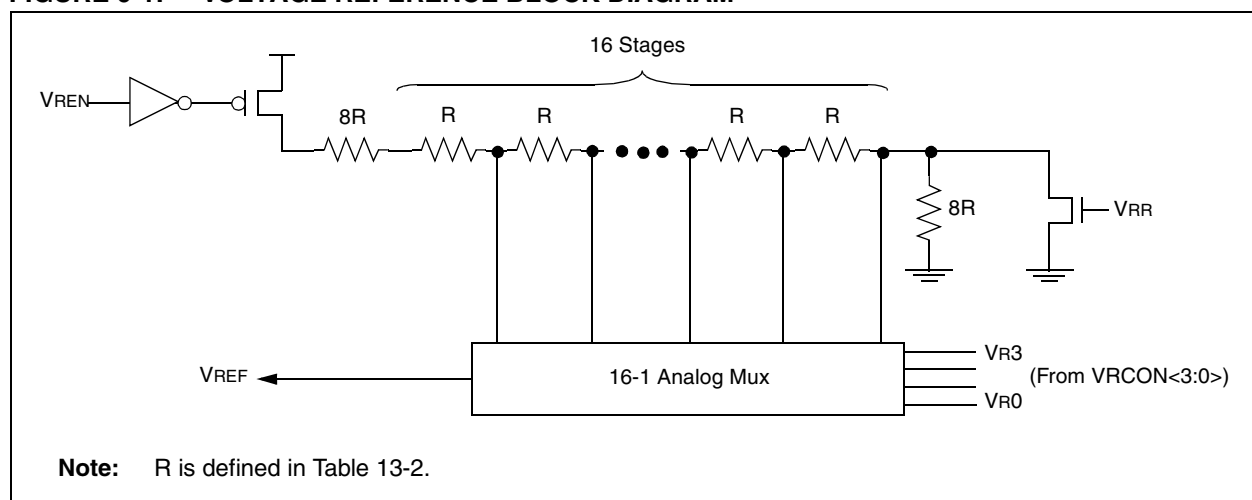


FIGURE 10-17: WATCHDOG TIMER BLOCK DIAGRAM

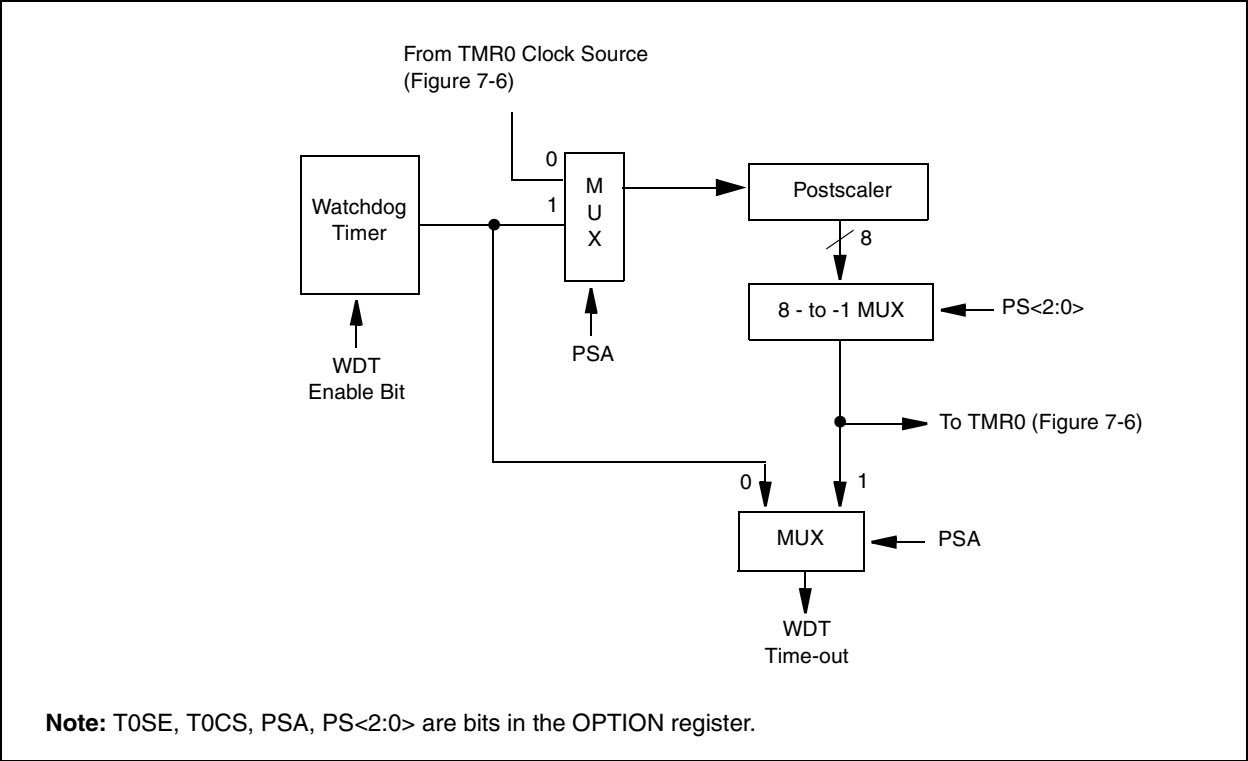


FIGURE 10-18: SUMMARY OF WATCHDOG TIMER REGISTERS

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|--------------------|--------|-------|-------|-------|-------|-------|-------|
| 2007h | Config. bits | — | BOREN | CP1 | CP0 | PWRTE | WDTE | FOSC1 | FOSC0 |
| 81h | OPTION | RBP \overline{U} | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |

Legend: – = Unimplemented location, read as “0”, + = Reserved for future use

Note: Shaded cells are not used by the Watchdog Timer.

PIC16CE62X

TABLE 11-2: PIC16CE62X INSTRUCTION SET

| Mnemonic, Operands | Description | Cycles | 14-Bit Opcode | | | | Status Affected | Notes | |
|--|-------------|------------------------------|---------------|----|------|------|--------------------|--------------------------------|-------|
| | | | MSb | | LSb | | | | |
| BYTE-ORIENTED FILE REGISTER OPERATIONS | | | | | | | | | |
| ADDWF | f, d | Add W and f | 1 | 00 | 0111 | dfff | ffff | C,DC,Z | 1,2 |
| ANDWF | f, d | AND W with f | 1 | 00 | 0101 | dfff | ffff | Z | 1,2 |
| CLRF | f | Clear f | 1 | 00 | 0001 | 1fff | ffff | Z | 2 |
| CLRW | - | Clear W | 1 | 00 | 0001 | 0000 | 0011 | Z | |
| COMF | f, d | Complement f | 1 | 00 | 1001 | dfff | ffff | Z | 1,2 |
| DECF | f, d | Decrement f | 1 | 00 | 0011 | dfff | ffff | Z | 1,2 |
| DECFSZ | f, d | Decrement f, Skip if 0 | 1(2) | 00 | 1011 | dfff | ffff | | 1,2,3 |
| INCF | f, d | Increment f | 1 | 00 | 1010 | dfff | ffff | Z | 1,2 |
| INCFSZ | f, d | Increment f, Skip if 0 | 1(2) | 00 | 1111 | dfff | ffff | | 1,2,3 |
| IORWF | f, d | Inclusive OR W with f | 1 | 00 | 0100 | dfff | ffff | Z | 1,2 |
| MOVF | f, d | Move f | 1 | 00 | 1000 | dfff | ffff | Z | 1,2 |
| MOVWF | f | Move W to f | 1 | 00 | 0000 | 1fff | ffff | | |
| NOP | - | No Operation | 1 | 00 | 0000 | 0xx0 | 0000 | | |
| RLF | f, d | Rotate Left f through Carry | 1 | 00 | 1101 | dfff | ffff | C | 1,2 |
| RRF | f, d | Rotate Right f through Carry | 1 | 00 | 1100 | dfff | ffff | C | 1,2 |
| SUBWF | f, d | Subtract W from f | 1 | 00 | 0010 | dfff | ffff | C,DC,Z | 1,2 |
| SWAPF | f, d | Swap nibbles in f | 1 | 00 | 1110 | dfff | ffff | | 1,2 |
| XORWF | f, d | Exclusive OR W with f | 1 | 00 | 0110 | dfff | ffff | Z | 1,2 |
| BIT-ORIENTED FILE REGISTER OPERATIONS | | | | | | | | | |
| BCF | f, b | Bit Clear f | 1 | 01 | 00bb | bfff | ffff | | 1,2 |
| BSF | f, b | Bit Set f | 1 | 01 | 01bb | bfff | ffff | | 1,2 |
| BTFSC | f, b | Bit Test f, Skip if Clear | 1 (2) | 01 | 10bb | bfff | ffff | | 3 |
| BTFSS | f, b | Bit Test f, Skip if Set | 1 (2) | 01 | 11bb | bfff | ffff | | 3 |
| LITERAL AND CONTROL OPERATIONS | | | | | | | | | |
| ADDLW | k | Add literal and W | 1 | 11 | 111x | kkkk | kkkk | C,DC,Z | |
| ANDLW | k | AND literal with W | 1 | 11 | 1001 | kkkk | kkkk | Z | |
| CALL | k | Call subroutine | 2 | 10 | 0kkk | kkkk | kkkk | | |
| CLRWD _T | - | Clear Watchdog Timer | 1 | 00 | 0000 | 0110 | 0100 | $\overline{TO}, \overline{PD}$ | |
| GOTO | k | Go to address | 2 | 10 | 1kkk | kkkk | kkkk | | |
| IORLW | k | Inclusive OR literal with W | 1 | 11 | 1000 | kkkk | kkkk | Z | |
| MOVLW | k | Move literal to W | 1 | 11 | 00xx | kkkk | kkkk | | |
| RETFIE | - | Return from interrupt | 2 | 00 | 0000 | 0000 | 1001 | | |
| RETLW | k | Return with literal in W | 2 | 11 | 01xx | kkkk | kkkk | | |
| RETURN | - | Return from Subroutine | 2 | 00 | 0000 | 0000 | 1000 | | |
| SLEEP | - | Go into standby mode | 1 | 00 | 0000 | 0110 | 0011 | $\overline{TO}, \overline{PD}$ | |
| SUBLW | k | Subtract W from literal | 1 | 11 | 110x | kkkk | kkkk | C,DC,Z | |
| XORLW | k | Exclusive OR literal with W | 1 | 11 | 1010 | kkkk | kkkk | Z | |

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

TABLE 12-1: DEVELOPMENT TOOLS FROM MICROCHIP

| | PIC12CXX | PIC14000 | PIC16C5X | PIC16C6X | PIC16CXX | PIC16F62X | PIC16C7X | PIC16C7XX | PIC16C8X | PIC16F8XX | PIC16C9XX | PIC17C4X | PIC17C7XX | PIC18CXX2 | 24CXX/ 25CXX/ 93CXX | HCSXX | MCRFXX | MCP2510 |
|---------------------------|---|----------|----------|----------|----------|-----------|----------|-----------|----------|-----------|-----------|----------|-----------|-----------|---------------------------|-------|--------|---------|
| Demo Boards and Eval Kits | MPLAB® Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | ✓ |
| | MPLAB® C17 Compiler | | | | | | | | | | | ✓ | ✓ | | | | | |
| | MPLAB® C18 Compiler | | | | | | | | | | | | | ✓ | | | | |
| | MPASM/MPLINK | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Emulators | MPLAB®-ICE | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | PICMASTER/PICMASTER-CE | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| Debugger | ICEPIC™ Low-Cost In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | | | | | | |
| | MPLAB®-ICD In-Circuit Debugger | | | | ✓ | | ✓ | | | ✓ | | | | | | | | |
| Programmers | PICSTART® Plus Low-Cost Universal Dev. Kit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | PRO MATE® II Universal Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Demo Boards and Eval Kits | SIMICE | ✓ | ✓ | ✓ | | | | | | | | | | | | | | |
| | PICDEM-1 | | ✓ | ✓ | | | † | | ✓ | | | ✓ | | | | | | |
| | PICDEM-2 | | | | † | | † | | | | | | | ✓ | | | | |
| | PICDEM-3 | | | | | | | | | | ✓ | | | | | | | |
| | PICDEM-14A | | ✓ | | | | | | | | | | ✓ | | | | | |
| | PICDEM-17 | | | | | | | | | | | | ✓ | | | | | |
| | KEELOO® Evaluation Kit | | | | | | | | | | | | | | ✓ | | | |
| | KEELOO Transponder Kit | | | | | | | | | | | | | | ✓ | | | |
| | microID™ Programmer's Kit | | | | | | | | | | | | | | | ✓ | | |
| | 125 kHz microID Developer's Kit | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz Anticollision microID Developer's Kit | | | | | | | | | | | | | | | | ✓ | |
| | 13.56 MHz Anticollision microID Developer's Kit | | | | | | | | | | | | | | | | ✓ | |
| | MCP2510 CAN Developer's Kit | | | | | | | | | | | | | | | | ✓ | ✓ |

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB®-ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

PIC16CE62X

13.3 DC CHARACTERISTICS:

PIC16CE62X-04 (Commercial, Industrial, Extended)
PIC16CE62X-20 (Commercial, Industrial, Extended)
PIC16LCE62X (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated) | | | | |
|--------------------|-------|--|---|------|-----------------|------|--|
| | | | Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended | | | | |
| | | | Operating voltage VDD range as described in DC spec Table 13-1 | | | | |
| Parm No. | Sym | Characteristic | Min | Typ† | Max | Unit | Conditions |
| D030 | VIL | Input Low Voltage I/O ports with TTL buffer | VSS | – | 0.8V 0.15VDD | V | VDD = 4.5V to 5.5V, Otherwise |
| D031 | | with Schmitt Trigger input | VSS | – | 0.2VDD | V | |
| D032 | | MCLR, RA4/T0CKI, OSC1 (in RC mode) | VSS | – | 0.2VDD | V | Note1 |
| D033 | | OSC1 (in XT and HS) | VSS | – | 0.3VDD | V | |
| | | OSC1 (in LP) | VSS | – | 0.6VDD - 1.0 | V | |
| D040 | VIH | Input High Voltage I/O ports with TTL buffer | 2.0V .25VDD + 0.8V | – | VDD VDD | V | VDD = 4.5V to 5.5V, Otherwise |
| D041 | | with Schmitt Trigger input | 0.8VDD | – | VDD | V | |
| D042 | | MCLR RA4/T0CKI | 0.8VDD | – | VDD | V | |
| D043 | | OSC1 (XT, HS and LP) | 0.7VDD | – | VDD | V | |
| D043A | | OSC1 (in RC mode) | 0.9VDD | – | | | Note1 |
| D070 | IPURB | PORTB weak pull-up current | 50 | 200 | 400 | μA | VDD = 5.0V, VPIN = VSS |
| D060 | IIL | Input Leakage Current (Notes 2, 3) I/O ports (Except PORTA) | – | – | ±1.0 | μA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| D061 | | PORTA | – | – | ±0.5 | μA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| D063 | | RA4/T0CKI | – | – | ±1.0 | μA | VSS ≤ VPIN ≤ VDD |
| | | OSC1, MCLR | – | – | ±5.0 | μA | VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration |
| D080 | VOL | Output Low Voltage I/O ports | – | – | 0.6 | V | IOL=8.5 mA, VDD=4.5V, -40° to $+85^{\circ}\text{C}$ |
| | | | – | – | 0.6 | V | IOL=7.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$ |
| D083 | | OSC2/CLKOUT (RC only) | – | – | 0.6 | V | IOL=1.6 mA, VDD=4.5V, -40° to $+85^{\circ}\text{C}$ |
| | | | – | – | 0.6 | V | IOL=1.2 mA, VDD=4.5V, $+125^{\circ}\text{C}$ |
| D090 | VOH | Output High Voltage (Note 3) I/O ports (Except RA4) | VDD-0.7 | – | – | V | IOH=-3.0 mA, VDD=4.5V, -40° to $+85^{\circ}\text{C}$ |
| | | | VDD-0.7 | – | – | V | IOH=-2.5 mA, VDD=4.5V, $+125^{\circ}\text{C}$ |
| D092 | | OSC2/CLKOUT (RC only) | VDD-0.7 | – | – | V | IOH=-1.3 mA, VDD=4.5V, -40° to $+85^{\circ}\text{C}$ |
| | | | VDD-0.7 | – | – | V | IOH=-1.0 mA, VDD=4.5V, $+125^{\circ}\text{C}$ |
| *D150 | VOD | Open-Drain High Voltage | | | 8.5 | V | RA4 pin |
| D100 | COSC2 | Capacitive Loading Specs on Output Pins OSC2 pin | | | 15 | pF | In XT, HS and LP modes when external clock used to drive OSC1. |
| D101 | Cio | All I/O pins/OSC2 (in RC mode) | | | 50 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16CE62X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

FIGURE 13-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

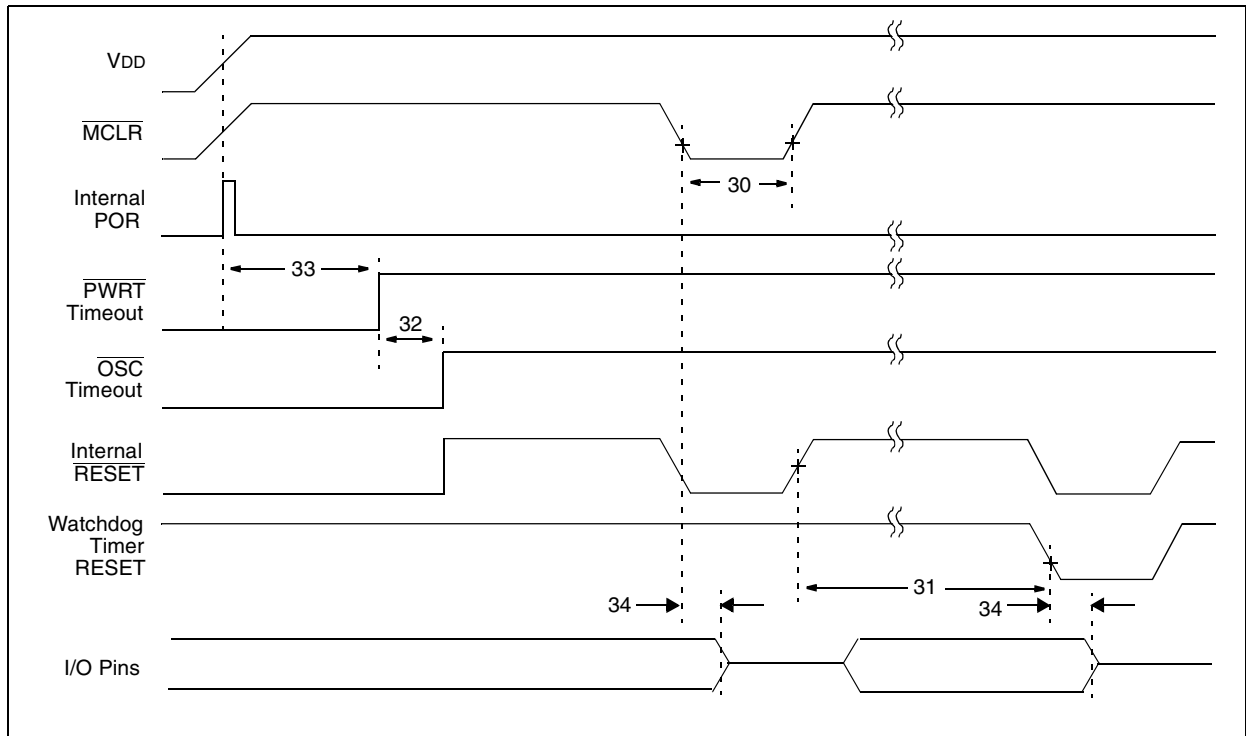


FIGURE 13-8: BROWN-OUT RESET TIMING

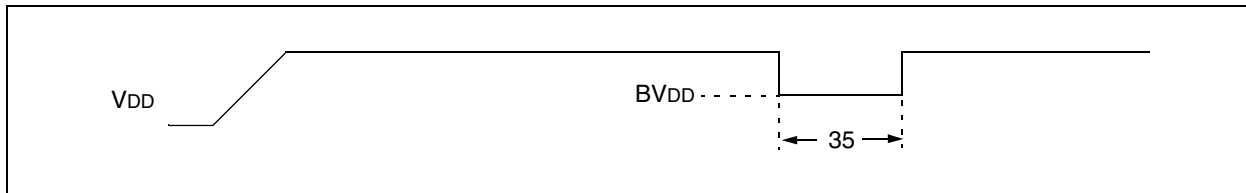


TABLE 13-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---------------|-------|---|------|-----------|------|-------|---------------------------|
| 30 | Tmcl | MCLR Pulse Width (low) | 2000 | — | — | ns | -40° to +85°C |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7* | 18 | 33* | ms | VDD = 5.0V, -40° to +85°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| 33 | Tpwrt | Power-up Timer Period | 28* | 72 | 132* | ms | VDD = 5.0V, -40° to +85°C |
| 34 | Tioz | I/O hi-impedance from MCLR low | — | — | 2.0 | μs | |
| 35 | TBOR | Brown-out Reset Pulse Width | 100* | — | — | μs | 3.7V ≤ VDD ≤ 4.3V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-9: TIMER0 CLOCK TIMING

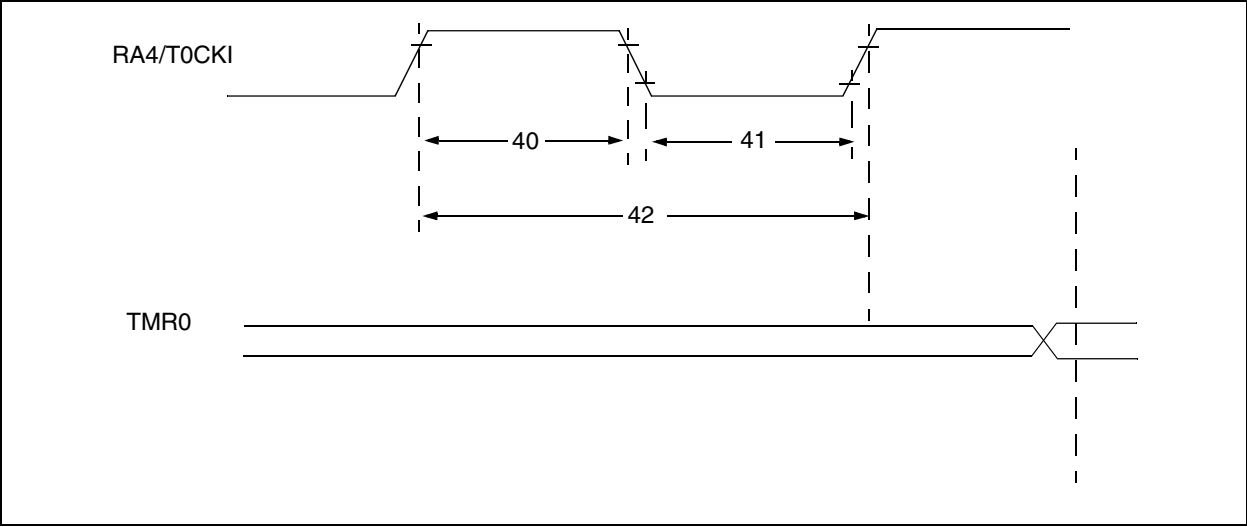


TABLE 13-6: TIMER0 CLOCK REQUIREMENTS

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---------------|------|------------------------|----------------|---------------------------|------|-----|-------|--|
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | $0.5 T_{CY} + 20^*$ | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | $0.5 T_{CY} + 20^*$ | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | | $\frac{T_{CY} + 40^*}{N}$ | — | — | ns | N = prescale value (1, 2, 4, ..., 256) |

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

13.6 EEPROM Timing

FIGURE 13-10: BUS TIMING DATA

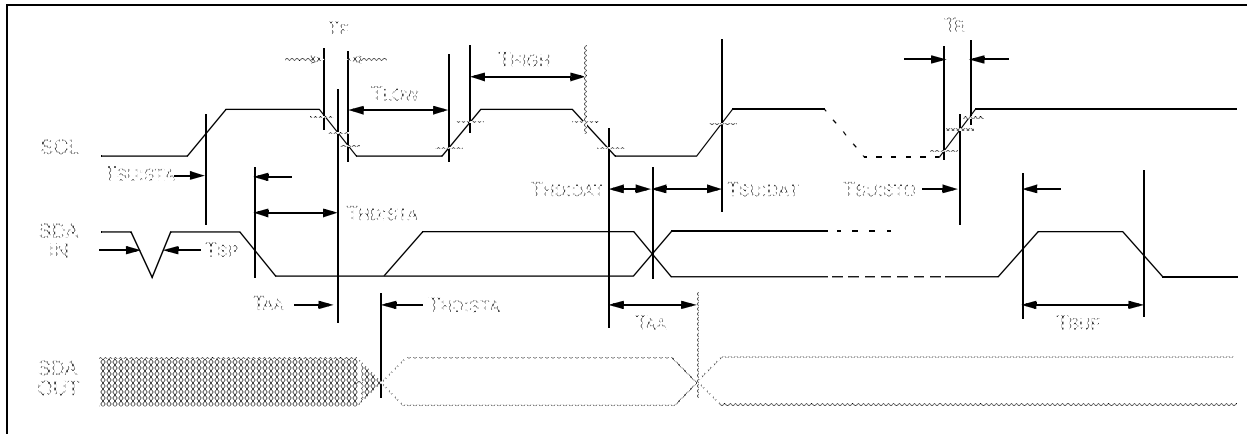


TABLE 13-7: AC CHARACTERISTICS

| Parameter | Symbol | STANDARD MODE | | Vcc = 4.5 - 5.5V FAST MODE | | Units | Remarks |
|---|---------|---------------|------|----------------------------|------|--------|---|
| | | Min. | Max. | Min. | Max. | | |
| Clock frequency | FCLK | — | 100 | — | 400 | kHz | |
| Clock high time | THIGH | 4000 | — | 600 | — | ns | |
| Clock low time | TLOW | 4700 | — | 1300 | — | ns | |
| SDA and SCL rise time | TR | — | 1000 | — | 300 | ns | (Note 1) |
| SDA and SCL fall time | TF | — | 300 | — | 300 | ns | (Note 1) |
| START condition hold time | THD:STA | 4000 | — | 600 | — | ns | After this period the first clock pulse is generated |
| START condition setup time | TSU:STA | 4700 | — | 600 | — | ns | Only relevant for repeated START condition |
| Data input hold time | THD:DAT | 0 | — | 0 | — | ns | (Note 2) |
| Data input setup time | TSU:DAT | 250 | — | 100 | — | ns | |
| STOP condition setup time | TSU:STO | 4000 | — | 600 | — | ns | |
| Output valid from clock | TAA | — | 3500 | — | 900 | ns | (Note 2) |
| Bus free time | TBUF | 4700 | — | 1300 | — | ns | Time the bus must be free before a new transmission can start |
| Output fall time from VIH minimum to VIL maximum | TOF | — | 250 | 20 + 0.1 CB | 250 | ns | (Note 1), CB ≤ 100 pF |
| Input filter spike suppression (SDA and SCL pins) | TSP | — | 50 | — | 50 | ns | (Note 3) |
| Write cycle time | TWR | — | 10 | — | 10 | ms | Byte or Page mode |
| Endurance | — | 10M 1M | — | 10M 1M | — | cycles | 25°C, Vcc = 5.0V, Block Mode (Note 4) |

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

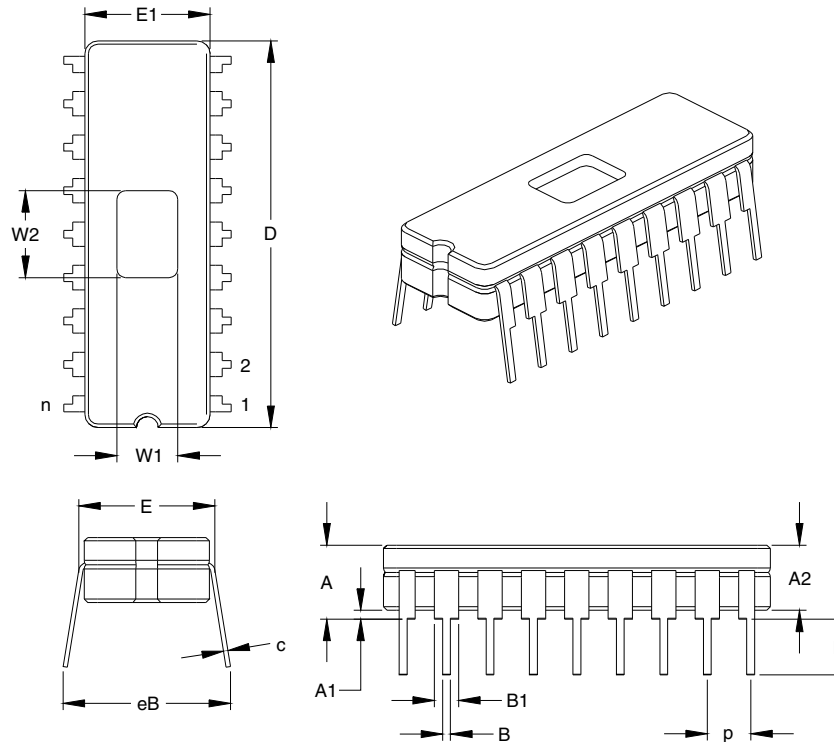
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

Note 4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

14.0 PACKAGING INFORMATION

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES* | | | MILLIMETERS | | |
|----------------------------|----|---------|------|------|-------------|-------|-------|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .170 | .183 | .195 | 4.32 | 4.64 | 4.95 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .023 | .030 | 0.38 | 0.57 | 0.76 |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Ceramic Pkg. Width | E1 | .285 | .290 | .295 | 7.24 | 7.37 | 7.49 |
| Overall Length | D | .880 | .900 | .920 | 22.35 | 22.86 | 23.37 |
| Tip to Seating Plane | L | .125 | .138 | .150 | 3.18 | 3.49 | 3.81 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .055 | .060 | 1.27 | 1.40 | 1.52 |
| Lower Lead Width | B | .016 | .019 | .021 | 0.41 | 0.47 | 0.53 |
| Overall Row Spacing | eB | .345 | .385 | .425 | 8.76 | 9.78 | 10.80 |
| Window Width | W1 | .130 | .140 | .150 | 3.30 | 3.56 | 3.81 |
| Window Length | W2 | .190 | .200 | .210 | 4.83 | 5.08 | 5.33 |

*Controlling Parameter
JEDEC Equivalent: MO-036
Drawing No. C04-010

PIC16CE62X

NOTES:

PIC16XXXXXX FAMILY

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