# E·XFL



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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lce623t-04e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### TABLE 1-1: PIC16CE62X FAMILY OF DEVICES

		PIC16CE623	PIC16CE624	PIC16CE625
Clock	Maximum Frequency of Operation (MHz)	20	20	20
Momory	EPROM Program Memory (x14 words)	512	1K	2K
Welliory	Data Memory (bytes)	96	96	128
	EEPROM Data Memory (bytes)	128	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2
	Internal Reference Voltage	Yes	Yes	Yes
	Interrupt Sources	4	4	4
	I/O Pins	13	13	13
	Voltage Range (Volts)	2.5-5.5	2.5-5.5	2.5-5.5
Features	Brown-out Reset	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC<sup>®</sup> Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16CE62X Family devices use serial programming with clock pin RB6 and data pin RB7.

### 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CE62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CE62X uses a Harvard architecture in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM) and non-volatile memory (EEPROM) for each PIC16CE62X device.

Device	Program Memory	RAM Data Memory	EEPROM Data Memory	
PIC16CE623	512x14	96x8	128x8	
PIC16CE624	1Kx14	96x8	128x8	
PIC16CE625	2Kx14	128x8	128x8	

The PIC16CE62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CE62X family has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CE62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CE62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

### 5.0 I/O PORTS

The PIC16CE62X parts have two ports, PORTA and PORTB. Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

### 5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Port RA4 is multiplexed with the TOCKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers), which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a hi- impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The PORTA pins are multiplexed with comparator and voltage reference functions. The operation of these pins are selected by control bits in the CMCON (Comparator Control Register) register and the VRCON (Voltage Reference Control Register) register. When selected as a comparator input, these pins will read as '0's.

#### FIGURE 5-1: BLOCK DIAGRAM OF RA<1:0> PINS



Note:	On reset, the TRISA register is set to all
	inputs. The digital inputs are disabled and
	the comparator inputs are forced to ground
	to reduce excess current consumption.

TRISA controls the direction of the RA pins, even when they are being used as comparator inputs. The user must make sure to keep the pins configured as inputs when using them as comparator inputs.

The RA2 pin will also function as the output for the voltage reference. When in this mode, the VREF pin is a very high impedance output. The user must configure TRISA<2> bit as an input and use high impedance loads.

In one of the comparator modes defined by the CMCON register, pins RA3 and RA4 become outputs of the comparators. The TRISA<4:3> bits must be cleared to enable outputs to use this function.

#### **EXAMPLE 5-1: INITIALIZING PORTA**

CLRF	PORTA	;Initialize PORTA by setting
		;output data latches
MOVLW	0X07	;Turn comparators off and
MOVWF	CMCON	;enable pins for I/O
		;functions
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x1F	;Value used to initialize
		;data direction
MOVWF	TRISA	;Set RA<4:0> as inputs
		;TRISA<7:5> are always
		;read as '0'.

#### FIGURE 5-2: BLOCK DIAGRAM OF RA2 PIN



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### TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other Resets
05h	PORTA	—	_	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	—	—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT		—	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged

Note: Shaded bits are not used by PORTA.

#### 5.3 <u>I/O Programming Considerations</u>

#### 5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read modify write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (i.e.,  ${\tt BCF}\,,\,\,{\tt BSF},\, etc.)$  on an I/O port.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

#### EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

; Initial PORT settings: PORTB<7:4> Inputs ; PORTB<3:0> Outputs ; ; PORTB<7:6> have external pull-up and are not ; connected to other circuitry ; PORT latch PORT pins ; ; BCF PORTB. 7 ; 01pp pppp 11pp pppp BCF PORTB, 6 ; 10pp pppp 11pp pppp BSF STATUS, RPO ; BCF TRISB, 7 ; 10pp pppp 11pp pppp BCF TRISB, 6 ; 10pp pppp 10pp pppp ; ; Note that the user may have expected the pin

; values to be 00pp pppp. The 2nd BCF caused ; RB7 to be latched as the pin value (High).

#### 5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with an NOP or another instruction not accessing this I/O port.



#### FIGURE 5-7: SUCCESSIVE I/O OPERATION

#### 7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

#### 7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



#### FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

The code example in Example 8-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

#### EXAMPLE 8-1: INITIALIZING COMPARATOR MODULE

FLAG_REG	EQU	0X20
CLRF	FLAG_REG	;Init flag register
CLRF	PORTA	;Init PORTA
MOVF	CMCON,W	;Move comparator contents to W
ANDLW	0xC0	;Mask comparator bits
IORWF	FLAG_REG,F	;Store bits in flag register
MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON, F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON,GIE	;Global interrupt enable

#### 8.2 Comparator Operation

A single comparator is shown in Figure 8-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN–, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN–, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 8-2 represent the uncertainty due to input offsets and response time.

#### 8.3 <u>Comparator Reference</u>

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN– is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 8-2).

FIGURE 8-2: SINGLE COMPARATOR



#### 8.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD and can be applied to either pin of the comparator(s).

#### 8.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 13, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 8-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

#### 10.9 <u>Code Protection</u>

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip	does	not	recommend	code
	protecting	windov	ved d	evices.	

#### 10.10 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. Only the least significant 4 bits of the ID locations are used.

#### 10.11 In-Circuit Serial Programming

The PIC16CE62X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low, while raising the MCLR (VPP) pin from VIL to VIHH (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X/9XX Programming Specifications (Literature #DS30228).

A typical in-circuit serial programming connection is shown in Figure 10-20.

#### FIGURE 10-20: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

#### 12.17 <u>SEEVAL Evaluation and Programming</u> <u>System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials<sup>™</sup> and secure serials. The Total Endurance<sup>™</sup> Disk is included to aid in tradeoff analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

### 12.18 <u>KEELOQ Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

#### 13.2 DC CHARACTERISTICS: F

#### PIC16LCE62X-04 (Commercial, Industrial)

			Standard Operating Conditions (unless otherwise stated)						
DC CH		STICS	Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \le \text{TA} \le +70^{\circ}\text{C}$ for comparatel and						
						-4	$0^{\circ}C \leq TA \leq +125^{\circ}C$ for extended		
Param	Sym	Characteristic	Min	Typ†	Max	Units	Conditions		
No.									
D001	Vdd	Supply Voltage	2.5	-	5.5	V	See Figure 13-1 through Figure 13-3		
D002	Vdr	RAM Data Retention Voltage (Note 1)	-	1.5*	-	V	Device in SLEEP mode		
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	-	V	See section on power-on reset for details		
D004	SVDD	VDD rise rate to ensure Power-on Reset	.05*	-	-	V/ms	See section on power-on reset for details		
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared		
D010	IDD	Supply Current (Note 2)	-	1.2	2.0	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled,		
							XT osc mode, (Note 4)*		
			-	_	1.1	mA	FOSC = 4 MHZ, $VDD = 2.5V$ , $WDT$ disabled, XT osc mode (Note 4)		
			_	35	70	μA	Fosc = $32 \text{ kHz}$ , VDD = 2.5V, WDT disabled,		
						•	LP osc mode		
D020	IPD	Power Down Current (Note 3)	-	-	2.0	μA	VDD = 2.5V		
			-	-	2.2	μA	VDD = 3.0V*		
			-	-	9.0	μA	VDD = 5.5V		
Dooo	Alwor		_	-	10	μΑ			
D022	AIWDT	WDT Current (Note 5)	-	6.0	10	μΑ	VDD=4.0V (125°C)		
D022A	AIBOB	Brown-out Beset Current	_	75	125	μΑ	$\frac{(123)}{BOD}$ enabled, VDD = 5.0V		
	2.001	(Note 5)			0	po t			
D023	$\Delta$ ICOMP	Comparator Current for each	-	30	60	μA	VDD = 4.0V		
00004		Comparator (Note 5)		80	105	A	$V_{DD} = 4.0 V_{c}$		
DUZSA		Operating Current	_	80	135	μA mA	$V_{DD} = 4.0V$		
		Operating Current	_		3 1	mA	VCC = 5.5V, SCL = 400 KHZ		
		Standby Current	_		30	uА	$V_{CC} = 3.0V$ . EE VDD = VCC		
	$\Delta IEE$	Standby Current	-		100	μA	VCC = 3.0V, EE VDD = VCC		
1A	Fosc	LP Oscillator Operating Frequency	0		200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures		

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in k $\Omega$ .

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

### FIGURE 13-9: TIMER0 CLOCK TIMING



#### **TABLE 13-6:** TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	_	_	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		<u>Tcy + 40</u> * N			ns	N = prescale value (1, 2, 4,, 256)

t

These parameters are characterized but not tested. Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### 13.6 EEPROM Timing





Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK		100		400	kHz	
Clock high time	Thigh	4000	—	600	_	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	_	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	_	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0		0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	_	ns	
STOP condition setup time	Tsu:sto	4000	—	600	_	ns	
Output valid from clock	ΤΑΑ	_	3500	_	900	ns	(Note 2)
Bus free time	TBUF	4700		1300	_	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VI∟ maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), $CB \le 100 \text{ pF}$
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	_	50	ns	(Note 3)
Write cycle time	Twr	—	10	_	10	ms	Byte or Page mode
Endurance	_	10M 1M	-	10M 1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

#### TABLE 13-7: AC CHARACTERISTICS

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

### APPENDIX A: CODE FOR ACCESSING EEPROM DATA MEMORY

Please check our web site at www.microchip.com for code availability.

### APPENDIX B:REVISION HISTORY

Revision D (January 2013)

Added a note to each package outline drawing.

#### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Printed on recycled paper.

ISBN: 9781620769768

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