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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lce624t-04e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CE62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CE62X uses a Harvard architecture in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM) and non-volatile memory (EEPROM) for each PIC16CE62X device.

Device	Program Memory	RAM Data Memory	EEPROM Data Memory
PIC16CE623	512x14	96x8	128x8
PIC16CE624	1Kx14	96x8	128x8
PIC16CE625	2Kx14	128x8	128x8

The PIC16CE62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CE62X family has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CE62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CE62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-7Fh (Bank0) on the PIC16CE623/624 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16CE625 are General Purpose Registers implemented as static RAM. Some special purpose registers are mapped in Bank 1. In all three microcontrollers, address space F0h-FFh (Bank1) is mapped to 70-7Fh (Bank0) as common RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 96×8 in the PIC16CE623/624 and 128 x 8 in the PIC16CE625. Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).









6.0 EEPROM PERIPHERAL OPERATION

The PIC16CE623/624/625 each have 128 bytes of EEPROM data memory. The EEPROM data memory supports a bi-directional, 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), and are mapped to bit1 and bit2, respectively, of the EEINTF register (SFR 90h). In addition, the power to the EEPROM can be controlled using bit0 (EEVDD) of the EEINTF register. For most applications, all that is required is calls to the following functions:

;	Byte_Write: Byte write routine
;	Inputs: EEPROM Address EEADDR
;	EEPROM Data EEDATA
;	Outputs: Return 01 in W if OK, else
;	return 00 in W
;	
;	Read_Current: Read EEPROM at address
cι	irrently held by EE device.
;	Inputs: NONE
;	Outputs: EEPROM Data EEDATA
;	Return 01 in W if OK, else
;	return 00 in W
;	
;	Read_Random: Read EEPROM byte at supplied
;	address
;	Inputs: EEPROM Address EEADDR
;	Outputs: EEPROM Data EEDATA
;	Return 01 in W if OK,
;	else return 00 in W

The code for these functions is available on our web site (www.microchip.com). The code will be accessed by either including the source code FL62XINC.ASM or by linking FLASH62X.ASM. FLASH62.IMC provides external definition to the calling program.

6.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the memory.

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

6.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer to and from the memory.

6.0.3 EEINTF REGISTER

The EEINTF register (SFR 90h) controls the access to the EEPROM. Register 6-1 details the function of each bit. User code must generate the clock and data signals.

REGISTER 6-1: EEINTF REGISTER (ADDRESS 90h)

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1		
	—	_	_	_	EESCL	EESDA	EEVDD	R = Readable bit	
bit7	bit0 W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset								
bit 7-3:	Unimplen	nented: F	lead as '0'						
bit 2:	EESCL: Clock line to the EEPROM 1 = Clock high 0 = Clock low								
bit 1:	EESDA : Data line to EEPROM 1 = Data line is high (pin is tri-stated, line is pulled high by a pull-up resistor) 0 = Data line is low								
bit 0:	EEVDD : VDD control bit for EEPROM 1 = VDD is turned on to EEPROM 0 = VDD is turned off to EEPROM (all pins are tri-stated and the EEPROM is powered down)								
Note:	EESDA, EESCL and EEVDD will read '0' if EEVDD is turned off.								



6.5 <u>Read Operation</u>

Read operations are initiated in the same way as write operations with the exception that the R/\overline{W} bit of the EEPROM address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.6 Current Address Read

The EEPROM contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the EEPROM address with R/W bit set to one, the EEPROM issues an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-7).

6.7 Random Read

Random read operations allow the processor to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the EEPROM as part of a write operation. After the word address is sent, the processor generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the processor issues the control byte again, but with the R/W bit set to a one. The EEPROM will then issue an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer, but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-8).

6.8 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the EEPROM transmits the first data byte, the processor issues an acknowledge as opposed to a stop condition in a random read. This directs the EEPROM to transmit the next sequentially addressed 8-bit word (Figure 6-9).

To provide sequential reads, the EEPROM contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.9 Noise Protection

The EEPROM employs a Vcc threshold detector circuit, which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits, which suppress noise spikes to assure proper device operation even on a noisy bus.





FIGURE 6-8: RANDOM READ

BUS ACTIVITY

. .

A C K

DATAn



DATAn + 1

DATAn + 2

N O

A C K

DATAn + X

7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

8.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The on-chip voltage reference (Section 9.0) can also be an input to the comparators.

The CMCON register, shown in Register 8-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 8-1.

R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0				
C2OU1	C10UT			CIS	CM2	CM1	CM0	R = Readable bit			
bit7							bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset			
bit 7:	C2OUT : Con 1 = C2 VIN+ 0 = C2 VIN+	C2OUT : Comparator 2 output 1 = C2 VIN+ > C2 VIN- 0 = C2 VIN+ < C2 VIN-									
bit 6:	C1OUT: Col 1 = C1 VIN+ 0 = C1 VIN+	C1OUT : Comparator 1 output 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN-									
bit 5-4:	Unimpleme	ented: F	lead as	'0'							
bit 3:	CIS: Comparator Input Switch When $CM<2:0>:=001:$ 1 = C1 VIN- connects to RA3 0 = C1 VIN- connects to RA0 When $CM<2:0>=010:$ 1 = C1 VIN- connects to RA3 C2 VIN- connects to RA2 0 = C1 VIN- connects to RA0 C2 VIN- connects to RA0										
bit 2-0:	CM<2:0> : C Figure 8-1.	Compara	ator moo	le							

REGISTER 8-1: CMCON REGISTER (ADDRESS 1Fh)

8.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
- b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

8.7 <u>Comparator Operation During SLEEP</u>

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

8.8 Effects of a RESET

A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

8.9 <u>Analog Input Connection</u> <u>Considerations</u>

A simplified circuit for an analog input is shown in Figure 8-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.



FIGURE 8-4: ANALOG INPUT MODEL

10.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (i.e. W register and STATUS register). This will have to be implemented in software.

Example 10-1 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x70 in Bank 0 and it must also be defined at 0xF0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 10-1:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- · Restores the W register

EXAMPLE 10-1: SAVING THE STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;copy W to temp register, ;could be in either bank
SWAPF	STATUS,W	;swap status to be saved into $\ensuremath{\mathtt{W}}$
BCF	STATUS, RPO	;change to bank 0 regardless ;of current bank
MOVWF	STATUS_TEMP	;save status to bank 0 ;register
:		
:	(ISR)	
:		
SWAPF	STATUS_TEMP,W	;swap STATUS_TEMP register ;into W, sets bank to original ;state
MOVWF	STATUS	;move W into STATUS register
SWAPF	W_TEMP,F	;swap W_TEMP
SWAPF	W_TEMP,W	;swap W_TEMP into W

10.7 <u>Watchdog Timer (WDT)</u>

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device have been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 10.1).

10.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

10.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

11.0 INSTRUCTION SET SUMMARY

Each PIC16CE62X instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CE62X instruction set summary in Table 11-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 11-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 11-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with $x = 0$. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination either the W register or the specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
<>	Register bit field
∈	In the set of
italics	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Table 11-1 lists the instructions recognized by the MPASM assembler.

Figure 11-1 shows the three general formats that the instructions can have.

Note:	То	maintain	upward	compatibility	with		
	future PIC [®] MCU products, do not use th						
	OP	TION and 1	TRIS inst	ructions.			

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS



^{13 11 10} OPCODE k (literal)

k = 11-bit immediate value

PIC16CE62X

CLRWDT	Clear Watchdog Timer					
Syntax:	[label] CLRWDT					
Operands:	None					
Operation:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \end{array}$					
Status Affected:	TO, PD					
Encoding:	00 0000 0110 0100					
	Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.					
Words:	1					
Cycles:	1					
Example	CLRWDT					
	Before Instruction WDT counter = ? After Instruction WDT counter = $0x00$ WDT prescaler= 0 TO = 1 PD = 1					
COMF	Complement f					
Syntax:	[label] COME fd					

COMI	oomplement						
Syntax:	[label] COMF f,d						
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$						
Operation:	$(\overline{f}) \rightarrow (dest)$						
Status Affected:	Z						
Encoding:	00 1001 dfff ffff						
Description:	complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example	COMF REG1,0						
	Before Instruction REG1 = 0x13 After Instruction REG1 = 0x13 W = 0xEC						

DECF	Decreme	ent f			
Syntax:	[label] DECF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	(f) - 1 \rightarrow	(dest)			
Status Affected:	Z				
Encoding:	00	0011	df	ff	ffff
Description:	Decremen result is st is 1, the re ter 'f'.	t register ored in th sult is sto	'f'. If e W i ored b	'd' is (regist back i), the er. If 'd' n regis-
Words:	1				
Cycles:	1				
Example	DECF	CNT,	1		
	Before In After Inst	struction CNT Z ruction CNT Z	= =	0x01 0 0x00 1)

DECFSZ	Decrement f, Skip if 0					
Syntax:	[label] DECFSZ f,d					
Operands:	$0 \le f \le 127$ $d \in [0,1]$					
Operation:	(f) - 1 \rightarrow (dest); skip if result = 0					
Status Affected:	None					
Encoding:	00 1011 dfff ffff					
Description:	decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.					
Words:	1					
Cycles:	1(2)					
Example	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • •					
	$\begin{array}{rcl} Before \ Instruction \\ PC &= & address \ {\tt HERE} \\ After \ Instruction \\ CNT &= & CNT - 1 \\ if \ CNT &= & 0, \\ PC &= & address \ {\tt CONTINUE} \\ if \ CNT \neq & 0, \\ PC &= & address \ {\tt HERE+1} \\ \end{array}$					

TABLE 12-1: DEVELOPMENT TOOLS FROM MICROCHIP

Metallicity (Metallicity) Metallicity (Metallicity) Me		PIC12CXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	X7281519	XX7Oðfolg	PIC16C8X	PIC16F8XX	PIC16C9XX	X4071019	XX7371319	PIC18CXX2	63CXX 52CXX/ 54CXX/	хххзэн	MCRFXXX	MCP2510
Bit Add C 17 Complex Source in the contraction of the control of the co	MPLAB [®] Integrated Development Environment	^	~	>	>	>	>	>	>	>	>	>	>	>	>				
MAME Complex Image Complex Comple	MPLAB [®] C17 Compiler												>	>					
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PICHARGE /<	MPLAB [®] -ICE	>	>	>	>	>	** ^	>	>	>	>	>	>	>	>				
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** Contact Microchip Technology Inc. for availability [†] Development tool is available on select devices.

PIC16CE62X

NOTES:

13.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.0V
Voltage on RA4 with respect to Vss	8.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	8.5V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into Vod pin	250 mA
Input Clamp Current, Iк (Vi <0 or Vi> VDD)	±20 mA
Output Clamp Current, Iок (Vo <0 or Vo>VDD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA and PORTB	200 mA
Maximum Current sourced by PORTA and PORTB	200 mA
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum {(VD	D-VOH) x IOH} + \sum (VOI x IOL)

2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100³/₄ should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16CE62X



20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		N	1ILLIMETERS	6
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.66	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	с	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150

Drawing No. C04-072

APPENDIX A: CODE FOR ACCESSING EEPROM DATA MEMORY

Please check our web site at www.microchip.com for code availability.

APPENDIX B:REVISION HISTORY

Revision D (January 2013)

Added a note to each package outline drawing.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

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- General Technical Support Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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- Technical Support

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Technical support is available through the web site at: http://microchip.com/support

PIC16CE62X PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NOXX X /XX XXX		
Pattern:	3-Digit Pattern Code for QTP (blank otherwise)	
Package:	P = PDIP SO = SOIC (Gull Wing, 300 mil body)	
	JW* = Windowed CERDIP Example a) PIC10	es: 6CE623-04/P301 =
Temperature Range:	$\begin{array}{rcl} - & = & 0^{\circ} \mathbb{C} \text{ to } + 70^{\circ} \mathbb{C} & & & \mathbb{C} \text{ Comm} \\ \mathbb{I} & = & -40^{\circ} \mathbb{C} \text{ to } + 85^{\circ} \mathbb{C} & & & \text{age,} \\ \mathbb{E} & = & -40^{\circ} \mathbb{C} \text{ to } + 125^{\circ} \mathbb{C} & & & \mathbb{Q} \text{ TP} \\ \end{array}$	4 MHz, normal VDD limits, pattern #301. 6CE623-04I/SO =
Frequency Range:	04=200kHz (LP osc)Indus04=4 MHz (XT and RC osc)age, 420=20 MHz (HS osc)its.	strial temp., SOIC pack- 4MHz, industrial VDD lim-
Device:	PIC16CE62X :VDD range 3.0V to 5.5V PIC16CE62XT:VDD range 3.0V to 5.5V (Tape and R	leel)

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)