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#### Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lce625t-04i-so

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### TABLE 1-1: PIC16CE62X FAMILY OF DEVICES

		PIC16CE623	PIC16CE624	PIC16CE625
Clock	Maximum Frequency of Operation (MHz)	20	20	20
Momory	EPROM Program Memory (x14 words)	512	1K	2K
Welliory	Data Memory (bytes)	96	96	128
	EEPROM Data Memory (bytes)	128	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2
	Internal Reference Voltage	Yes	Yes	Yes
	Interrupt Sources	4	4	4
	I/O Pins	13	13	13
	Voltage Range (Volts)	2.5-5.5	2.5-5.5	2.5-5.5
Features	Brown-out Reset	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC<sup>®</sup> Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16CE62X Family devices use serial programming with clock pin RB6 and data pin RB7.

#### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM. The special registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other resets <sup>(1)</sup>
Bank 0											
00h	INDF	Addressin register)	ig this locat	ion uses co	ontents of F	SR to addre	ess data me	emory (not a	a physical	xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 M	odule's Reg	jister						xxxx xxxx	uuuu uuuu
02h	PCL	Program (	Counter's (F	PC) Least S	Significant B	yte				0000 0000	0000 0000
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h	FSR	Indirect da	ata memory	address p	ointer					xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									_	-
08h	Unimplemented									-	-
09h	Unimplemented									-	-
0Ah	PCLATH	—	—	—	Write buff	er for upper	5 bits of pr	ogram cou	nter	0 0000	0 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	_	—	-0	- 0
0Dh-1Eh	Unimplemented									-	-
1Fh	CMCON	C2OUT	C10UT		—	CIS	CM2	CM1	CM0	00 0000	00 0000
Bank 1											
80h	INDF	Addressin register)	ig this locat	ion uses co	ontents of F	SR to addre	ess data me	emory (not a	a physical	XXXX XXXX	XXXX XXXX
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program (	Counter's (F	PC) Least S	Significant B	yte				0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h	FSR	Indirect da	ata memory	address p	ointer					xxxx xxxx	uuuu uuuu
85h	TRISA	—	—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									_	-
88h	Unimplemented									_	_
89h	Unimplemented									_	_
8Ah	PCLATH	—	_	_	Write buff	er for upper	5 bits of pr	ogram cou	nter	0 0000	0 0000
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	—	CMIE	_	_	—	_	_	_	-0	- 0
8Dh	Unimplemented									_	_
8Eh	PCON	—	—	_	_	—	_	POR	BOD	0x	uq
8Fh-9Eh	Unimplemented									-	_
90h	EEINTF	_	—	—	—	_	EESCL	EESDA	EEVDD	111	111
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

#### TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16CE62X

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) resets include MCLR reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

Note 2: IRP & RPI bits are reserved; always maintain these bits clear.

#### 4.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 4-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the status register as 000uu1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any status bit. For other instructions, not affecting any status bits, see the "Instruction Set Summary".

Note 1:	The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16CE62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
Note 2:	The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

### REGISTER 4-1: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
IRP bit7	RP1	RP0	TO	PD	Z	DC	C bit0	R = Readable bit W = Writable bit
								U = Unimplemented bit, read as '0'
								-n = Value at POR reset -x = Unknown at POR reset
bit 7:	IRP: The IF	RP bit is r	eserved or	the PIC1	6CE62X, a	lways mair	ntain this bit	t clear.
bit 6:5	<b>RP&lt;1:O&gt;:</b> 11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	Register 3 (180h - 2 (100h - 1 (80h - 1 0 (00h - 1 is 128 by	Bank Sele 1FFh) 17Fh) FFh) 7Fh) rtes. The R	ct bits (use P1 bit is re	ed for direc	t addressin ways maint	g) tain this bit d	clear.
bit 4:	<b>TO</b> : Time-o 1 = After po 0 = A WDT	out bit ower-up, <sup>-</sup> time-out	CLRWDT in	struction, o	or sleep ii	nstruction		
bit 3:	<b>PD</b> : Power- 1 = After po 0 = By exe	-down bit ower-up c cution of	or by the CI the SLEEP	LRWDT instruction	truction			
bit 2:	<b>Z</b> : Zero bit 1 = The res 0 = The res	sult of an sult of an	arithmetic arithmetic	or logic op or logic op	peration is a	zero not zero		
bit 1:	<b>DC</b> : Digit c 1 = A carry 0 = No carr	arry/borro v-out from ry-out fro	bw bit (ADD the 4th low m the 4th l	WF, ADDLW w order bit ow order b	of the result of the result	SUBWF instr ult occurred sult	uctions) (for I	or borrow the polarity is reversed)
bit 0:	C: Carry/bc 1 = A carry 0 = No carr Note: For b second ope the source	orrow bit -out from ry-out from porrow the erand. Fo register.	(ADDWF, AD the most s m the mos e polarity is r rotate (RH	DLW, SUB: significant t significan s reversed RF, RLF) in	LW, SUBWF bit of the ro t bit of the . A subtrac structions,	instructior esult occurr result occu tion is exec this bit is lo	ns) red urred suted by add baded with e	ding the two's complement of the either the high or low order bit of

NOTES:

#### 6.3 Write Operations

#### BYTE WRITE 6.3.1

Following the start signal from the processor, the device code (4 bits), the don't care bits (3 bits), and the R/W bit, which is a logic low, is placed onto the bus by the processor. This indicates to the EEPROM that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the processor is the word address and will be written into the address pointer of the EEPROM. After receiving another acknowledge signal from the EEPROM, the processor will transmit the data word to be written into the addressed memory location. The EEPROM acknowledges again and the processor generates a stop condition. This initiates the internal write cycle, and during this time, the EEPROM will not generate acknowledge signals (Figure 6-5).

#### 6.3.2 PAGE WRITE

The write control byte, word address and the first data byte are transmitted to the EEPROM in the same way as in a byte write. But instead of generating a stop condition, the processor transmits up to eight data bytes to the EEPROM, which are temporarily stored in the onchip page buffer and will be written into the memory after the processor has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the processor should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-6).

#### 6.4 Acknowledge Polling

Since the EEPROM will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the processor, the EEPROM initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the processor sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the processor can then proceed with the next read or write command. See Figure 6-4 for flow diagram.

#### FIGURE 6-4: ACKNOWLEDGE POLLING FLOW





#### FIGURE 6-5:

#### 7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

#### 7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



#### FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

#### 7.3 <u>Prescaler</u>

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (i.e., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



#### FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

The code example in Example 8-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

#### EXAMPLE 8-1: INITIALIZING COMPARATOR MODULE

FLAG_REG	EQU	0X20
CLRF	FLAG_REG	;Init flag register
CLRF	PORTA	;Init PORTA
MOVF	CMCON,W	;Move comparator contents to W
ANDLW	0xC0	;Mask comparator bits
IORWF	FLAG_REG,F	;Store bits in flag register
MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON, F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON,GIE	;Global interrupt enable

#### 8.2 Comparator Operation

A single comparator is shown in Figure 8-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN–, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN–, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 8-2 represent the uncertainty due to input offsets and response time.

#### 8.3 <u>Comparator Reference</u>

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN– is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 8-2).

FIGURE 8-2: SINGLE COMPARATOR



#### 8.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD and can be applied to either pin of the comparator(s).

#### 8.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 13, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 8-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

#### 8.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
- b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

### 8.7 <u>Comparator Operation During SLEEP</u>

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

#### 8.8 Effects of a RESET

A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

#### 8.9 <u>Analog Input Connection</u> <u>Considerations</u>

A simplified circuit for an analog input is shown in Figure 8-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k $\Omega$  is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.



#### FIGURE 8-4: ANALOG INPUT MODEL

#### EXAMPLE 9-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	;	4 Inputs Muxed
MOVWF	CMCON	;	to 2 comps.
BSF	STATUS, RPO	;	go to Bank 1
MOVLW	0x07	;	RA3-RA0 are
MOVWF	TRISA	;	outputs
MOVLW	0xA6	;	enable VREF
MOVWF	VRCON	;	low range
		;	set VR<3:0>=6
BCF	STATUS, RPO	;	go to Bank 0
CALL	DELAY10	;	10µs delay

#### 9.2 <u>Voltage Reference Accuracy/Error</u>

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 9-1) keep VREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The absolute accuracy of the Voltage Reference can be found in Table 13-2.

#### 9.3 Operation During Sleep

When the device wakes up from sleep through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the Voltage Reference should be disabled.

#### 9.4 Effects of a Reset

A device reset disables the Voltage Reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

#### 9.5 <u>Connection Considerations</u>

The Voltage Reference Module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the Voltage Reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the Voltage Reference output for external connections to VREF. Figure 9-2 shows an example buffering technique.

## VREF Module Voltage Reference Output Impedance

### FIGURE 9-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

Note 1: R is dependent upon the Voltage Reference Configuration VRCON<3:0> and VRCON<5>.

#### TABLE 9-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR / BOD	Value On All Other Resets
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	—	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	—	—	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: - = Unimplemented, read as "0"

#### 10.2 Oscillator Configurations

#### 10.2.1 OSCILLATOR TYPES

The PIC16CE62X can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

## 10.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 10-1). The PIC16CE62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 10-2).

#### FIGURE 10-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 10-1 and Table 10-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

#### FIGURE 10-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



#### TABLE 10-1: CERAMIC RESONATORS, PIC16CE62X

**Ranges Tested:** OSC2 Mode Freq OSC1 XT 455 kHz 68 - 100 pF 68 - 100 pF 15 - 68 pF 15 - 68 pF 2.0 MHz 4.0 MHz 15 - 68 pF 15 - 68 pF HS 10 - 68 pF 10 - 68 pF 8.0 MHz 16.0 MHz 10 - 22 pF 10 - 22 pF

These values are for design guidance only. See notes at bottom of page.

#### TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16CE62X

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

These values are for design guidance only. See notes at bottom of page.

- 1. Recommended values of C1 and C2 are identical to the ranges tested table.
- 2. Higher capacitance increases the stability of oscillator, but also increases the start-up time.
- 3. Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

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#### 10.4.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired, then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (PWRT disabled), there will be no time-out at all. Figure 10-8, Figure 10-9 and Figure 10-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Then bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (see Figure 10-9). This is useful for testing purposes or to synchronize more than one  $\text{PIC}^{\textcircled{B}}$  device operating in parallel.

Table 10-5 shows the reset conditions for some special registers, while Table 10-6 shows the reset conditions for all the registers.

#### 10.4.6 POWER CONTROL (PCON)/STATUS REGISTER

The power control/status register, PCON (address 8Eh) has two bits.

Bit0 is  $\overline{\text{BOR}}$  (Brown-out).  $\overline{\text{BOR}}$  is unknown on power-on-reset. It must then be set by the user and checked on subsequent resets to see if  $\overline{\text{BOR}} = 0$ indicating that a brown-out has occurred. The  $\overline{\text{BOR}}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on-reset). It is a '0' on power-on-reset and unaffected otherwise. The user must write a '1' to this bit following a power-on-reset. On a subsequent reset, if POR is '0', it will indicate that a power-on-reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Beset	Wake-up from SLEEP	
	<b>PWRTE</b> = 0	PWRTE = 1	brown-out neset		
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms	—	72 ms	—	

#### TABLE 10-3: TIME-OUT IN VARIOUS SITUATIONS

POR	BOR	TO	PD	
0	Х	1	1	Power-on-reset
0	Х	0	Х	Illegal, TO is set on POR
0	Х	Х	0	Illegal, PD is set on POR

Brown-out Reset

WDT Reset

WDT Wake-up

MCLR reset during normal operation

MCLR reset during SLEEP

#### TABLE 10-4: STATUS/PCON BITS AND THEIR SIGNIFICANCE

Х

u

0

u

Ο

Legend: x = unknown, u = unchanged

0

1

1

1

1

Х

0

0

u

1

1

1

1

1

1





#### FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



#### FIGURE 10-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)



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CLRWDT	Clear Watchdog Timer						
Syntax:	[label] CLRWDT						
Operands:	None						
Operation:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \end{array}$						
Status Affected:	TO, PD						
Encoding:	00 0000 0110 0100						
	Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.						
Words:	1						
Cycles:	1						
Example	CLRWDT						
	Before Instruction WDT counter = ? After Instruction WDT counter = $0x00$ WDT prescaler= $0$ TO = $1$ PD = $1$						
COMF	Complement f						
Syntax:	[label] COME fd						

COM	oomplement							
Syntax:	[label] COMF f,d							
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$							
Operation:	$(\overline{f}) \rightarrow (dest)$							
Status Affected:	Z							
Encoding:	00 1001 dfff ffff							
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example	COMF REG1,0							
	Before Instruction REG1 = 0x13 After Instruction REG1 = 0x13 W = 0xEC							

DECF	Decrement f						
Syntax:	[label] DECF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$						
Operation:	(f) - 1 $\rightarrow$ (dest)						
Status Affected:	Z						
Encoding:	00 0011 d	lfff ffff					
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in regis- ter 'f'.						
Words:	1						
Cycles:	1						
Example	DECF CNT, 1						
	Before Instruction CNT = Z = After Instruction CNT = Z =	0x01 0 0x00 1					

DECFSZ	Decrement f, Skip if 0						
Syntax:	[label] DECFSZ f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$						
Operation:	(f) - 1 $\rightarrow$ (dest); skip if result = 0						
Status Affected:	None						
Encoding:	00 1011 dfff ffff						
Description:	decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.						
Words:	1						
Cycles:	1(2)						
Example	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • •						
	$\begin{array}{rcl} Before \ Instruction \\ PC &= & address \ {\rm HERE} \\ After \ Instruction \\ CNT &= & CNT - 1 \\ if \ CNT &= & 0, \\ PC &= & address \ {\rm CONTINUE} \\ if \ CNT \neq & 0, \\ PC &= & address \ {\rm HERE} + 1 \\ \end{array}$						

### 12.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB<sup>®</sup> IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER<sup>®</sup>/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE<sup>®</sup> II Universal Programmer
  - PICSTART<sup>®</sup> Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - SIMICE
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - SEEVAL®
  - KEELOQ<sup>®</sup>

#### 12.1 <u>MPLAB Integrated Development</u> <u>Environment Software</u>

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows<sup>®</sup>-based application which contains:

- · Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- · A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

#### 12.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PIC MCUs. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

#### 12.3 <u>MPLAB-C17 and MPLAB-C18</u> <u>C Compilers</u>

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

#### 12.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with precompiled libraries using directives from a linker script.

## **13.0 ELECTRICAL SPECIFICATIONS**

#### Absolute Maximum Ratings †

Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.0V
Voltage on RA4 with respect to Vss	8.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	8.5V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into Vod pin	250 mA
Input Clamp Current, Iк (Vi <0 or Vi> VDD)	±20 mA
Output Clamp Current, Iок (Vo <0 or Vo>VDD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA and PORTB	200 mA
Maximum Current sourced by PORTA and PORTB	200 mA
<b>Note 1:</b> Power dissipation is calculated as follows: PDIS = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VD	D-VOH) x IOH} + $\sum$ (VOI x IOL)

2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100<sup>3</sup>/<sub>4</sub> should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

**† NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



#### 13.6 EEPROM Timing





Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK		100		400	kHz	
Clock high time	Thigh	4000	—	600	_	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	_	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	_	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0		0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	_	ns	
STOP condition setup time	Tsu:sto	4000	—	600	_	ns	
Output valid from clock	ΤΑΑ	_	3500	_	900	ns	(Note 2)
Bus free time	TBUF	4700		1300	_	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VI∟ maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), $CB \le 100 \text{ pF}$
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	_	50	ns	(Note 3)
Write cycle time	Twr	—	10	_	10	ms	Byte or Page mode
Endurance	_	10M 1M	-	10M 1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

#### TABLE 13-7: AC CHARACTERISTICS

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

NOTES: