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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164cs-32f20f-bb-a

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
$\overline{\text{TRST}}$	36	I	Test-System Reset Input. A high level at this pin activates the XC164CS's debug system. For normal system operation, pin $\overline{\text{TRST}}$ should be held low.	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture In.,
		O	$\overline{\text{TxD1}}$	ASC0 Clock/Data Output (Async./Sync.),
		O	$\overline{\text{BRKOUT}}$	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	$\overline{\text{T2IN}}$	GPT1 Timer T2 Count/Gate/Reload/Capture In.,
		I	$\overline{\text{BRKIN}}$	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	$\overline{\text{EX2IN}}$	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 4 XC164CS Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$

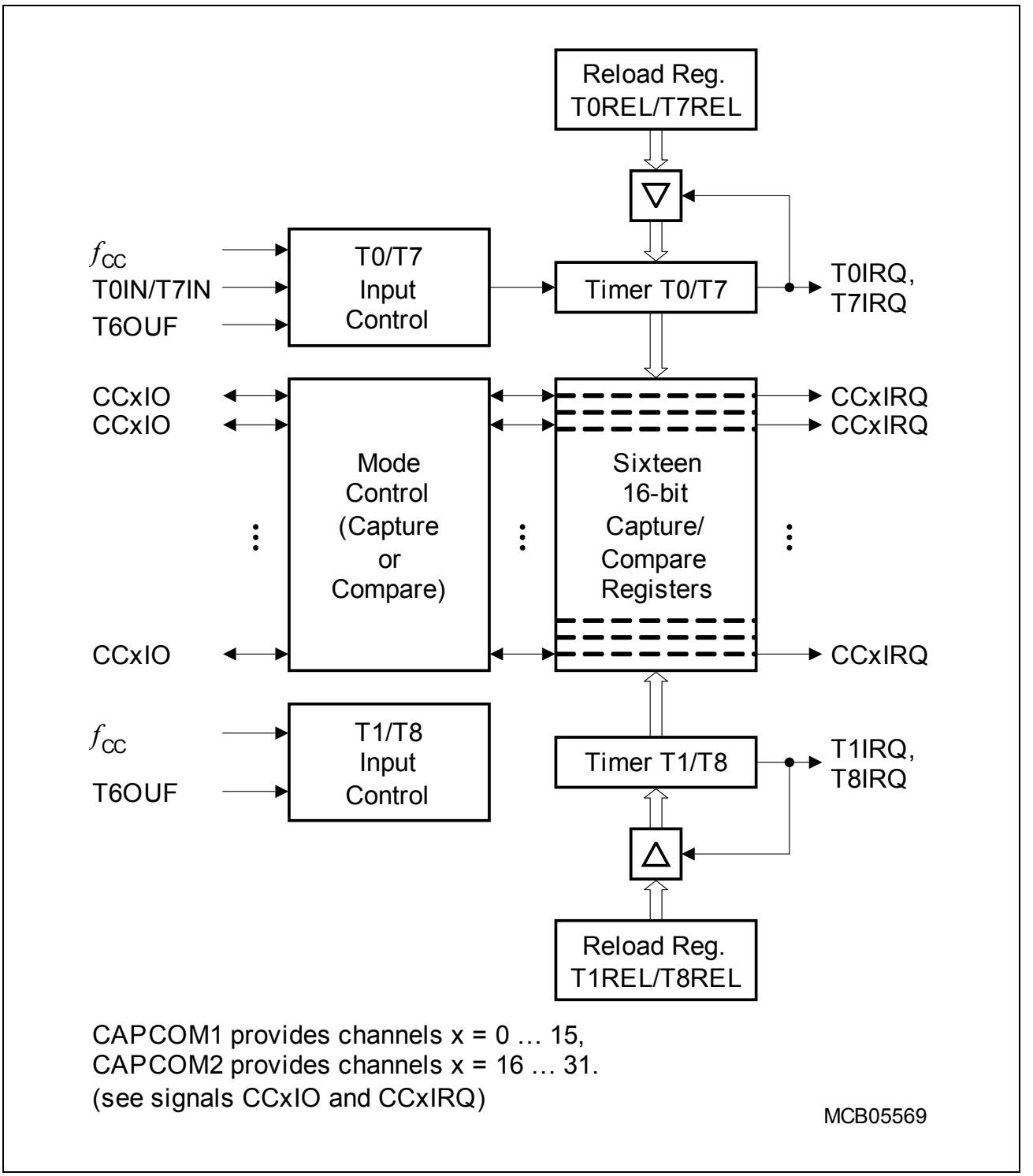
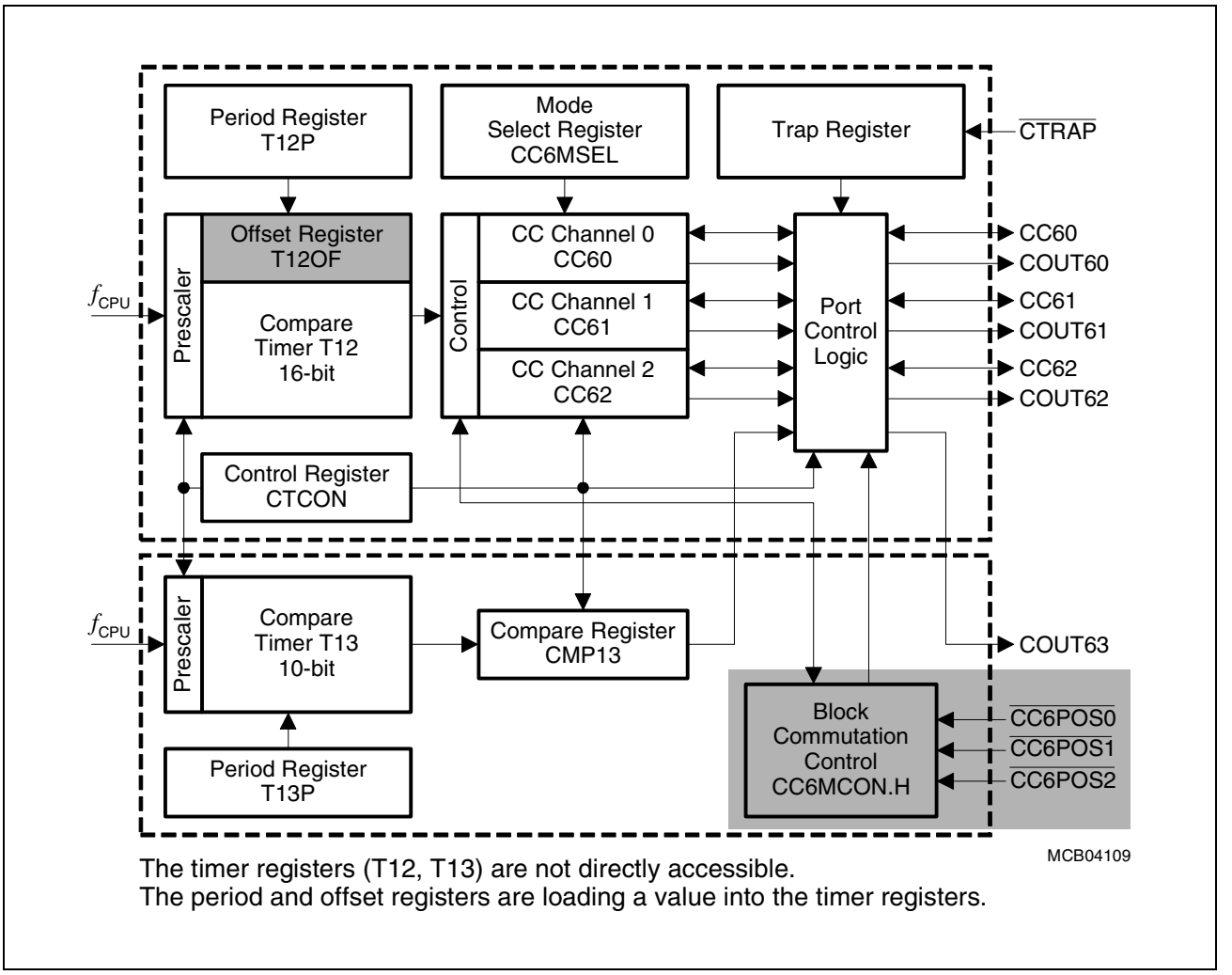


Figure 5 CAPCOM1/2 Unit Block Diagram

3.7 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.



The timer registers (T12, T13) are not directly accessible.
The period and offset registers are loading a value into the timer registers.

Figure 6 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

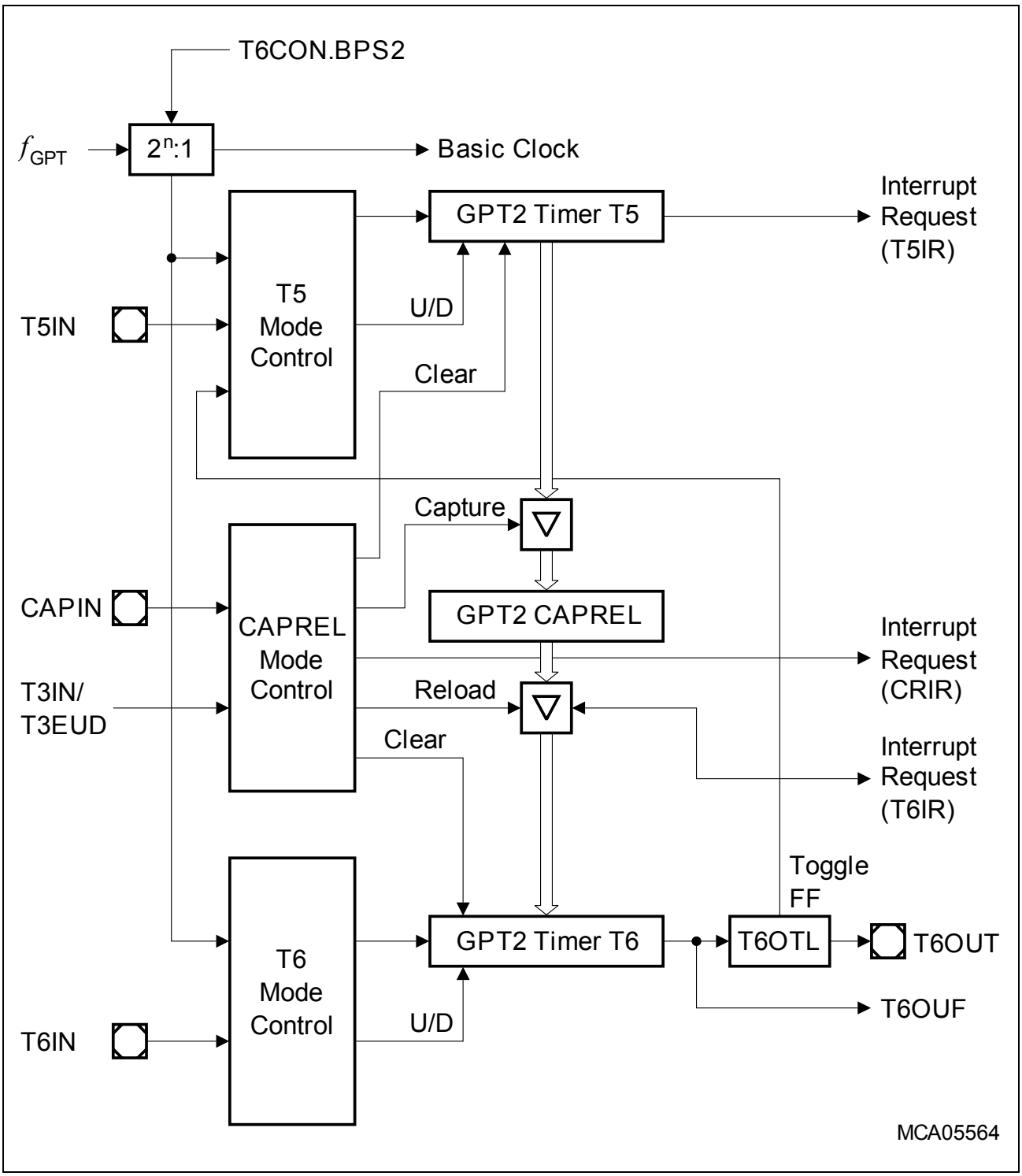


Figure 8 Block Diagram of GPT2

The RTC module can be used for different purposes:

- System clock to determine the current time and date,
  optionally during idle mode, sleep mode, and power down mode
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode
- 48-bit timer for long term measurements (maximum timespan is > 100 years)
- Alarm interrupt for wake-up on a defined time

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
  - Assignment to one of the two CAN nodes
  - Configuration as transmit object or receive object
  - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
  - Handling of frames with 11-bit or 29-bit identifiers
  - Individual programmable acceptance mask register for filtering for each object
  - Monitoring via a frame counter
  - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

Note: When a CAN node has the interface lines assigned to Port 4, the segment address output on Port 4 must be limited. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

3.15 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC164CS with high flexibility. The master clock f_{MC} is the reference clock signal, and is used for TwinCAN and is output to the external system. The CPU clock f_{CPU} and the system clock f_{SYS} are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also **Section 4.4.1**.

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock/OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

The oscillator watchdog can be disabled by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of an external reset ($\overline{EA}$ = '0') the oscillator watchdog may be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration.

3.16 Parallel Ports

The XC164CS provides up to 79 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs (except for pin $\overline{RSTOUT}$).

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

3.18 Instruction Set Summary

Table 8 lists the instructions of the XC164CS in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164CS. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)2)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)3)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	V_{DDP} - V_{DDI} 4)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 5)6)
		-2	5	mA	Per analog input pin 5)6)
Overload current coupling factor for analog inputs 7)	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins 7)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	6)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 8)
Ambient temperature	T_A	0	70	°C	SAB-XC164…
		-40	85	°C	SAF-XC164…
		-40	125	°C	SAK-XC164…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 12**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

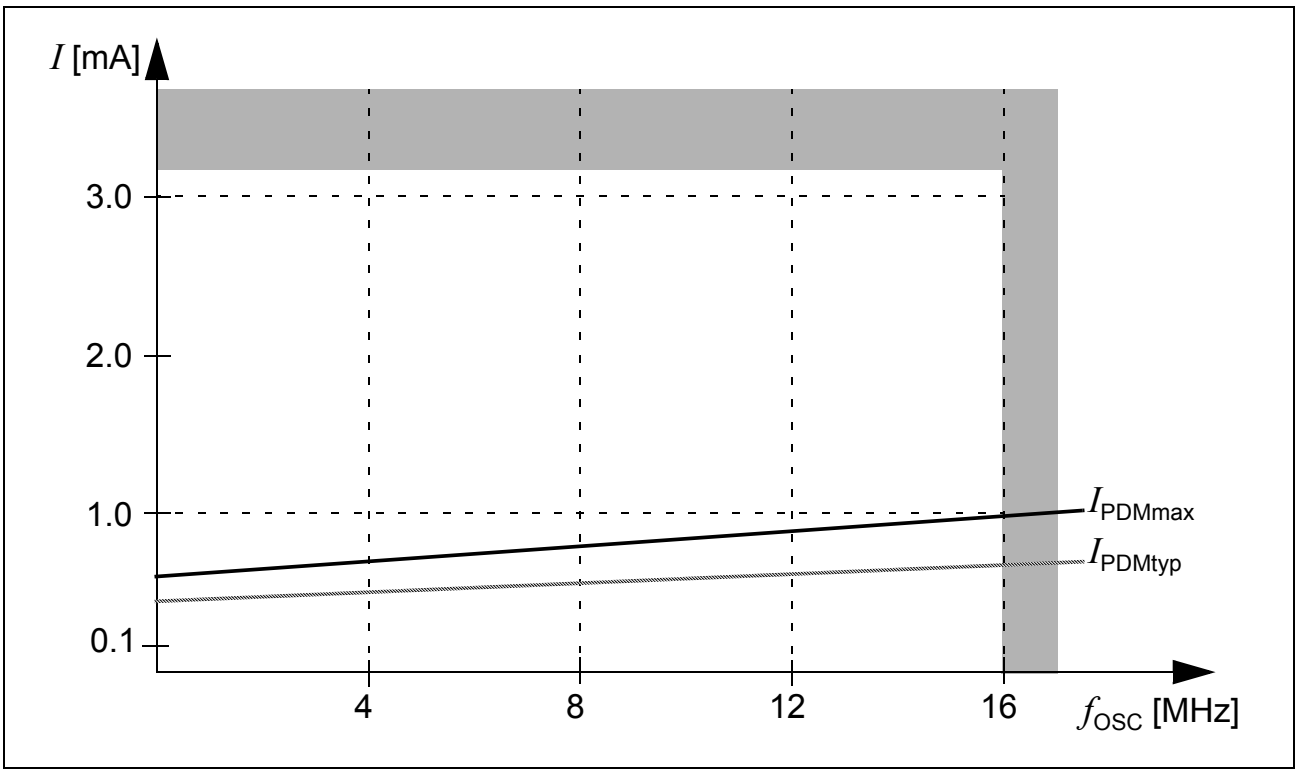


Figure 12 **Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency**

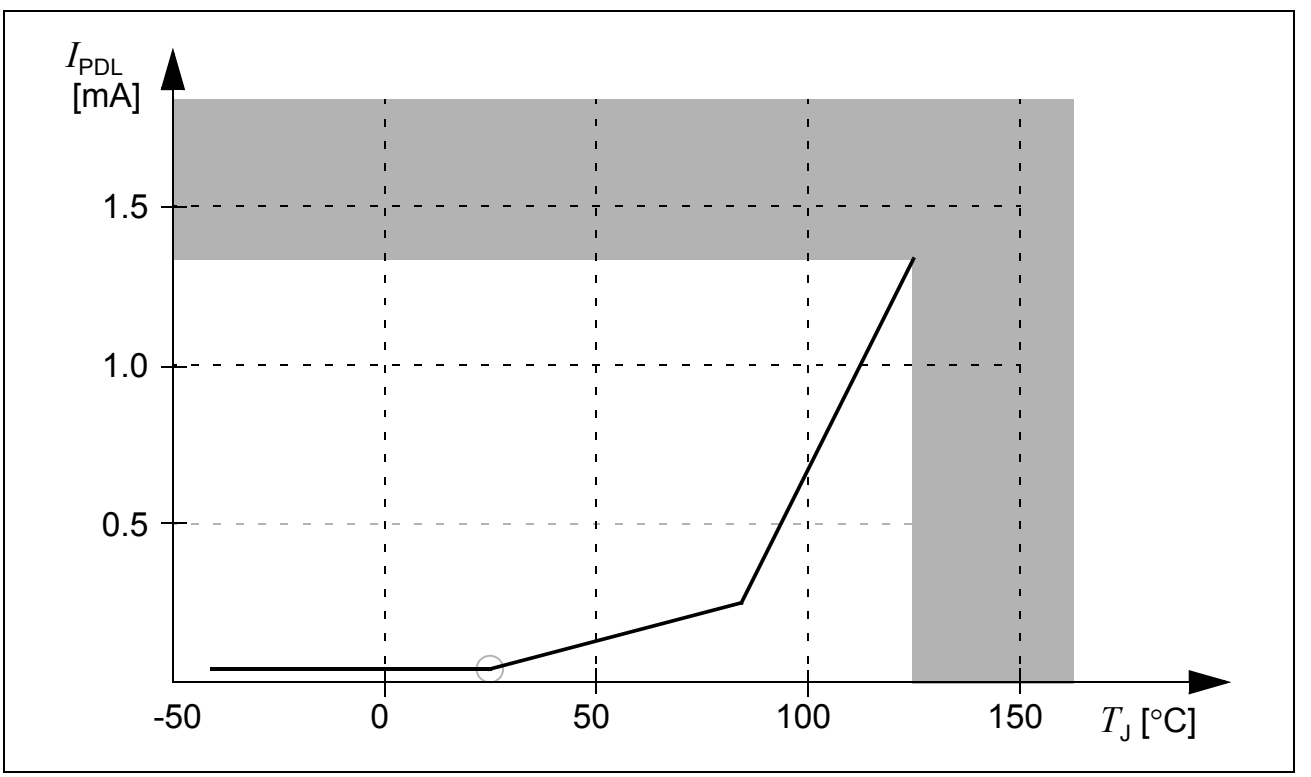


Figure 13 **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	kΩ	6)

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU}.

Bypass Operation

When bypass operation is configured (PLLCTRL = $0x_B$) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$f_{MC} = f_{OSC} / ((PLLIDIV+1) \times (PLLODIV+1))$.

If both divider factors are selected as ‘1’ (PLLIDIV = PLLODIV = ‘0’) the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC}.

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$f_{MC} = f_{OSC} / ((3 + 1) \times (14 + 1)) = f_{OSC} / 60$.

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor, and the output divider (**F** = PLLMUL+1 / (PLLIDIV+1 $\times$ PLLODIV+1)). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 16**).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train

Table 16 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

4.4.2 On-chip Flash Operation

The XC164CS's Flash module delivers data within a fixed access time (see **Table 17**).

Accesses to the Flash module are controlled by the PMI and take 1 + WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. Therefore, the required Flash waitstates depend on the available speed grade as well as on the actual system frequency.

Note: The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15%.

Table 17 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time (Standard)	t_{ACC}	CC	–	–	70[1]	ns
Flash module access time (Grade A)	t_{ACC}	CC	–	–	50[1]	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[2]	5	ms
Erase time per sector	t_{ER}	CC	–	200[2]	500	ms

1) The actual access time is also influenced by the system frequency, so the frequency ranges are not fully linear. See **Table 18**.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), Standard devices must be operated with 2 waitstates: ((2 + 1) × 25 ns) ≥ 70 ns.
Grade A devices can be operated with 1 waitstate: ((1 + 1) × 25 ns) ≥ 50 ns.

Table 18 indicates the interrelation of waitstates, system frequency, and speed grade.

Table 18 Flash Access Waitstates

Required Waitstates	Frequency Range for Standard Flash Speed	Frequency Range for Flash Speed Grade A
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 16$ MHz	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 28$ MHz	$f_{CPU} \leq 40$ MHz
2 WS (WSFLASH = 10_B)	$f_{CPU} \leq 40$ MHz	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for xxx-32F20F devices).

4.4.3 External Clock Drive XTAL1

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1)]	ns
High time[2)]	t_1	SR	6	–	ns
Low time[2)]	t_2	SR	6	–	ns
Rise time[2)]	t_3	SR	–	8	ns
Fall time[2)]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

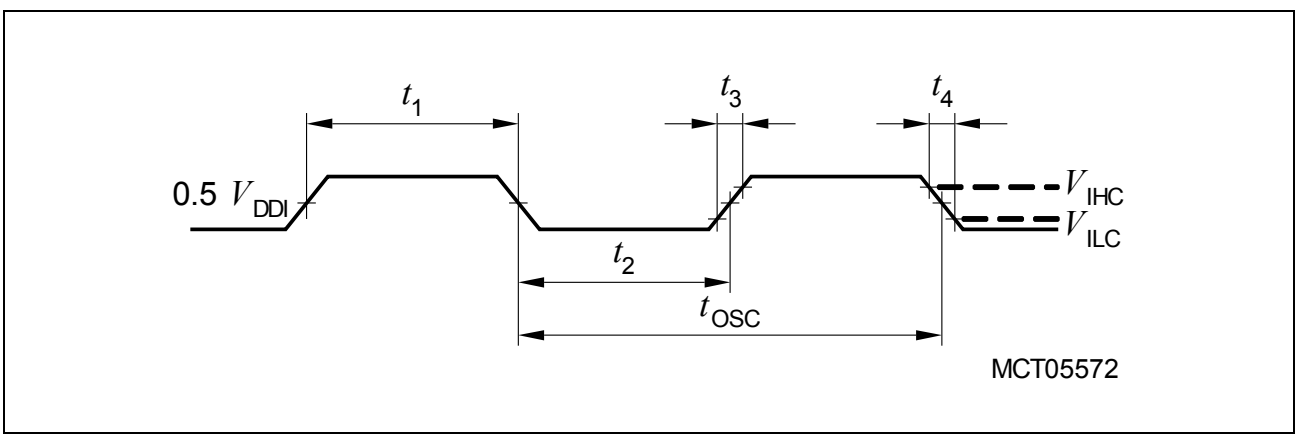


Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

Package Outlines

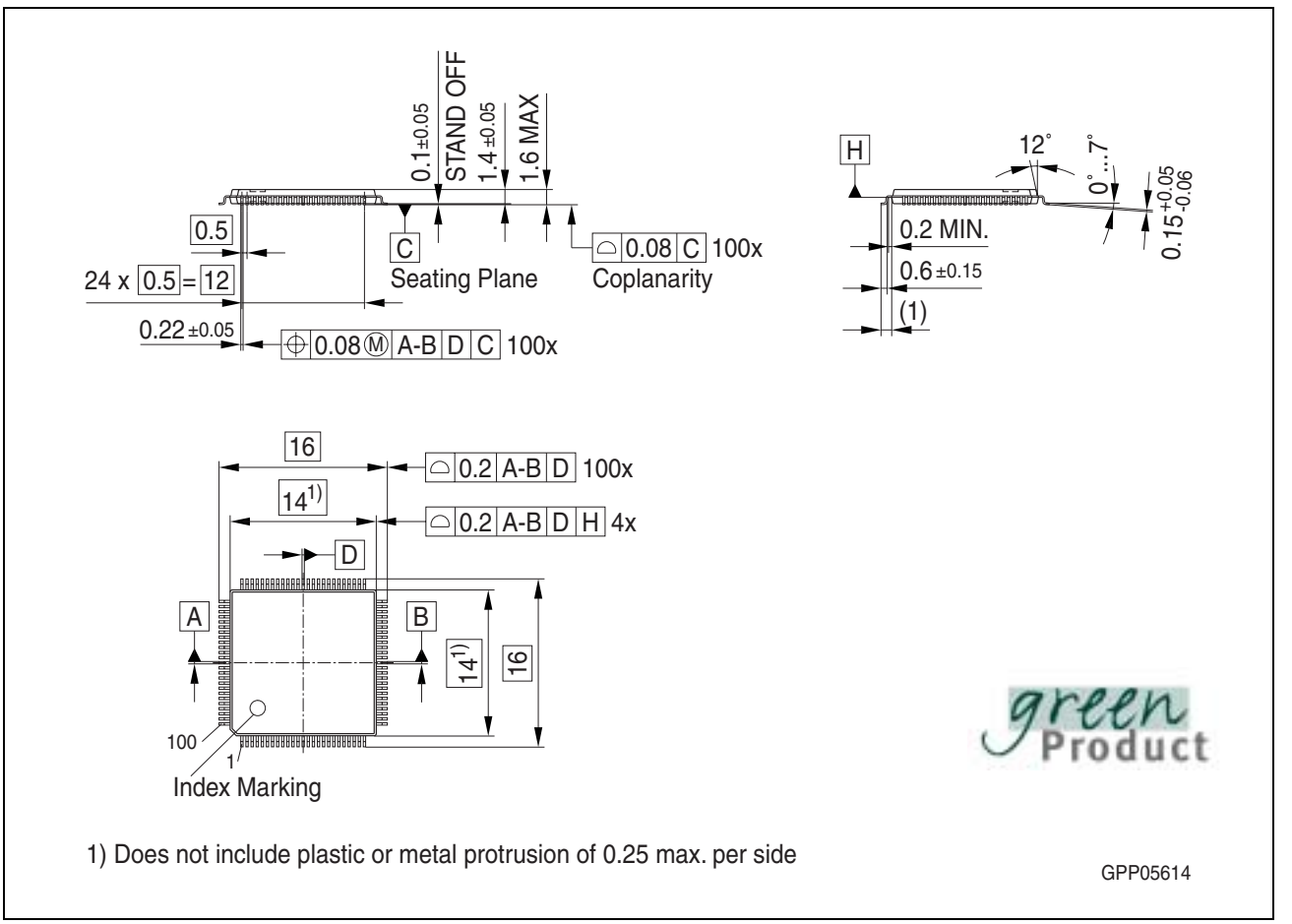


Figure 23 PG-TQFP-100-5 (Plastic Green Thin Quad Flat Package)

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