Infineon Technologies - XC164CS32F40FBBAFXQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cs32f40fbbafxqma1

XC164CS-32F/32R

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

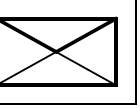
Never stop thinking

XC164CS
Revision History: V1.1, 2006-08

Previous Version(s):
V1.0, 2005-06 (XC164-32F)

Page	Subjects (major changes since last revision)
6	New derivatives added.
51	Footnote at XTAL1 input pin.
55	Footnote on leakage of P3.15 added.
76	Green Package added.
75	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
mcdocu.comments@infineon.com



- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Four Programmable Chip-Select Signals
- Up to 79 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 100-Pin Green TQFP Package, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164CS please refer to your responsible sales representative or your local distributor.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the XC164CS group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164CS** throughout this document.

RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Table 3 XC164CS Memory Map[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Flash register space	$FF'F000_H$	$FF'FFFF_H$	4 Kbytes	[3)]
Reserved (Acc. trap)	$FE'0000_H$	$FF'EFFF_H$	60 Kbytes	–
Reserved for EPSRAM	$F8'1800_H$	$FD'FFFF_H$	378 Kbytes	–
Emul. Program SRAM[4)]	$F8'0000_H$	$F8'17FF_H$	6 Kbytes	2nd way to PSRAM
Reserved for PSRAM	$E0'1800_H$	$F7'FFFF_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	$E0'0000_H$	$E0'17FF_H$	6 Kbytes	Maximum
Reserved for program memory	$C4'0000_H$	$DF'FFFF_H$	< 2 Mbytes	Minus Flash
Program Flash/ROM	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	–
Reserved	$BF'0000_H$	$BF'FFFF_H$	64 Kbytes	–
External memory area	$40'0000_H$	$BE'FFFF_H$	< 8 Mbytes	Minus reserved segment
External IO area[5)]	$20'0800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus TwinCAN
TwinCAN registers	$20'0000_H$	$20'07FF_H$	2 Kbytes	–
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
Data RAMs and SFRs	$00'8000_H$	$00'FFFF_H$	32 Kbytes	Partly used
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) Accesses to the shaded areas generate external bus accesses.
2) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.
3) Not defined register locations return a trap code.
4) The Emulation PSRAM (EPSRAM) realizes a 2nd access path to the PSRAM with a different timing.

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM1/2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC164CS to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

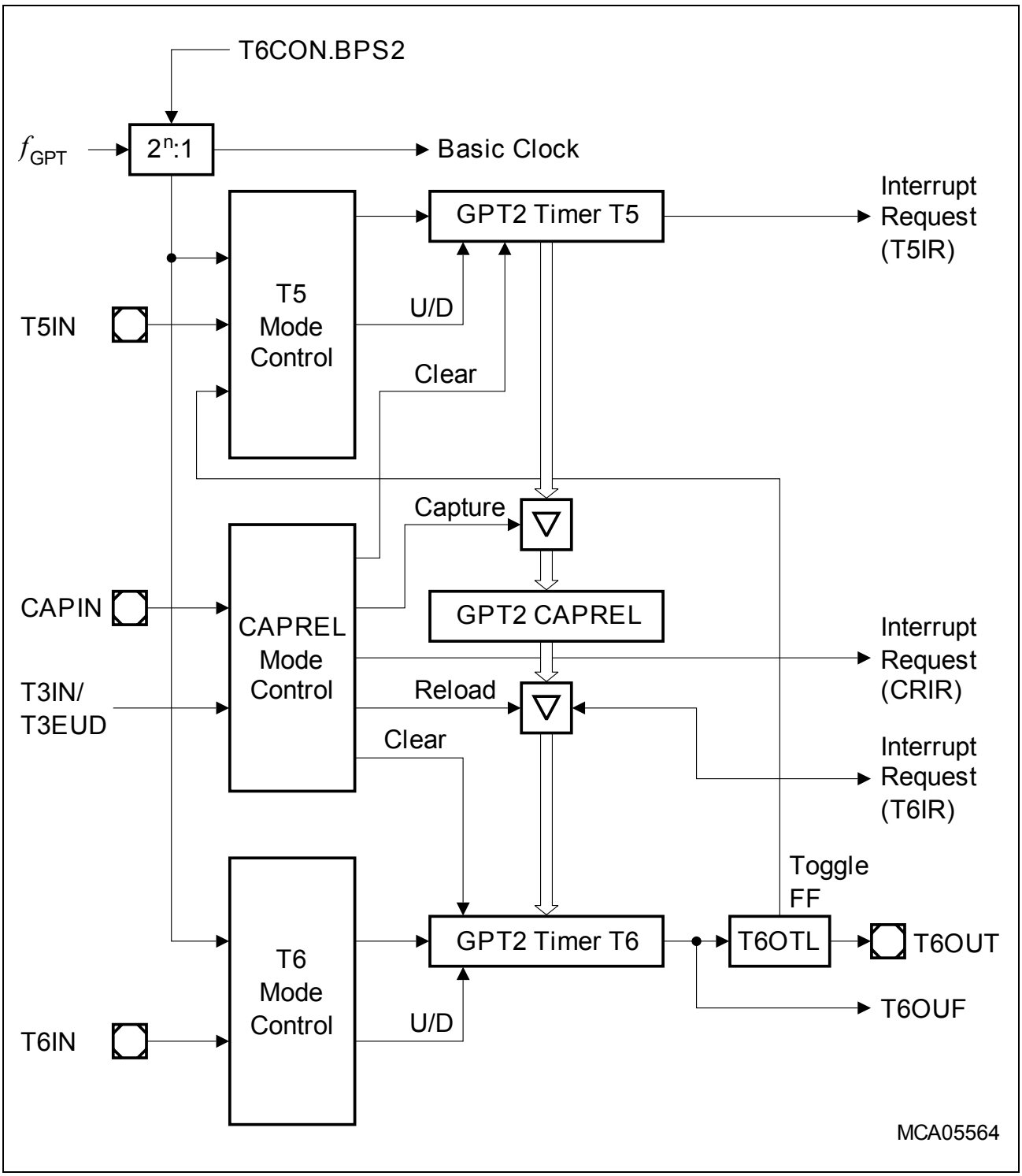


Figure 8 Block Diagram of GPT2

3.10 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 14 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC164CS supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.

3.12 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

3.15 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC164CS with high flexibility. The master clock f_{MC} is the reference clock signal, and is used for TwinCAN and is output to the external system. The CPU clock f_{CPU} and the system clock f_{SYS} are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also **Section 4.4.1**.

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock/OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

The oscillator watchdog can be disabled by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of an external reset ($\overline{EA}$ = '0') the oscillator watchdog may be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration.

3.16 Parallel Ports

The XC164CS provides up to 79 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs (except for pin $\overline{RSTOUT}$).

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

3.18 Instruction Set Summary

Table 8 lists the instructions of the XC164CS in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
   Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.
6) Not subject to production test - verified by design/characterization.
7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
   The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.
8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164CS and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC164CS will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the XC164CS.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP}$ - 0.1	V	–
Input low voltage XTAL1[2)]	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	[3)]
Input high voltage TTL (all except XTAL1)	V_{IH}	SR	$0.2 \times V_{DDP}$ + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1[2)]	V_{IHC}	SR	$0.7 \times V_{DDI}$	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP}$ - 0.2	V_{DDP} + 0.5	V	[3)]
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	–	V	V_{DDP} in [V], Series resistance = 0 Ω[3)]
Output low voltage	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[4)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[4)5)]
Output high voltage[6)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[4)]
			V_{DDP} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[4)5)]
Input leakage current (Port 5)[7)]	I_{OZ1}	CC	–	±300	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 125$ °C
				±200	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 85$ °C[14)]
Input leakage current (all other[8)])[7)]	I_{OZ2}	CC	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[9)]	I_{CPUH}[10)]		–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[11)]		-100	–	µA	$V_{IN} = V_{ILmax}$
Configuration pull-down current[12)]	I_{CPDL}[10)]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[11)]		120	–	µA	$V_{IN} = V_{IHmin}$

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Level inactive hold current[13]	I_{LHI}[10]		–	-10	µA	V_{OUT} = 0.5 × V_{DDP}
Level active hold current[13]	I_{LHA}[11]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[14] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) This parameter is tested for P3, P4, P9.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

9) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0

10) The maximum current may be drawn while the respective signal line remains inactive.

11) The minimum current must be drawn to drive the respective signal line active.

12) This specification is valid during Reset for configuration on ALE.

13) This specification is valid during Reset for pins P4.3-0, which can act as $\overline{CS}$ outputs, and for P3.12.

14) Not subject to production test - verified by design/characterization.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 12**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

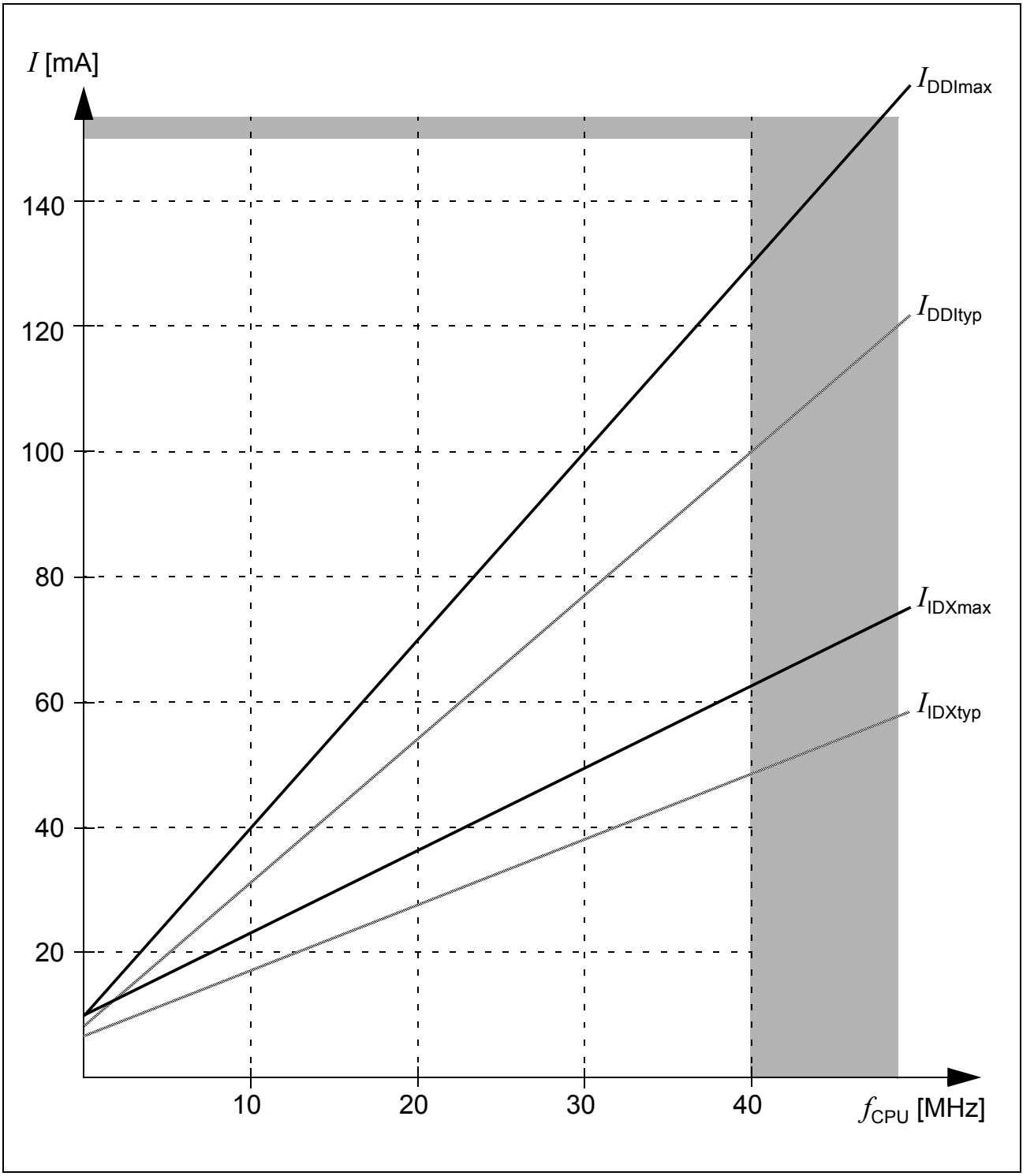


Figure 11 Supply/Idle Current as a Function of Operating Frequency

3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 x t_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

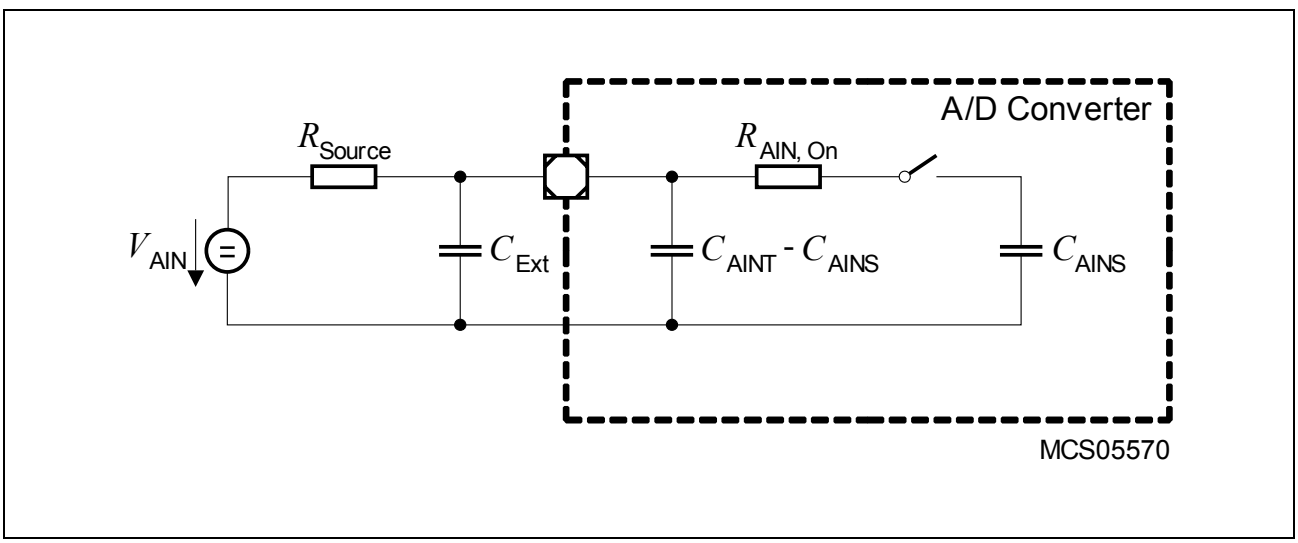


Figure 14 Equivalent Circuitry for Analog Inputs

4.4.2 On-chip Flash Operation

The XC164CS's Flash module delivers data within a fixed access time (see **Table 17**).

Accesses to the Flash module are controlled by the PMI and take 1 + WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. Therefore, the required Flash waitstates depend on the available speed grade as well as on the actual system frequency.

Note: The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15%.

Table 17 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time (Standard)	t_{ACC}	CC	–	–	70[1]	ns
Flash module access time (Grade A)	t_{ACC}	CC	–	–	50[1]	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[2]	5	ms
Erase time per sector	t_{ER}	CC	–	200[2]	500	ms

1) The actual access time is also influenced by the system frequency, so the frequency ranges are not fully linear. See **Table 18**.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), Standard devices must be operated with 2 waitstates: ((2 + 1) × 25 ns) ≥ 70 ns.
Grade A devices can be operated with 1 waitstate: ((1 + 1) × 25 ns) ≥ 50 ns.

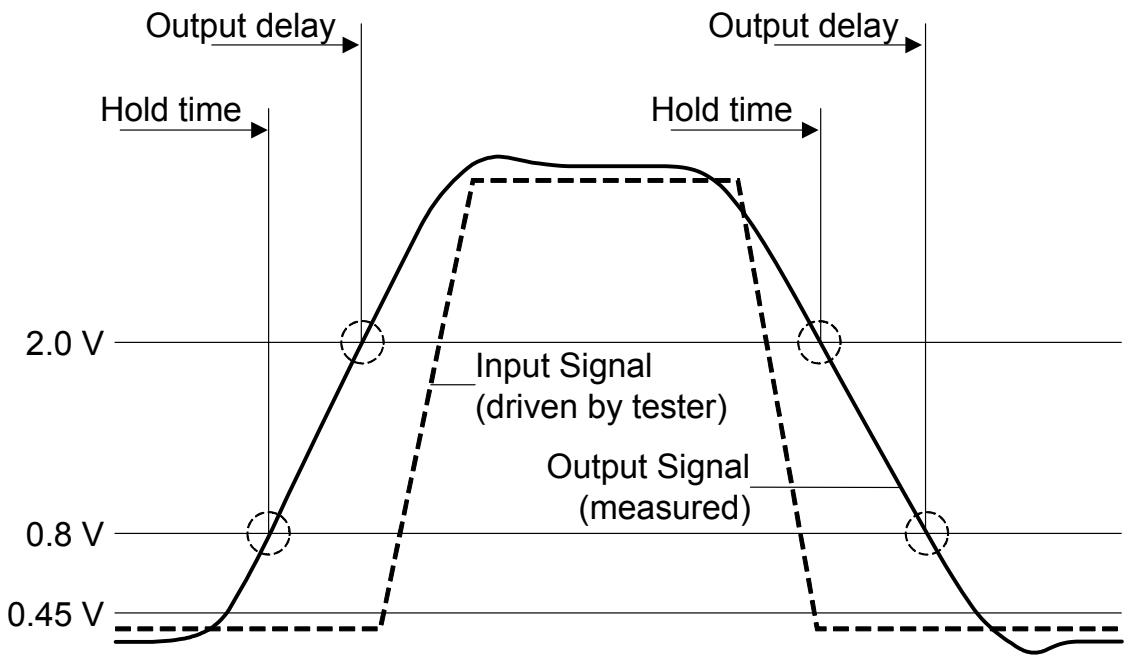
Table 18 indicates the interrelation of waitstates, system frequency, and speed grade.

Table 18 Flash Access Waitstates

Required Waitstates	Frequency Range for Standard Flash Speed	Frequency Range for Flash Speed Grade A
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 16$ MHz	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 28$ MHz	$f_{CPU} \leq 40$ MHz
2 WS (WSFLASH = 10_B)	$f_{CPU} \leq 40$ MHz	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for xxx-32F20F devices).

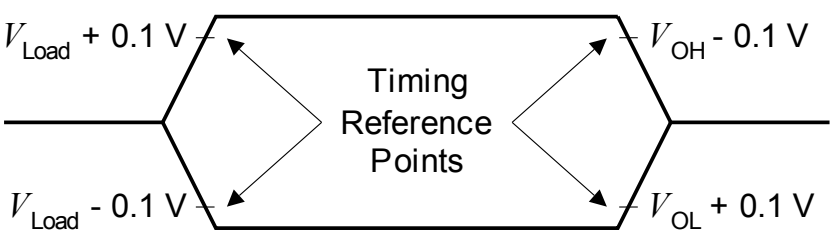
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 18 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 19 Float Waveforms

Table 22 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Output valid delay for: RD, WR(L/H)	tc_{10}	CC	1	15	ns
Output valid delay for: BHE, ALE	tc_{11}	CC	-1	8	ns
Output valid delay for: A23 … A16, A15 … A0 (on PORT1)	tc_{12}	CC	3	18	ns
Output valid delay for: A15 … A0 (on PORT0)	tc_{13}	CC	3	18	ns
Output valid delay for: CS	tc_{14}	CC	3	16	ns
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15}	CC	3	19	ns
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16}	CC	2	16	ns
Output hold time for: RD, WR(L/H)	tc_{20}	CC	-3	4	ns
Output hold time for: BHE, ALE	tc_{21}	CC	0	11	ns
Output hold time for: A23 … A16, A15 … A0 (on PORT0)	tc_{23}	CC	1	13	ns
Output hold time for: CS	tc_{24}	CC	-2	4	ns
Output hold time for: D15 … D0 (write data)	tc_{25}	CC	1	13	ns
Input setup time for: D15 … D0 (read data)	tc_{30}	SR	29	–	ns
Input hold time D15 … D0 (read data)[1)]	tc_{31}	SR	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD.

Note: The shaded parameters have been verified by characterization. They are not subject to production test.

5.2 Flash Memory Parameters

The data retention time of the XC164CS's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 24 Flash Parameters (XC164CS, 256 Kbytes)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Data retention time	t_{RET}	15	–	years	Max. 10^3 erase/program cycles
Flash Erase Endurance	N_{ER}	20×10^3	–	–	Max. data retention time 5 years