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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cs32f40fbbafxuma1

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XC164CS-32F/32R

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

Table of Contents

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
$\overline{\text{TRST}}$	36	I	Test-System Reset Input. A high level at this pin activates the XC164CS's debug system. For normal system operation, pin $\overline{\text{TRST}}$ should be held low.	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture In.,
		O	$\overline{\text{TxD1}}$	ASC0 Clock/Data Output (Async./Sync.),
		O	$\overline{\text{BRKOUT}}$	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	$\overline{\text{T2IN}}$	GPT1 Timer T2 Count/Gate/Reload/Capture In.,
		I	$\overline{\text{BRKIN}}$	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	$\overline{\text{EX2IN}}$	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]
P4.0	53	O	A16 Least Significant Segment Address Line,
		O	CS3 Chip Select 3 Output
P4.1	54	O	A17 Segment Address Line,
		O	CS2 Chip Select 2 Output
P4.2	55	O	A18 Segment Address Line,
		O	CS1 Chip Select 1 Output
P4.3	56	O	A19 Segment Address Line,
		O	CS0 Chip Select 0 Output
P4.4	57	O	A20 Segment Address Line,
		I	CAN1_RxD CAN Node B Receive Data Input,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin B)
P4.5	58	O	A21 Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin B)
P4.6	59	O	A22 Segment Address Line,
		O	CAN0_TxD CAN Node A Transmit Data Output,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin A)
P4.7	60	O	A23 Most Significant Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		O	CAN1_TxD CAN Node B Transmit Data Output,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	63	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	64	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.4	65	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	66	I	$\overline{EA}$	External Access Enable pin. **A low level** at this pin during and after Reset forces the XC164CS to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the XC164CS to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	2	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{DDI}	35, 97	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Condition Parameters**.
V_{DDP}	9, 17, 38, 61, 87	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Condition Parameters**.
V_{SSI}	34, 98	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	8, 16, 37, 62, 88	–	

1) The CAN interface lines are assigned to ports P4 and P9 under software control.

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CS is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CS supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CS has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164CS interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC164CS Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

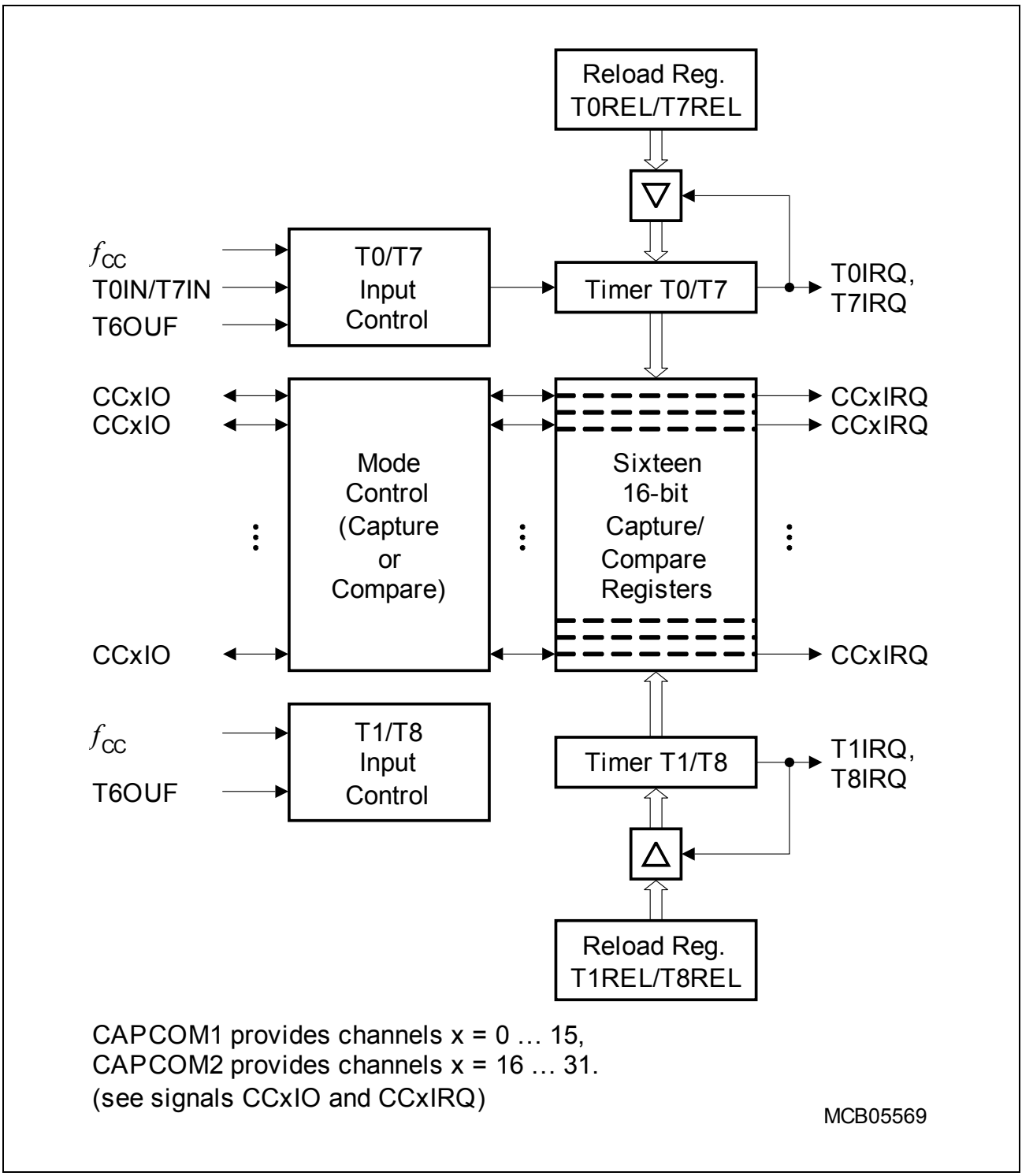

Figure 5 CAPCOM1/2 Unit Block Diagram

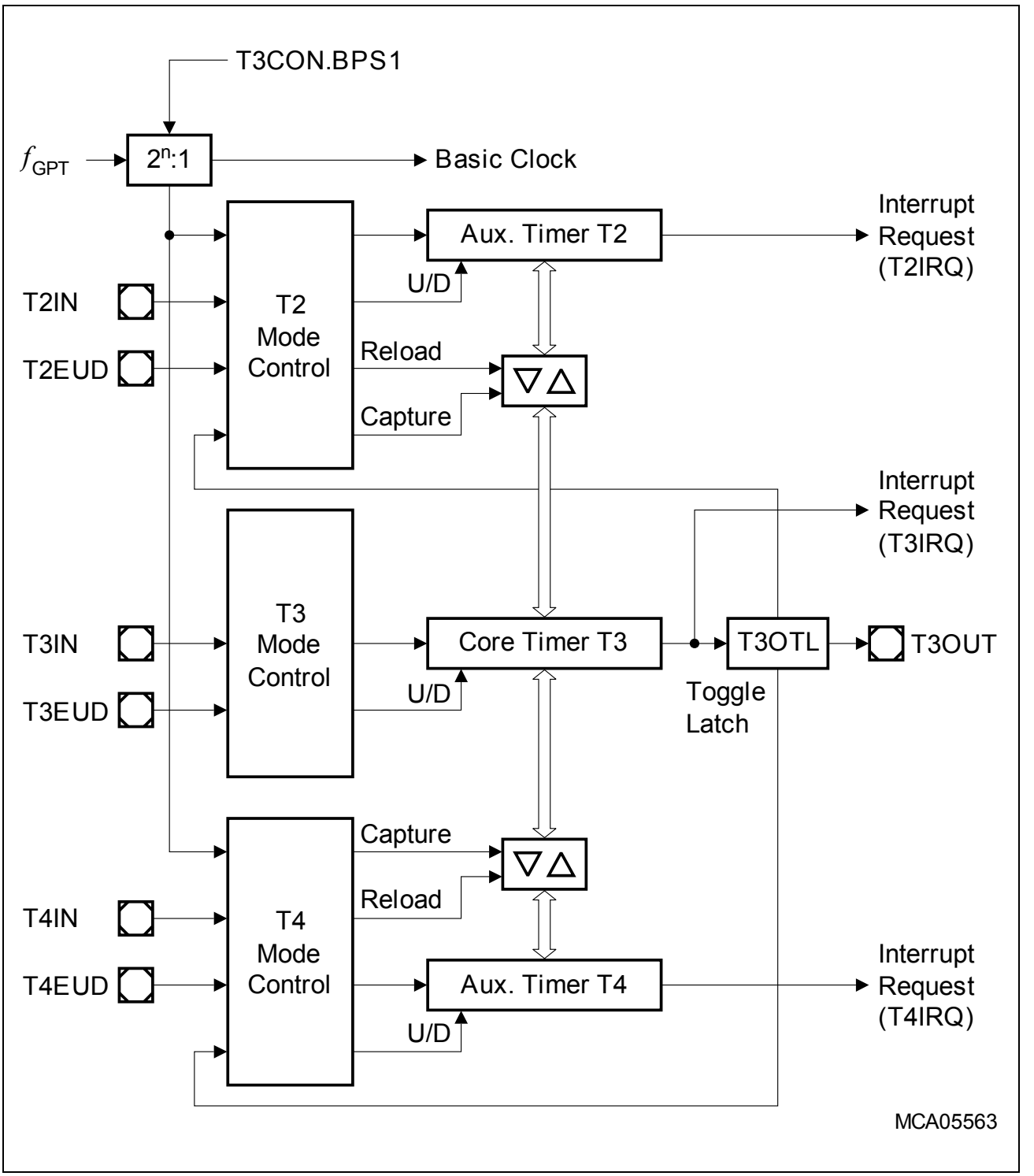

Figure 7 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The

3.15 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC164CS with high flexibility. The master clock f_{MC} is the reference clock signal, and is used for TwinCAN and is output to the external system. The CPU clock f_{CPU} and the system clock f_{SYS} are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also **Section 4.4.1**.

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock/OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

The oscillator watchdog can be disabled by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of an external reset ($\overline{EA}$ = '0') the oscillator watchdog may be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration.

3.16 Parallel Ports

The XC164CS provides up to 79 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs (except for pin $\overline{RSTOUT}$).

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP}$ - 0.1	V	–
Input low voltage XTAL1[2)]	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	[3)]
Input high voltage TTL (all except XTAL1)	V_{IH}	SR	$0.2 \times V_{DDP}$ + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1[2)]	V_{IHC}	SR	$0.7 \times V_{DDI}$	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP}$ - 0.2	V_{DDP} + 0.5	V	[3)]
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	–	V	V_{DDP} in [V], Series resistance = 0 Ω[3)]
Output low voltage	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[4)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[4)5)]
Output high voltage[6)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[4)]
			V_{DDP} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[4)5)]
Input leakage current (Port 5)[7)]	I_{OZ1}	CC	–	±300	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 125$ °C
				±200	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 85$ °C[14)]
Input leakage current (all other[8)])[7)]	I_{OZ2}	CC	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[9)]	I_{CPUH}[10)]		–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[11)]		-100	–	µA	$V_{IN} = V_{ILmax}$
Configuration pull-down current[12)]	I_{CPDL}[10)]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[11)]		120	–	µA	$V_{IN} = V_{IHmin}$

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 12**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

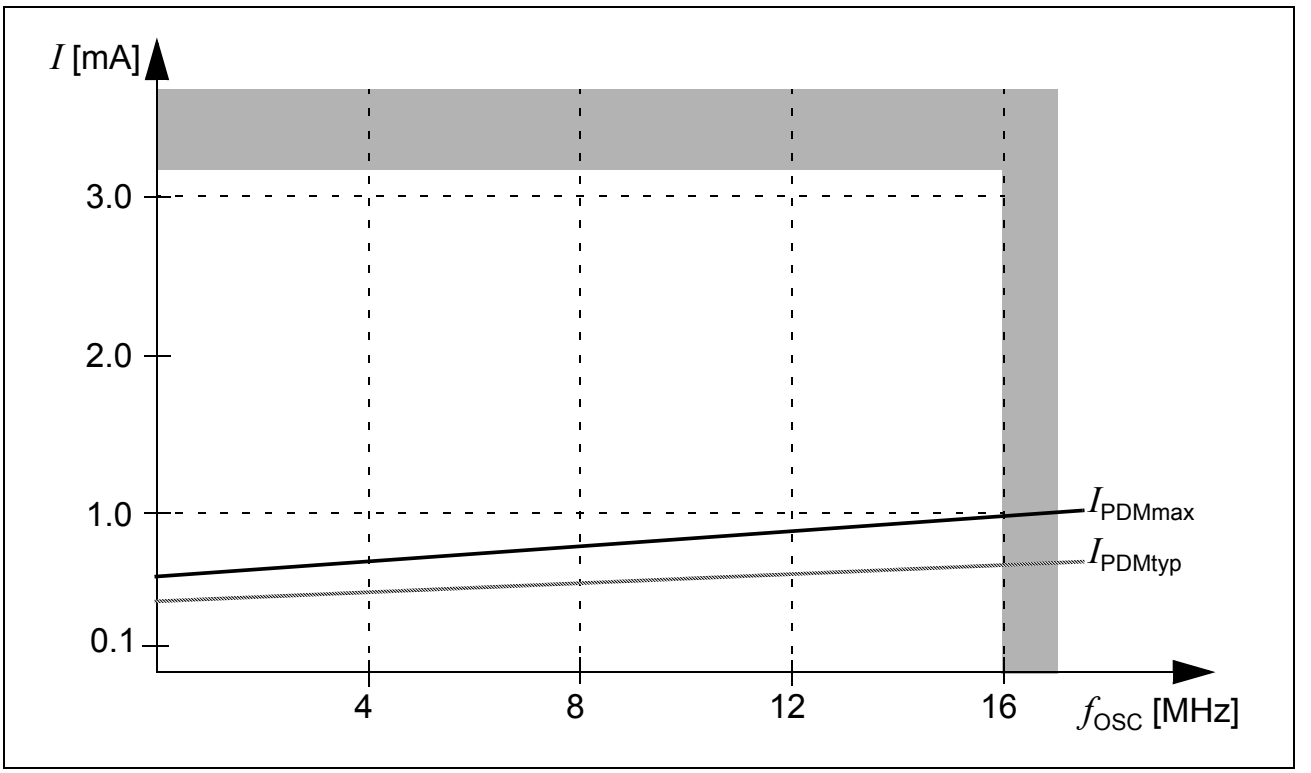

Figure 12 **Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency**

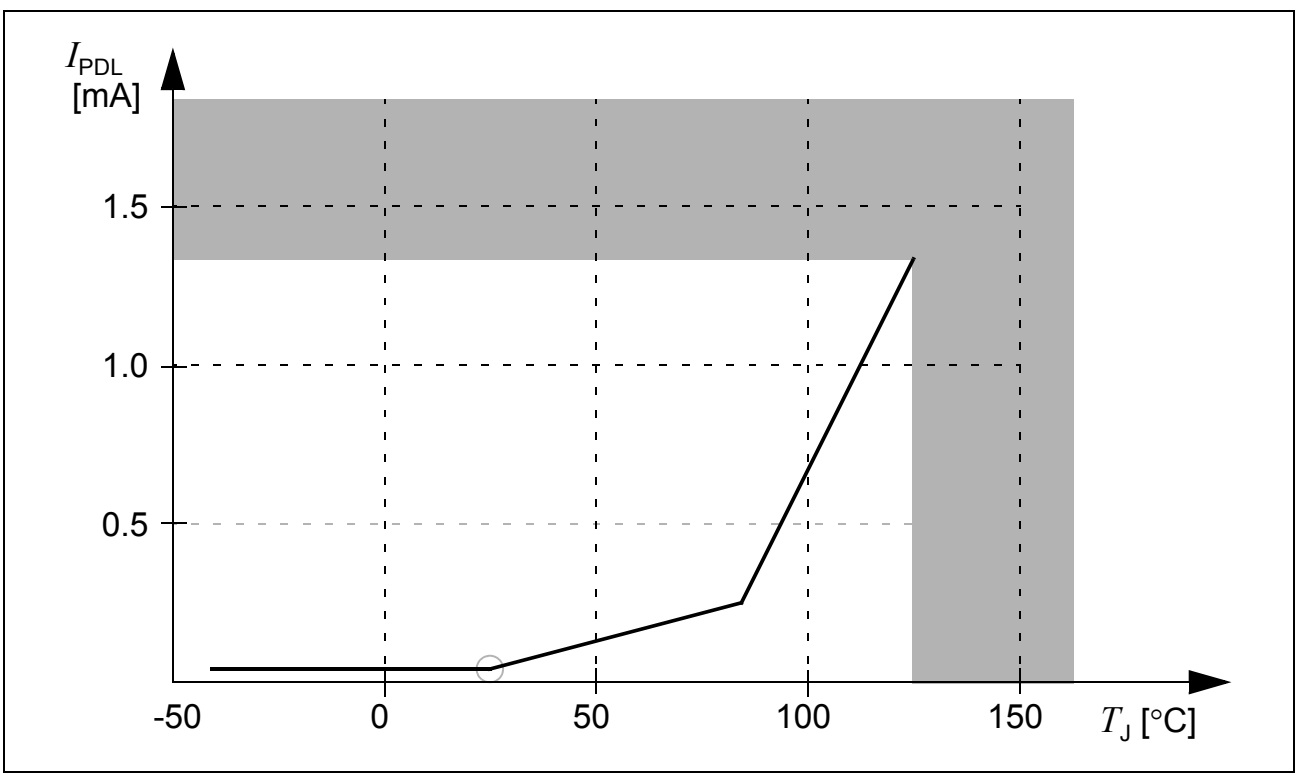

Figure 13 **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 x t_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

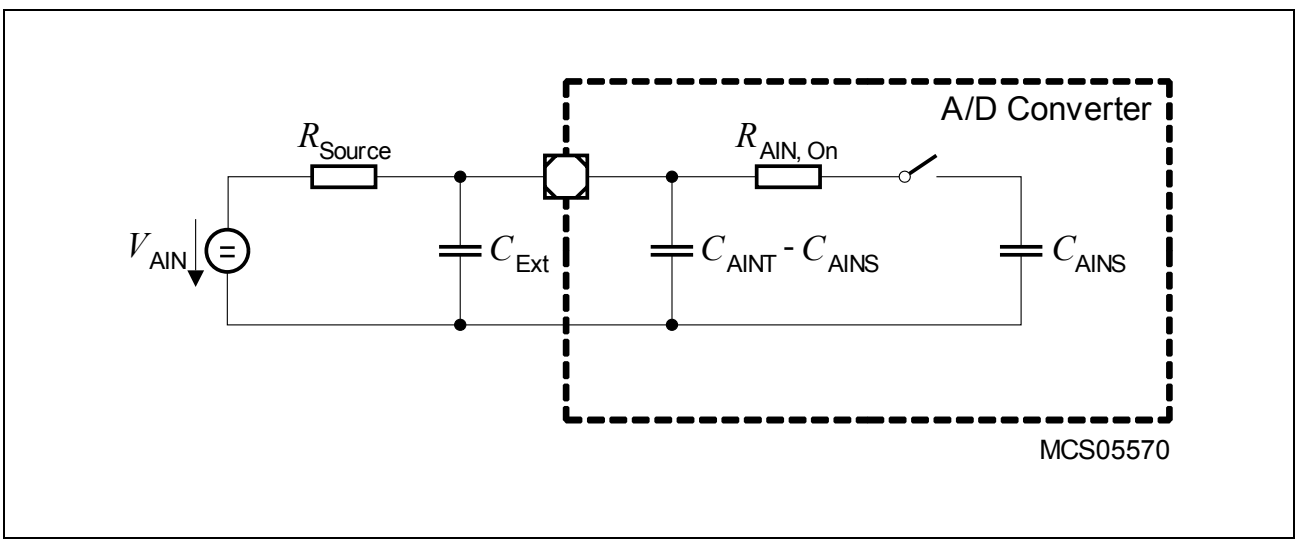

Figure 14 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the XC164CS's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using **Table 15**.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 15 A/D Converter Computation Table[1)]

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample Time t_S
00	f_{SYS} / 4	00	$t_{BC} \times 8$
01	f_{SYS} / 2	01	$t_{BC} \times 16$
10	f_{SYS} / 16	10	$t_{BC} \times 32$
11	f_{SYS} / 8	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), ADCTC = '01', ADSTC = '00'
Basic clock f_{BC} = f_{SYS} / 2 = 20 MHz, i.e. t_{BC} = 50 ns
Sample time t_S = $t_{BC} \times 8$ = 400 ns
Conversion 10-bit:
With post-calibr. t_{C10P} = $52 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2600 + 400 + 150) ns = 3.15 µs
Post-calibr. off t_{C10} = $40 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2000 + 400 + 150) ns = 2.55 µs
Conversion 8-bit:
With post-calibr. t_{C8P} = $44 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2200 + 400 + 150) ns = 2.75 µs
Post-calibr. off t_{C8} = $32 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (1600 + 400 + 150) ns = 2.15 µs

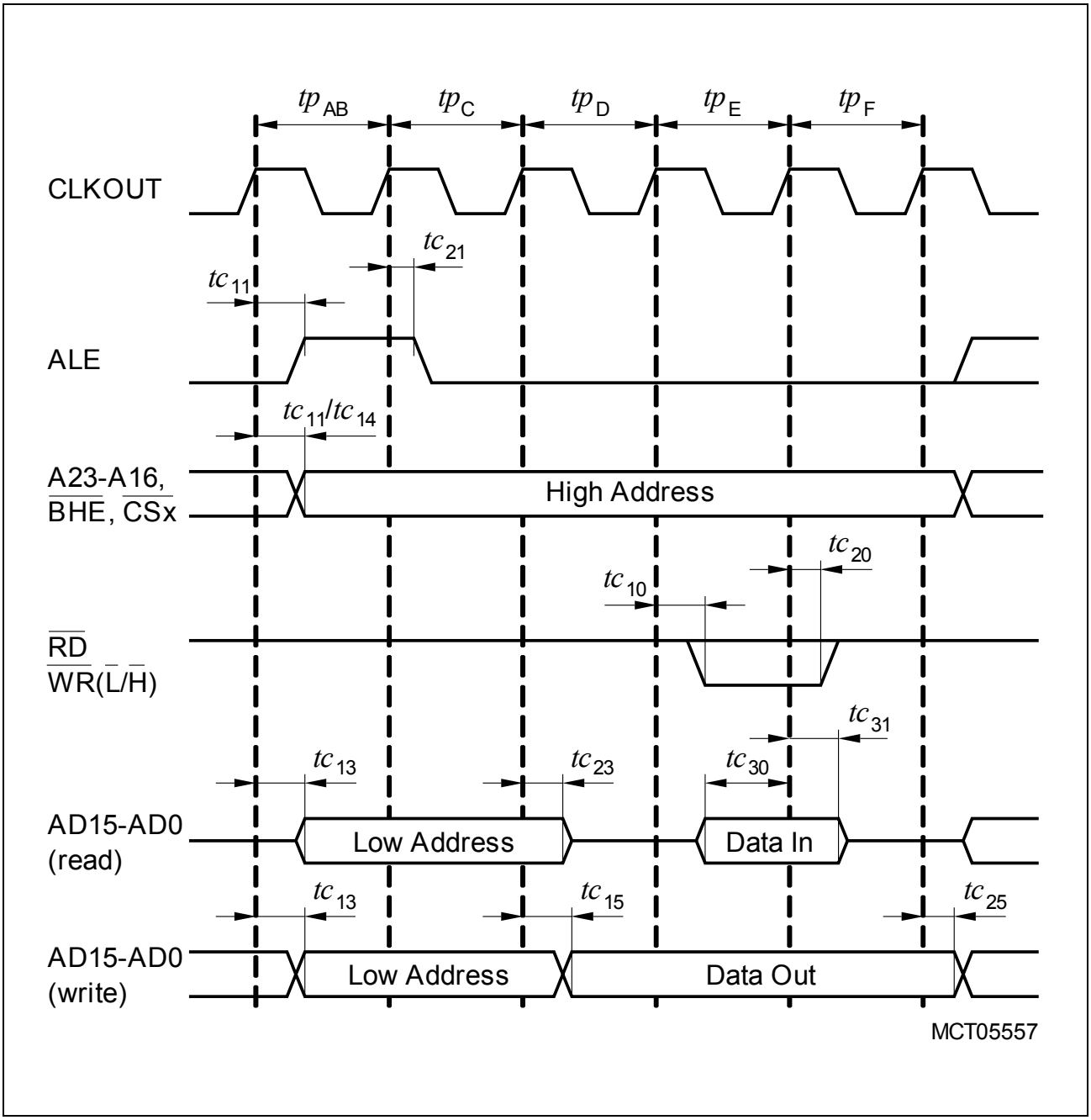

Figure 21 Multiplexed Bus Cycle

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