Infineon Technologies - XC164CS32F40FBBAKXQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cs32f40fbbakxqma1

XC164CS
Revision History: V1.1, 2006-08

Previous Version(s):
V1.0, 2005-06 (XC164-32F)

Page	Subjects (major changes since last revision)
6	New derivatives added.
51	Footnote at XTAL1 input pin.
55	Footnote on leakage of P3.15 added.
76	Green Package added.
75	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
mcdocu.comments@infineon.com

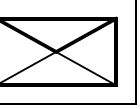


Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	63	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	64	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.4	65	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	66	I	$\overline{EA}$	External Access Enable pin. **A low level** at this pin during and after Reset forces the XC164CS to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the XC164CS to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	2	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

3 Functional Description

The architecture of the XC164CS combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164CS.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164CS.

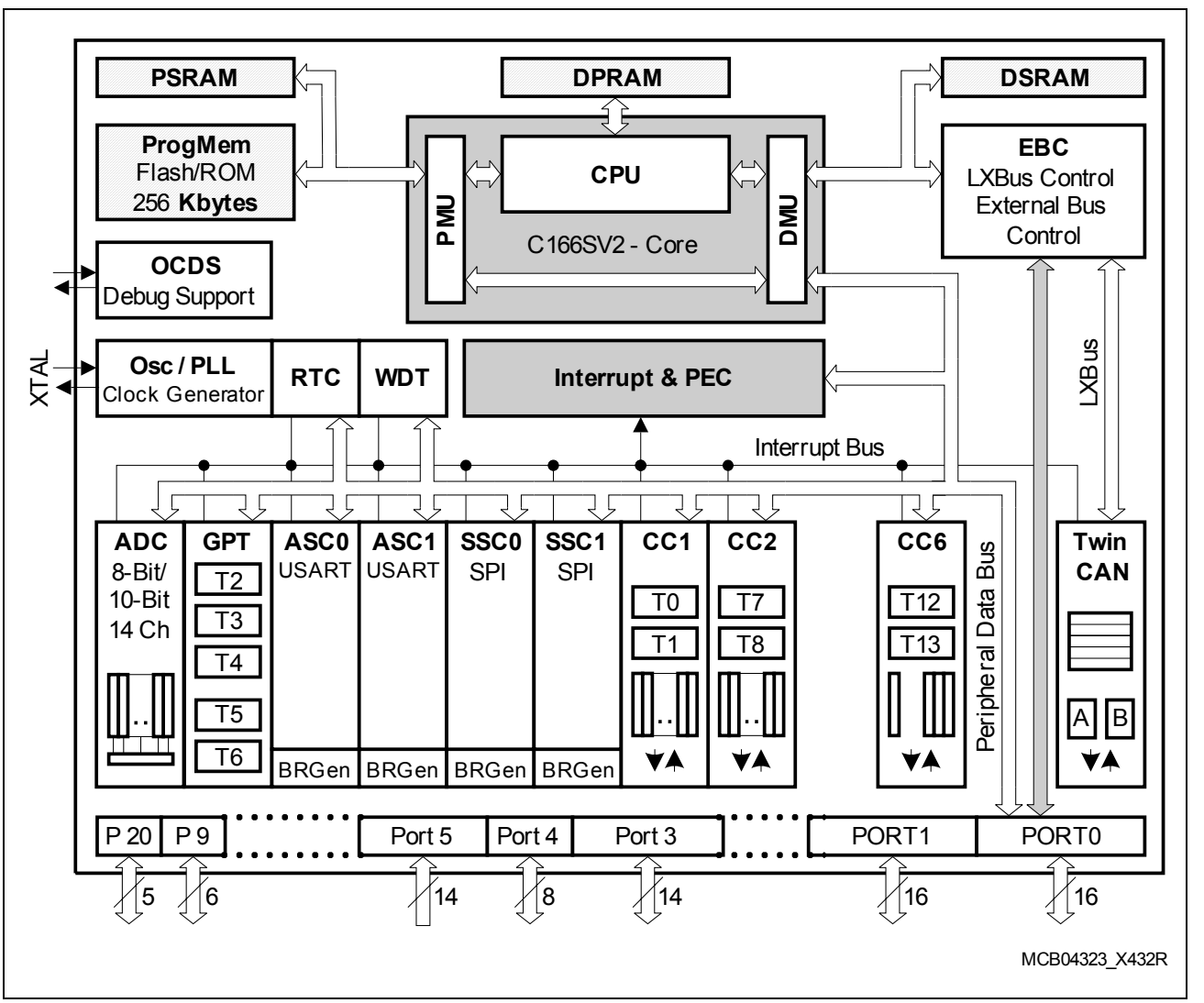


Figure 3 Block Diagram

3.1 Memory Subsystem and Organization

The memory space of the XC164CS is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

256 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and three 64-Kbyte sectors. Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
For timing characteristics, please refer to **Section 4.4.2**.

6 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

4 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7,

1) Each two 8-Kbyte sectors are combined for write-protection purposes.

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

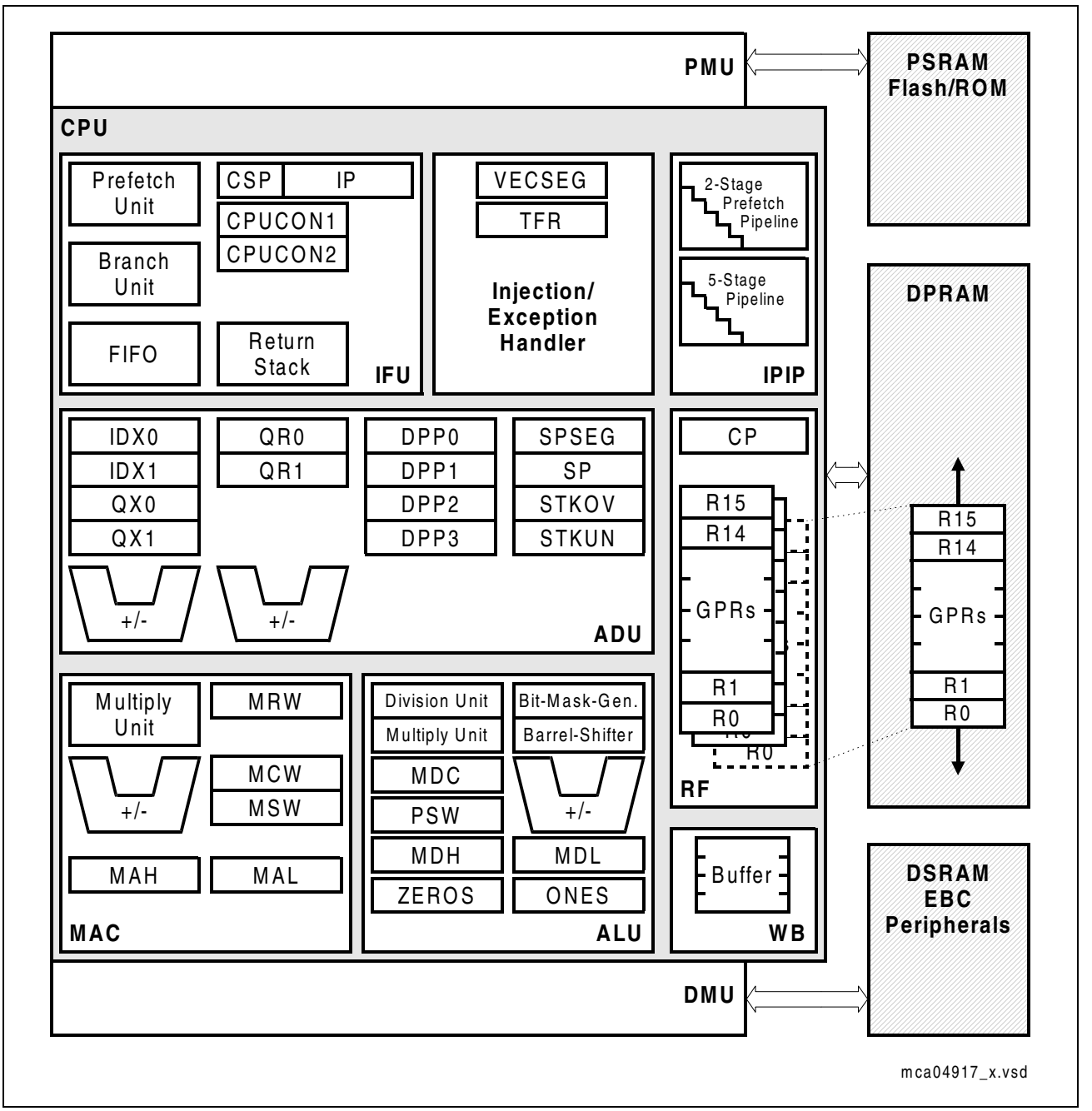


Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC164CS's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

The XC164CS also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	xx’0000$_H$	00$_H$	III
• Software Reset		RESET	xx’0000$_H$	00$_H$	III
• Watchdog Timer Overflow		RESET	xx’0000$_H$	00$_H$	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	xx’0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx’0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx’0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx’0020$_H$	08$_H$	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	xx’0028$_H$	0A$_H$	I
• PMI Access Error	PACER	BTRAP	xx’0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx’0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx’0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

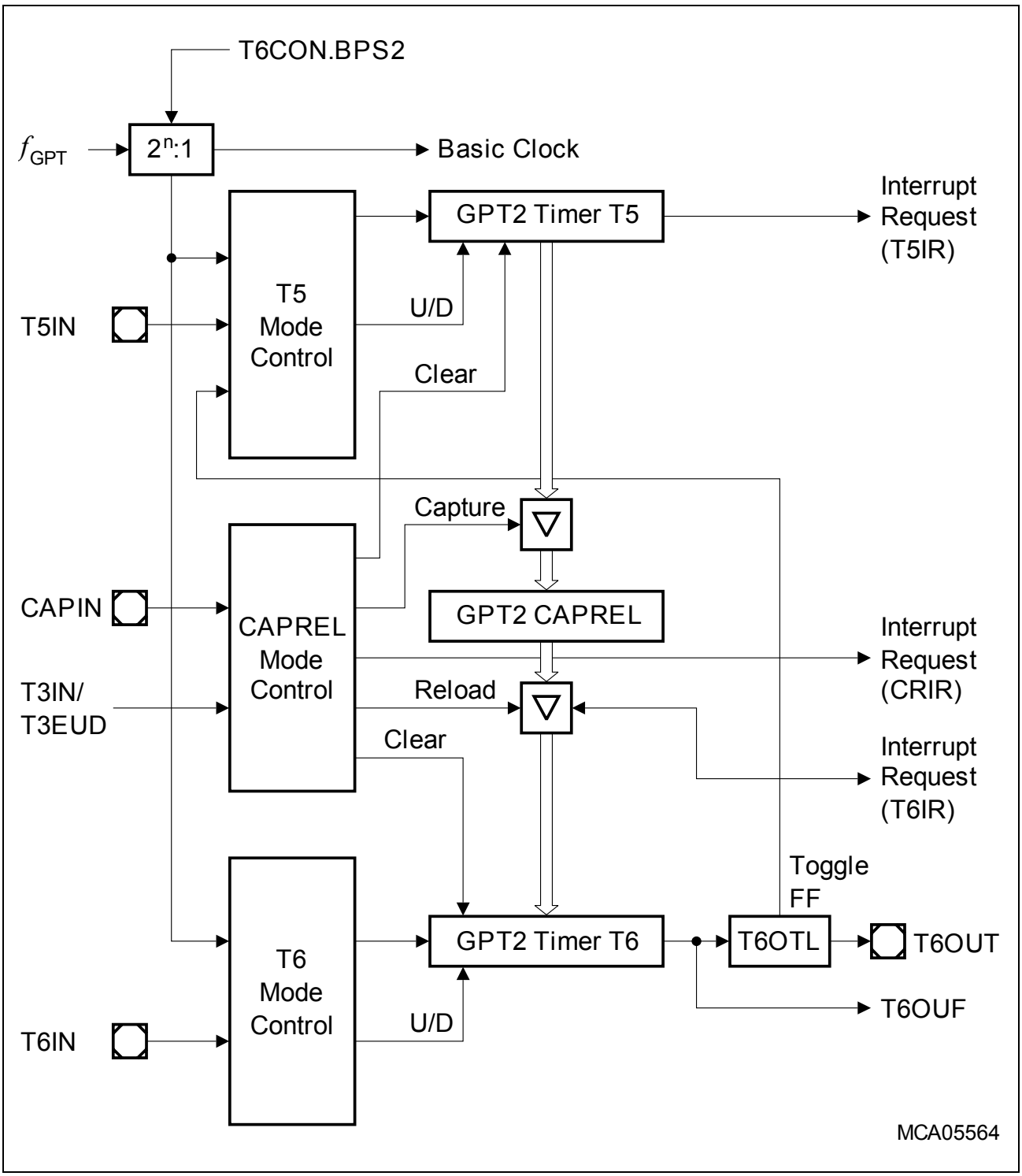


Figure 8 Block Diagram of GPT2

The RTC module can be used for different purposes:

- System clock to determine the current time and date,
  optionally during idle mode, sleep mode, and power down mode
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode
- 48-bit timer for long term measurements (maximum timespan is > 100 years)
- Alarm interrupt for wake-up on a defined time

3.18 Instruction Set Summary

Table 8 lists the instructions of the XC164CS in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 12 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Table 13 Power Consumption XC164CS (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	$10 + 3.0 \times f_{CPU}$	mA	f_{CPU} in [MHz][1)2)]
Pad supply current	I_{DDP}	–	5	mA	[3)]
Idle mode supply current with all peripherals active	I_{IDX}	–	$10 + 1.3 \times f_{CPU}$	mA	f_{CPU} in [MHz][2)]
Sleep and Power down mode supply current caused by leakage[4)]	I_{PDL}[5)]	–	$128{,}000 \times e^{-\alpha}$	mA	$V_{DDI} = V_{DDImax}$[6)] T_J in [°C] $\alpha = 4670 / (273 + T_J)$
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator[4)]	I_{PDM}[7)]	–	$0.6 + 0.02 \times f_{OSC} + I_{PDL}$	mA	$V_{DDI} = V_{DDImax}$ f_{OSC} in [MHz]

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 11**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.

4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator (if active).

5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 13**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC164CS is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC164CS.

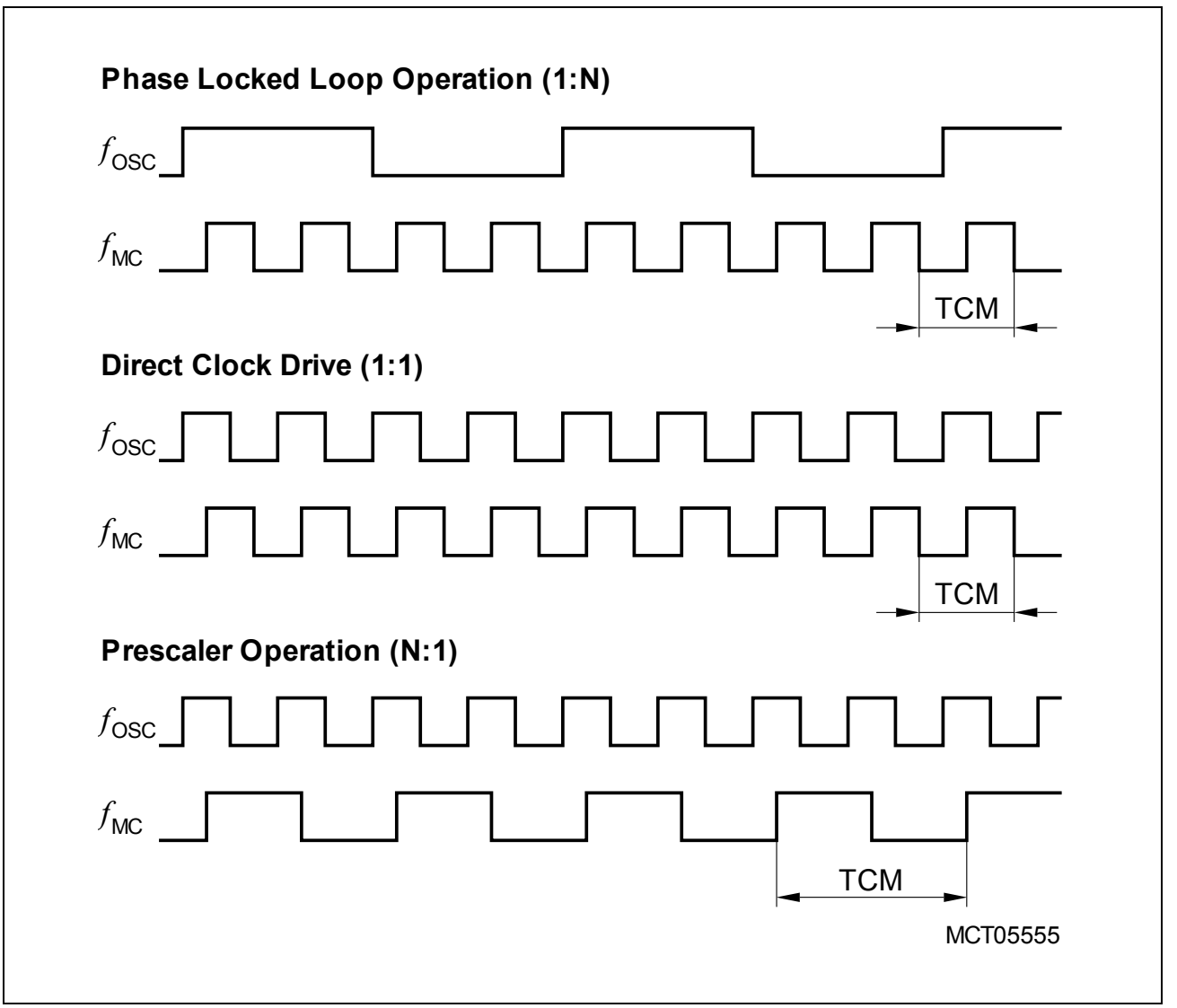


Figure 15 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 15** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

Table 16 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

4.4.2 On-chip Flash Operation

The XC164CS's Flash module delivers data within a fixed access time (see **Table 17**).

Accesses to the Flash module are controlled by the PMI and take 1 + WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. Therefore, the required Flash waitstates depend on the available speed grade as well as on the actual system frequency.

Note: The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15%.

Table 17 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time (Standard)	t_{ACC}	CC	–	–	70[1]	ns
Flash module access time (Grade A)	t_{ACC}	CC	–	–	50[1]	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[2]	5	ms
Erase time per sector	t_{ER}	CC	–	200[2]	500	ms

1) The actual access time is also influenced by the system frequency, so the frequency ranges are not fully linear. See **Table 18**.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), Standard devices must be operated with 2 waitstates: ((2 + 1) × 25 ns) ≥ 70 ns.
Grade A devices can be operated with 1 waitstate: ((1 + 1) × 25 ns) ≥ 50 ns.

Table 18 indicates the interrelation of waitstates, system frequency, and speed grade.

Table 18 Flash Access Waitstates

Required Waitstates	Frequency Range for Standard Flash Speed	Frequency Range for Flash Speed Grade A
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 16$ MHz	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 28$ MHz	$f_{CPU} \leq 40$ MHz
2 WS (WSFLASH = 10_B)	$f_{CPU} \leq 40$ MHz	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for xxx-32F20F devices).

4.4.3 External Clock Drive XTAL1

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1)]	ns
High time[2)]	t_1	SR	6	–	ns
Low time[2)]	t_2	SR	6	–	ns
Rise time[2)]	t_3	SR	–	8	ns
Fall time[2)]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

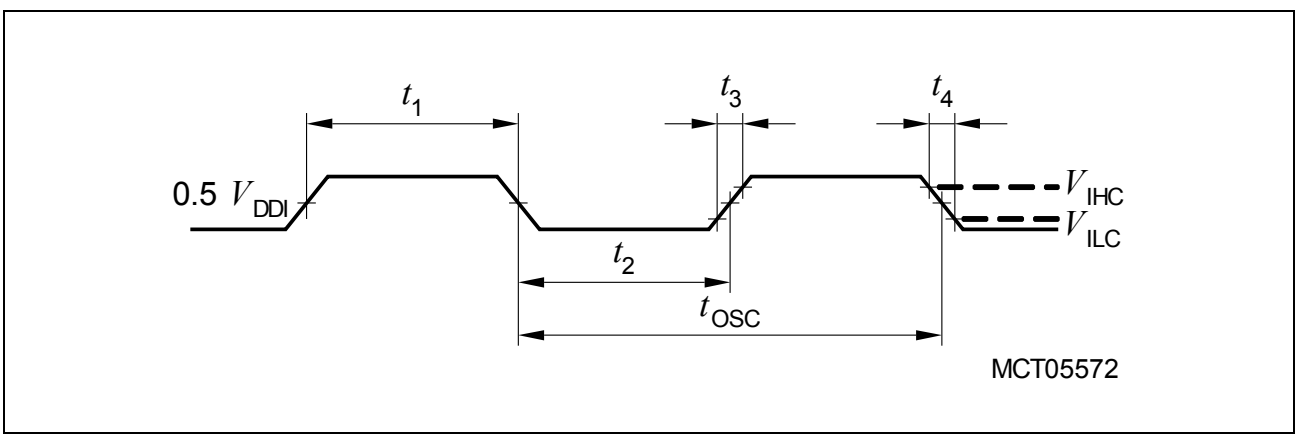
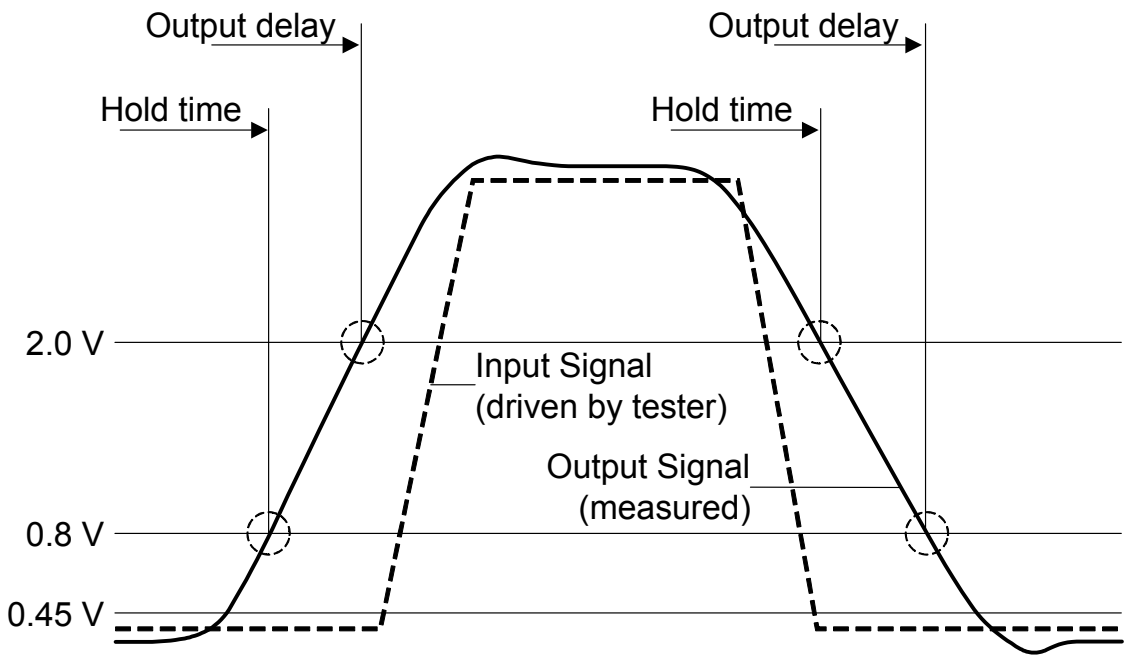


Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

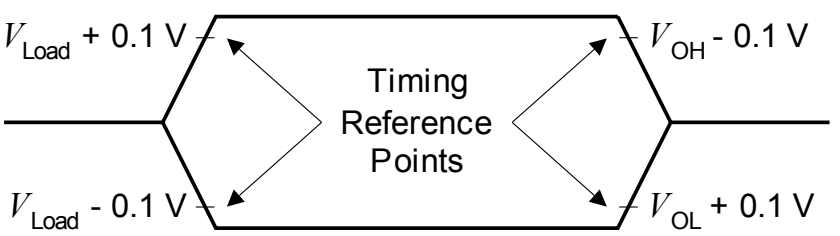
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 18 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 19 Float Waveforms

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1)]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

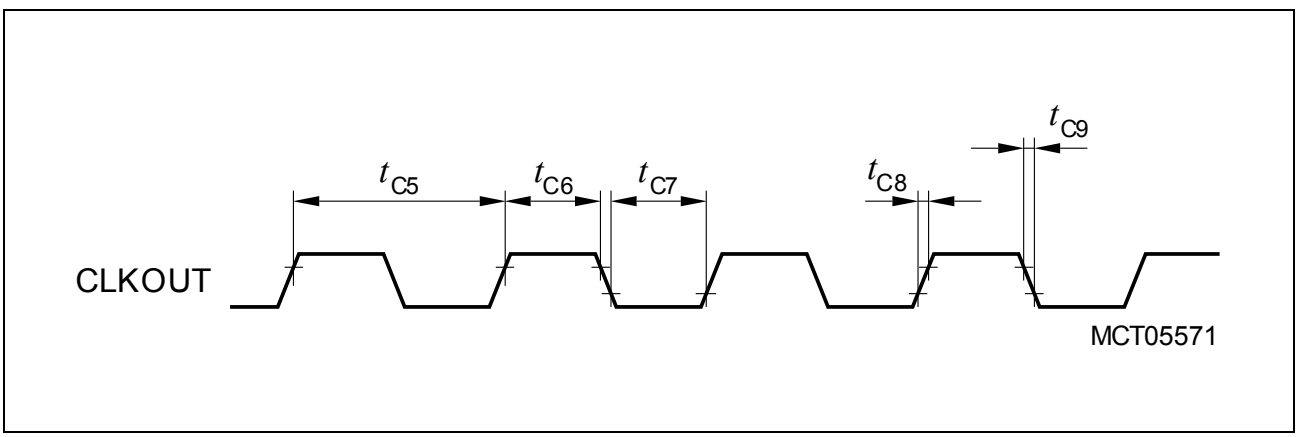


Figure 20 CLKOUT Signal Timing

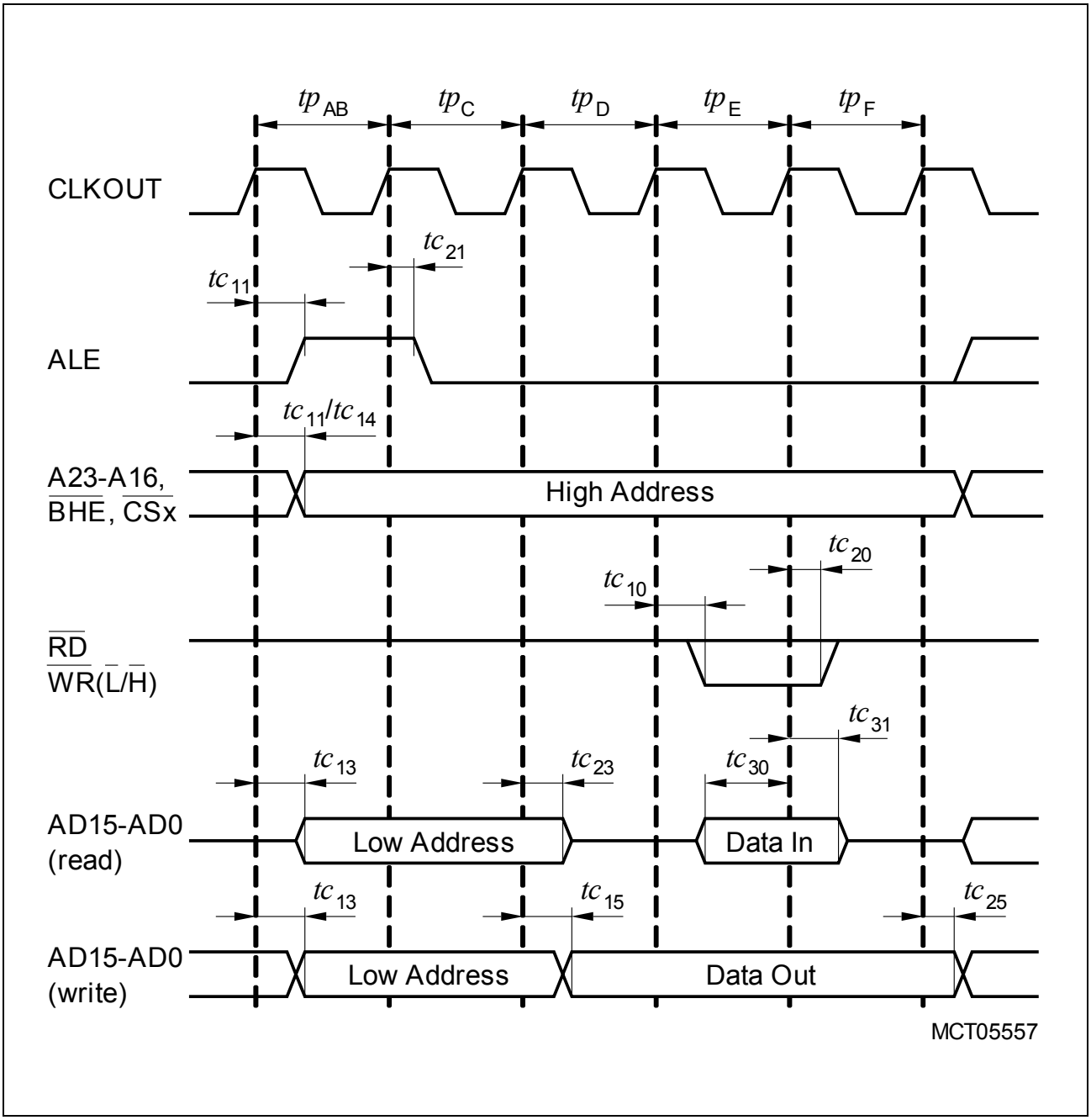


Figure 21 Multiplexed Bus Cycle

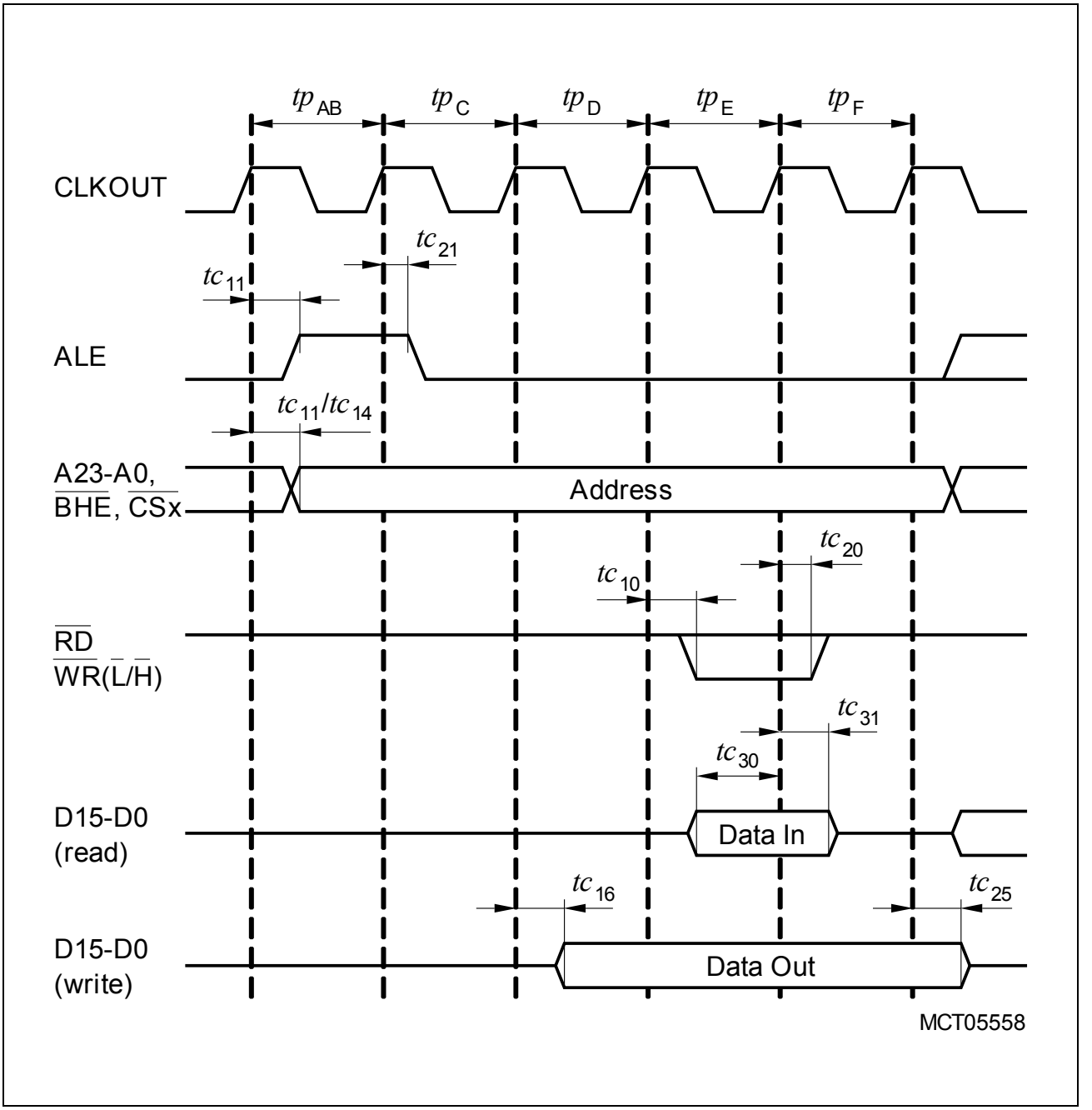
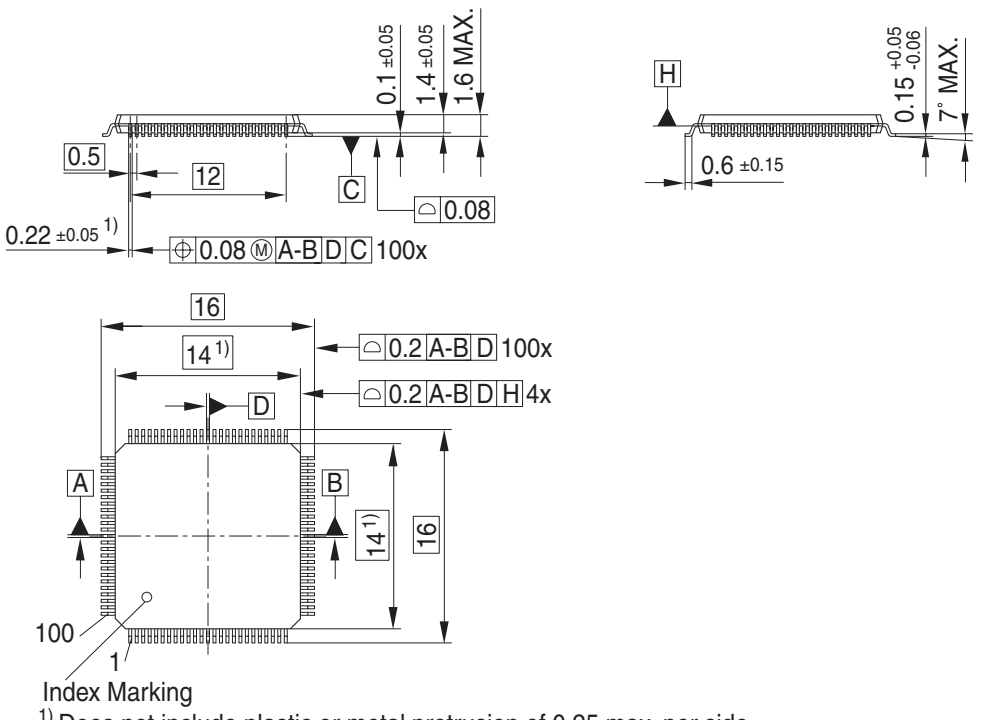


Figure 22 Demultiplexed Bus Cycle



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side at max. material condition

GPP09189

Figure 24 P-TQFP-100-16 (Plastic - Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm