Infineon Technologies - XC164CS32F40FBBAKXUMA1 Datasheet

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Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cs32f40fbbakxuma1

2 General Device Information

2.1 Introduction

The XC164CS derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.

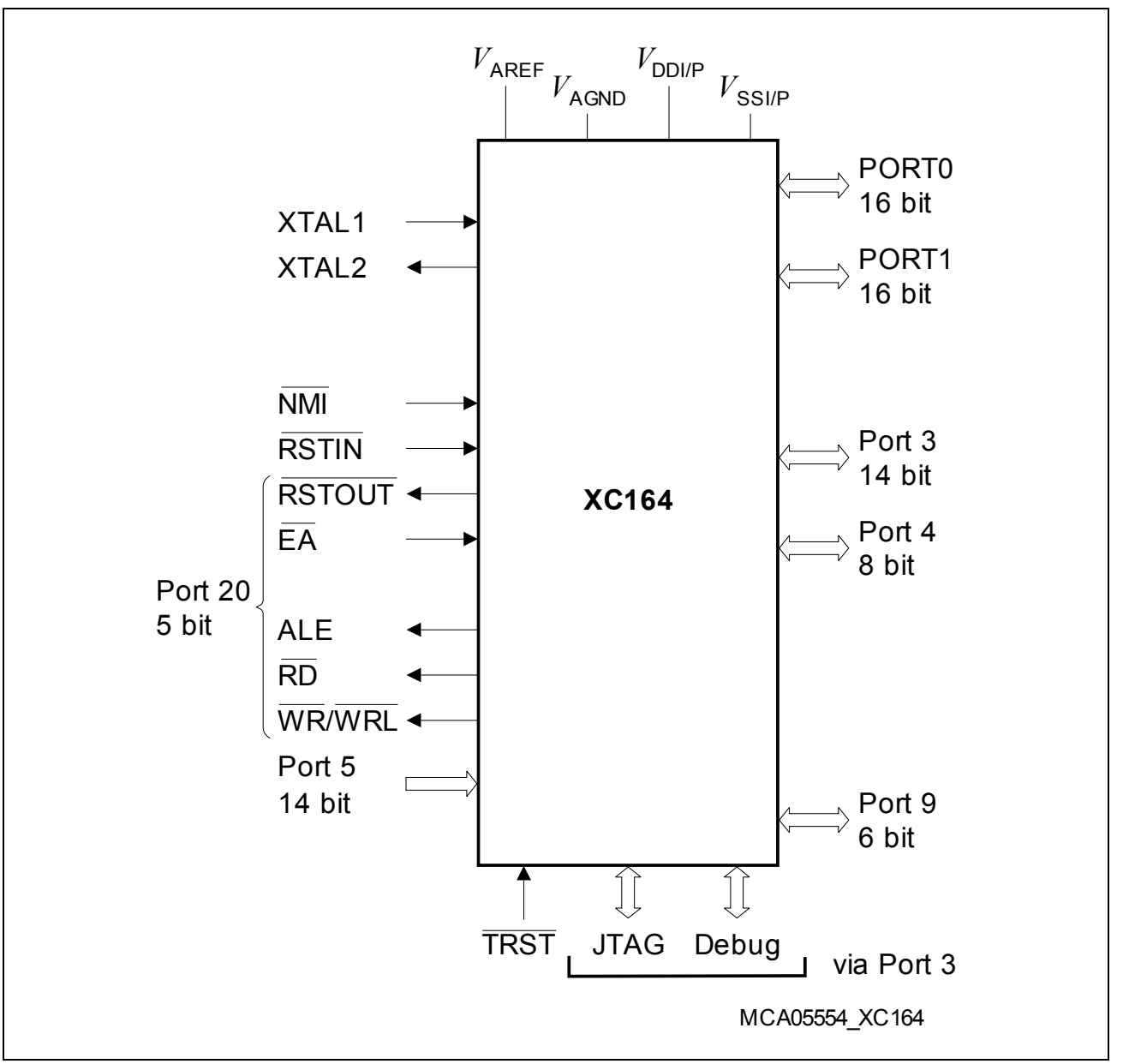


Figure 1 Logic Symbol

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
$\overline{\text{TRST}}$	36	I	Test-System Reset Input. A high level at this pin activates the XC164CS's debug system. For normal system operation, pin $\overline{\text{TRST}}$ should be held low.	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture In.,
		O	$\overline{\text{TxD1}}$	ASC0 Clock/Data Output (Async./Sync.),
		O	$\overline{\text{BRKOUT}}$	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	$\overline{\text{T2IN}}$	GPT1 Timer T2 Count/Gate/Reload/Capture In.,
		I	$\overline{\text{BRKIN}}$	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	$\overline{\text{EX2IN}}$	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]
P4.0	53	O	A16 Least Significant Segment Address Line,
		O	CS3 Chip Select 3 Output
P4.1	54	O	A17 Segment Address Line,
		O	CS2 Chip Select 2 Output
P4.2	55	O	A18 Segment Address Line,
		O	CS1 Chip Select 1 Output
P4.3	56	O	A19 Segment Address Line,
		O	CS0 Chip Select 0 Output
P4.4	57	O	A20 Segment Address Line,
		I	CAN1_RxD CAN Node B Receive Data Input,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin B)
P4.5	58	O	A21 Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin B)
P4.6	59	O	A22 Segment Address Line,
		O	CAN0_TxD CAN Node A Transmit Data Output,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin A)
P4.7	60	O	A23 Most Significant Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		O	CAN1_TxD CAN Node B Transmit Data Output,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	63	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	64	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.4	65	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	66	I	$\overline{EA}$	External Access Enable pin. **A low level** at this pin during and after Reset forces the XC164CS to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the XC164CS to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	2	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{DDI}	35, 97	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Condition Parameters**.
V_{DDP}	9, 17, 38, 61, 87	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Condition Parameters**.
V_{SSI}	34, 98	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	8, 16, 37, 62, 88	–	

1) The CAN interface lines are assigned to ports P4 and P9 under software control.

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a division algorithm is performed in 18 to 21 CPU cycles, depending on the data and division type. Four cycles are always visible, the rest runs in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. The global register bank is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active global register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164CS instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 4 XC164CS Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$

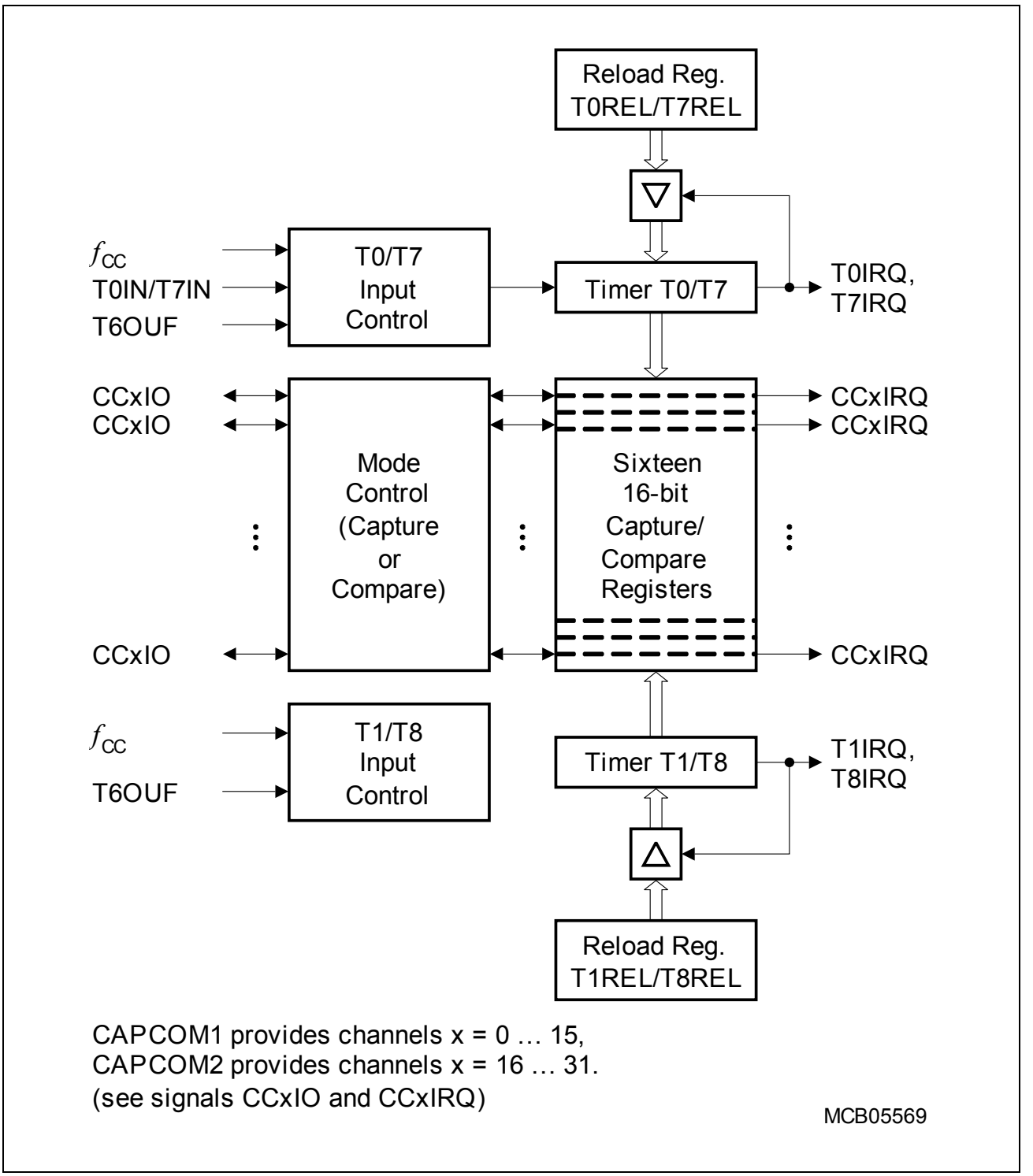


Figure 5 CAPCOM1/2 Unit Block Diagram

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
   Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.
6) Not subject to production test - verified by design/characterization.
7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
   The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.
8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164CS and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC164CS will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the XC164CS.

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Level inactive hold current[13]	I_{LHI}[10]		–	-10	µA	V_{OUT} = 0.5 × V_{DDP}
Level active hold current[13]	I_{LHA}[11]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[14] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) This parameter is tested for P3, P4, P9.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

9) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0

10) The maximum current may be drawn while the respective signal line remains inactive.

11) The minimum current must be drawn to drive the respective signal line active.

12) This specification is valid during Reset for configuration on ALE.

13) This specification is valid during Reset for pins P4.3-0, which can act as $\overline{CS}$ outputs, and for P3.12.

14) Not subject to production test - verified by design/characterization.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 12**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	kΩ	6)

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

Sample time and conversion time of the XC164CS's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using **Table 15**.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 15 A/D Converter Computation Table[1)]

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample Time t_S
00	f_{SYS} / 4	00	$t_{BC} \times 8$
01	f_{SYS} / 2	01	$t_{BC} \times 16$
10	f_{SYS} / 16	10	$t_{BC} \times 32$
11	f_{SYS} / 8	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), ADCTC = '01', ADSTC = '00'
Basic clock f_{BC} = f_{SYS} / 2 = 20 MHz, i.e. t_{BC} = 50 ns
Sample time t_S = $t_{BC} \times 8$ = 400 ns
Conversion 10-bit:
With post-calibr. t_{C10P} = $52 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2600 + 400 + 150) ns = 3.15 µs
Post-calibr. off t_{C10} = $40 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2000 + 400 + 150) ns = 2.55 µs
Conversion 8-bit:
With post-calibr. t_{C8P} = $44 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (2200 + 400 + 150) ns = 2.75 µs
Post-calibr. off t_{C8} = $32 \times t_{BC} + t_S + 6 \times t_{SYS}$ = (1600 + 400 + 150) ns = 2.15 µs

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC164CS is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC164CS.

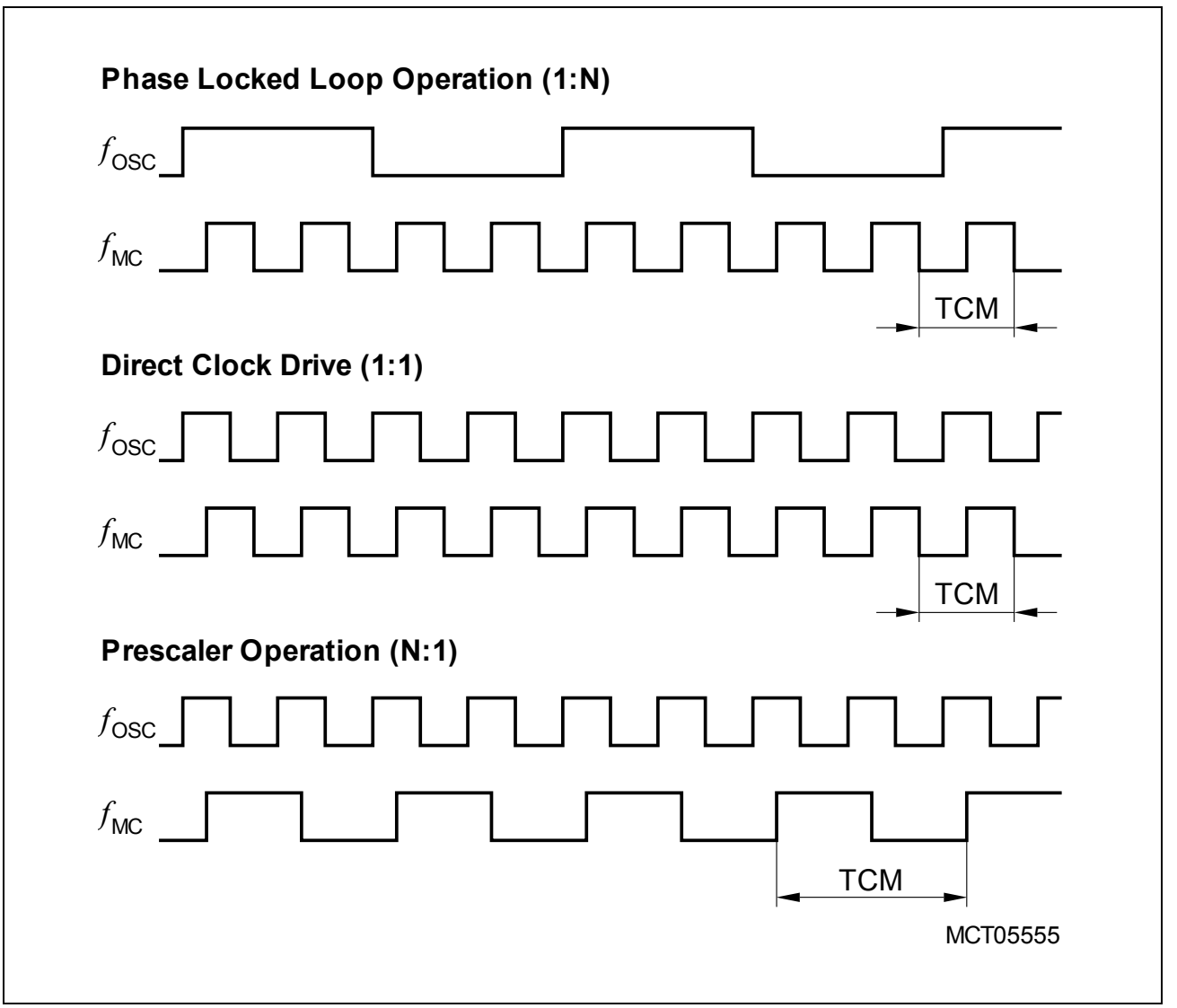


Figure 15 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 15** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as K × **N**, where **N** is the number of consecutive f_{MC} cycles (TCM).

For a period of **N** × TCM the accumulated PLL jitter is defined by the deviation D_N:

D_N [ns] = ±(1.5 + 6.32 × **N** / f_{MC}); f_{MC} in [MHz], **N** = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: D_3 = ±(1.5 + 6.32 × **3** / 20) = 2.448 ns.

This formula is applicable for K × **N** < 95. For longer periods the K × **N** = 95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).

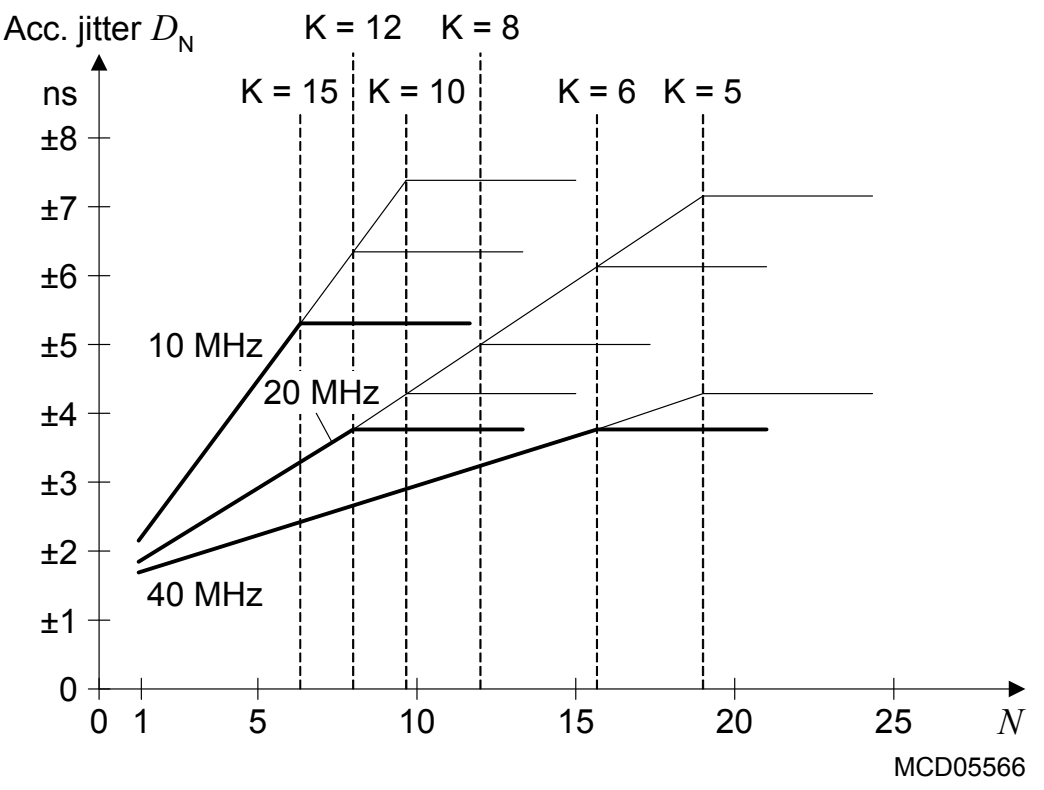


Figure 16 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

4.4.3 External Clock Drive XTAL1

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1)]	ns
High time[2)]	t_1	SR	6	–	ns
Low time[2)]	t_2	SR	6	–	ns
Rise time[2)]	t_3	SR	–	8	ns
Fall time[2)]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

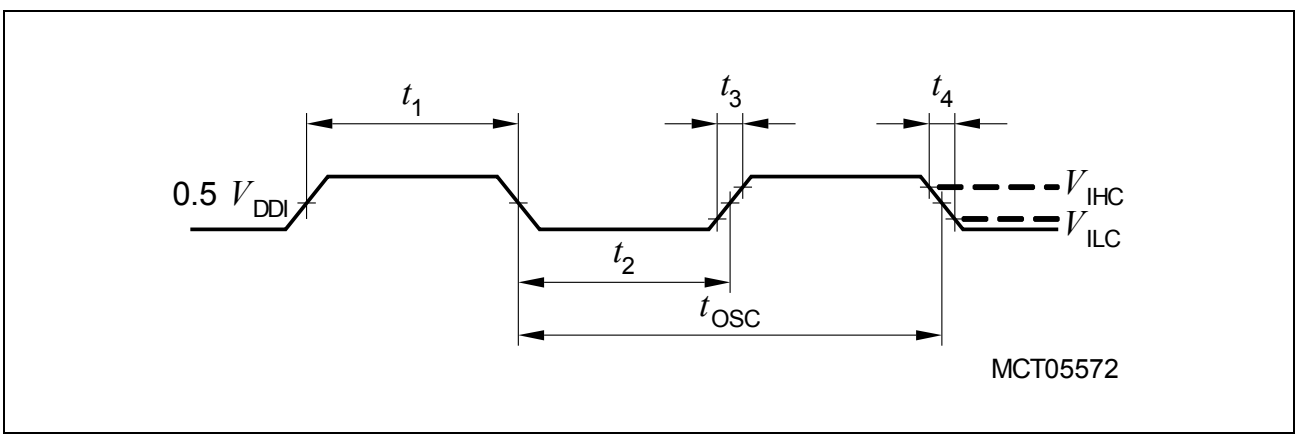
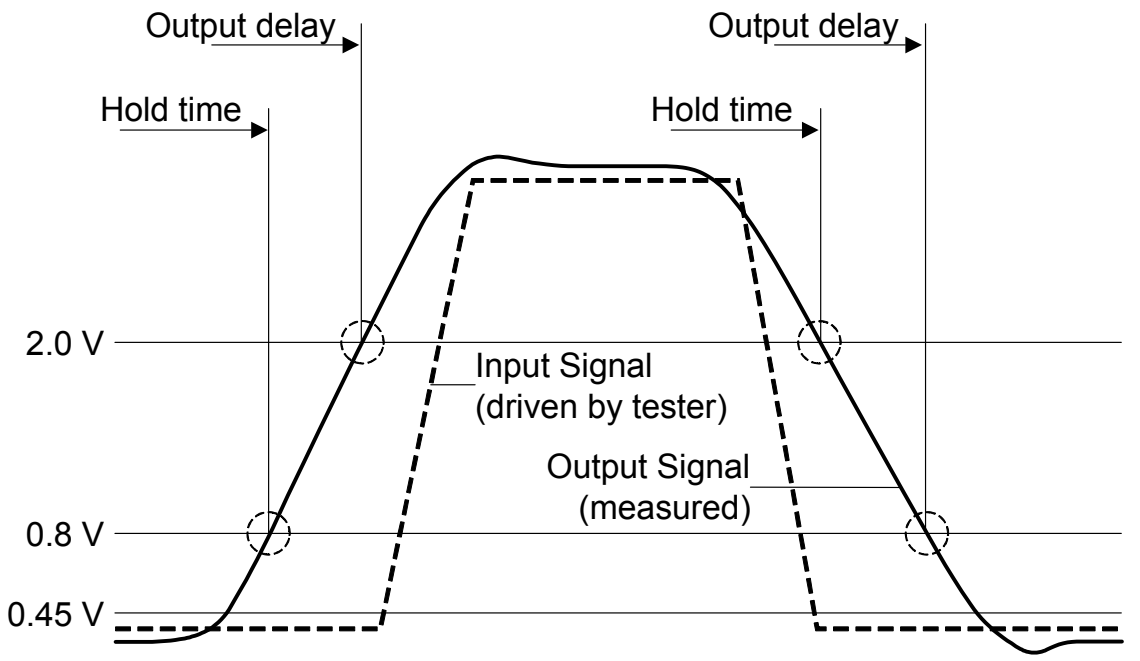


Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

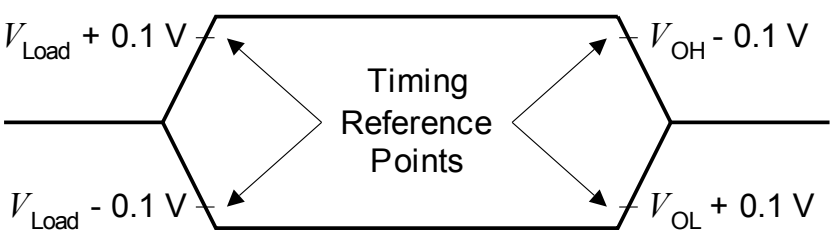
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 18 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 19 Float Waveforms

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1)]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

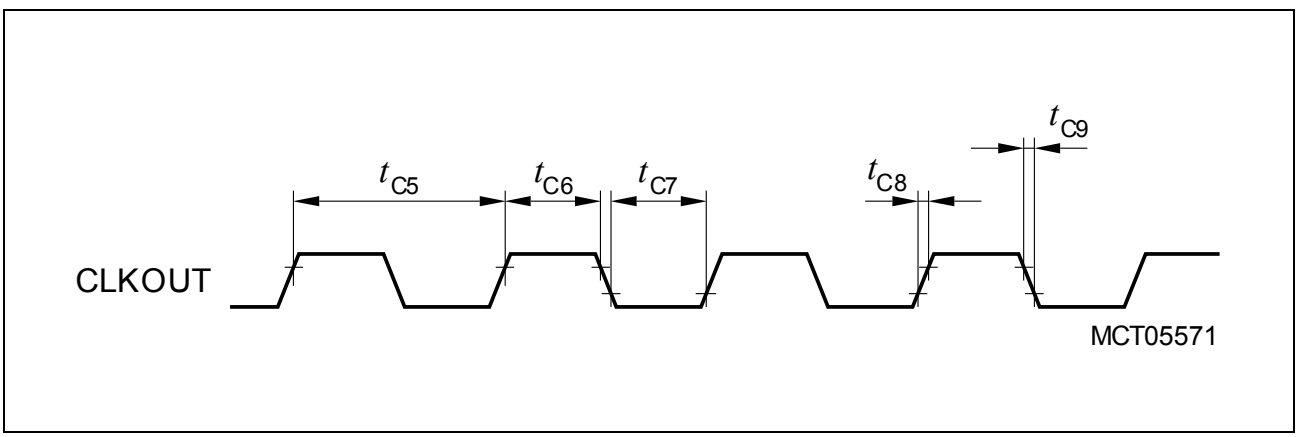


Figure 20 CLKOUT Signal Timing