



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 27x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dn512vlk10

Table of Contents

1 Ordering parts.....	4	6 Peripheral operating requirements and behaviors.....	23
1.1 Determining valid orderable parts.....	4	6.1 Core modules.....	23
2 Part identification.....	4	6.1.1 Debug trace timing specifications.....	23
2.1 Description.....	4	6.1.2 JTAG electricals.....	24
2.2 Format.....	4	6.2 System modules.....	27
2.3 Fields.....	4	6.3 Clock modules.....	27
2.4 Example.....	5	6.3.1 MCG specifications.....	27
3 Terminology and guidelines.....	5	6.3.2 Oscillator electrical specifications.....	29
3.1 Definition: Operating requirement.....	5	6.3.3 32 kHz oscillator electrical characteristics.....	32
3.2 Definition: Operating behavior.....	6	6.4 Memories and memory interfaces.....	32
3.3 Definition: Attribute.....	6	6.4.1 Flash electrical specifications.....	32
3.4 Definition: Rating.....	7	6.4.2 EzPort switching specifications.....	34
3.5 Result of exceeding a rating.....	7	6.4.3 Flexbus switching specifications.....	35
3.6 Relationship between ratings and operating requirements.....	7	6.5 Security and integrity modules.....	38
3.7 Guidelines for ratings and operating requirements.....	8	6.6 Analog.....	38
3.8 Definition: Typical value.....	8	6.6.1 ADC electrical specifications.....	38
3.9 Typical value conditions.....	9	6.6.2 CMP and 6-bit DAC electrical specifications.....	46
4 Ratings.....	10	6.6.3 12-bit DAC electrical characteristics.....	49
4.1 Thermal handling ratings.....	10	6.6.4 Voltage reference electrical specifications.....	52
4.2 Moisture handling ratings.....	10	6.7 Timers.....	53
4.3 ESD handling ratings.....	10	6.8 Communication interfaces.....	53
4.4 Voltage and current operating ratings.....	10	6.8.1 USB electrical specifications.....	53
5 General.....	11	6.8.2 USB DCD electrical specifications.....	54
5.1 AC electrical characteristics.....	11	6.8.3 USB VREG electrical specifications.....	54
5.2 Nonswitching electrical specifications.....	11	6.8.4 CAN switching specifications.....	55
5.2.1 Voltage and current operating requirements.....	12	6.8.5 DSPI switching specifications (limited voltage range).....	55
5.2.2 LVD and POR operating requirements.....	13	6.8.6 DSPI switching specifications (full voltage range).....	56
5.2.3 Voltage and current operating behaviors.....	13	6.8.7 Inter-Integrated Circuit Interface (I2C) timing.....	58
5.2.4 Power mode transition operating behaviors.....	15	6.8.8 UART switching specifications.....	59
5.2.5 Power consumption operating behaviors.....	16	6.8.9 SDHC specifications.....	59
5.2.6 EMC radiated emissions operating behaviors.....	19	6.8.10 I2S/SAI switching specifications.....	60
5.2.7 Designing with radiated emissions in mind.....	20	6.9 Human-machine interfaces (HMI).....	67
5.2.8 Capacitance attributes.....	20	6.9.1 TSI electrical specifications.....	67
5.3 Switching specifications.....	20	7 Dimensions.....	68
5.3.1 Device clock specifications.....	20	7.1 Obtaining package dimensions.....	68
5.3.2 General switching specifications.....	21	8 Pinout.....	68
5.4 Thermal specifications.....	22	8.1 K20 signal multiplexing and pin assignments.....	68
5.4.1 Thermal operating requirements.....	22	8.2 K20 pinouts.....	72
5.4.2 Thermal attributes.....	22		

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = -40 to 105 • C = -40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK20DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

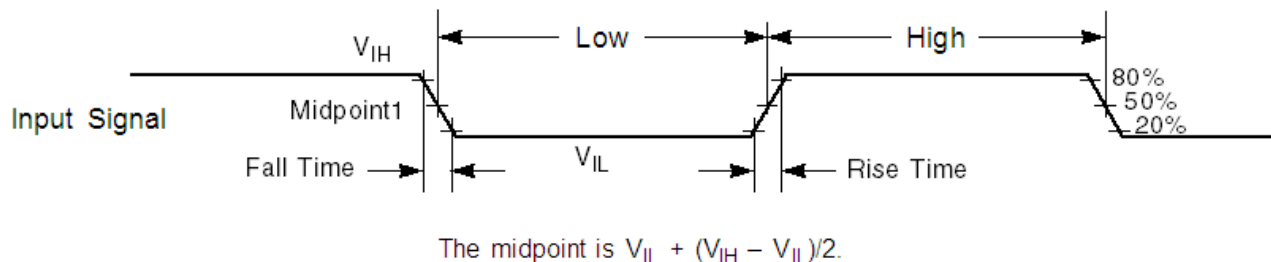


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. V_{DD} slew rate ≥ 5.7 kV/s V_{DD} slew rate < 5.7 kV/s	—	300	μs	1
	• VLLS1 $\rightarrow$ RUN	—	130	μs	
	• VLLS2 $\rightarrow$ RUN	—	92	μs	
	• VLLS3 $\rightarrow$ RUN	—	92	μs	
	• LLS $\rightarrow$ RUN	—	5.9	μs	
	• VLPS $\rightarrow$ RUN	—	5.0	μs	
	• STOP $\rightarrow$ RUN	—	5.0	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	—	37	63	mA	2
		—	38	64	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V @ 25°C @ 125°C	—	46	77	mA	3, 4
		—	47	63	mA	
		—	58	79	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	20	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	9	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.12	—	mA	6

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8V @ -40 to 25°C @ 70°C @ 105°C @ 3.0V @ -40 to 25°C @ 70°C @ 105°C	—	0.57	0.67	μA	10
		—	0.90	1.2	μA	
		—	2.4	3.5	μA	
		—	0.67	0.94	μA	
		—	1.0	1.4	μA	
		—	2.7	3.9	μA	
		—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 μA.
10. Includes 32kHz oscillator current and RTC operation.

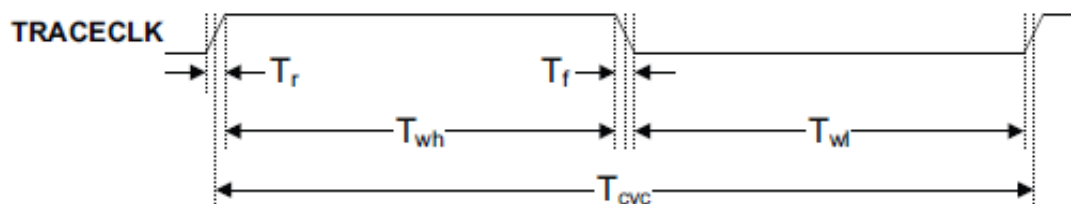
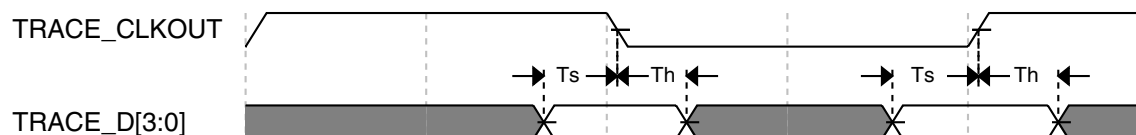
5.2.5.1 Diagram: Typical I_{DD_RUN} operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

Table 12. Debug trace operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns


Figure 3. TRACE_CLKOUT specifications

Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns

Table continues on the next page...

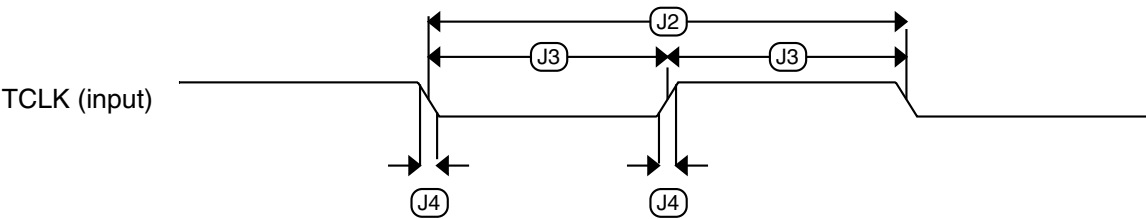


Figure 5. Test clock input timing

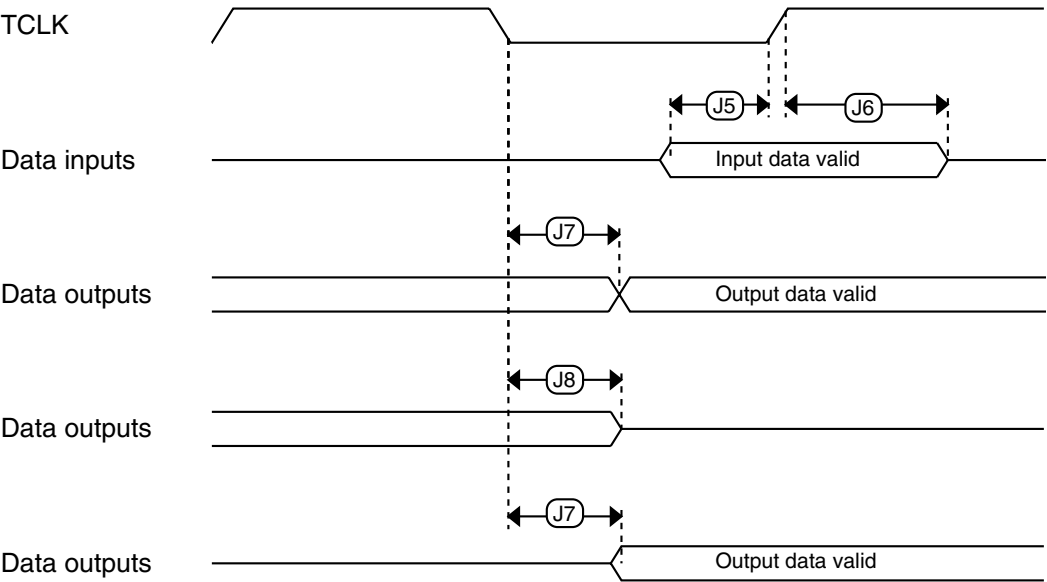
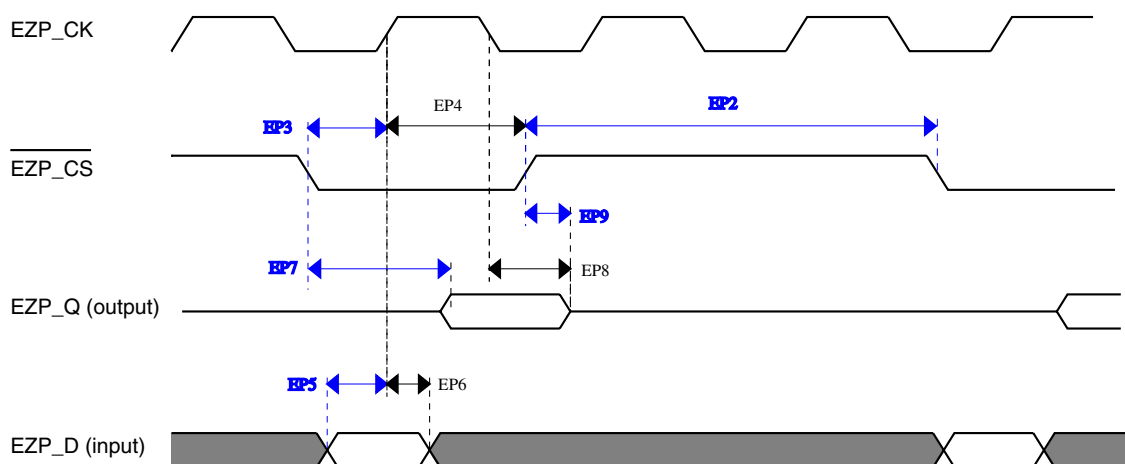


Figure 6. Boundary scan (JTAG) timing

Table 24. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{\text{SYS}}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns


Figure 9. EzPort Timing Diagram

6.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

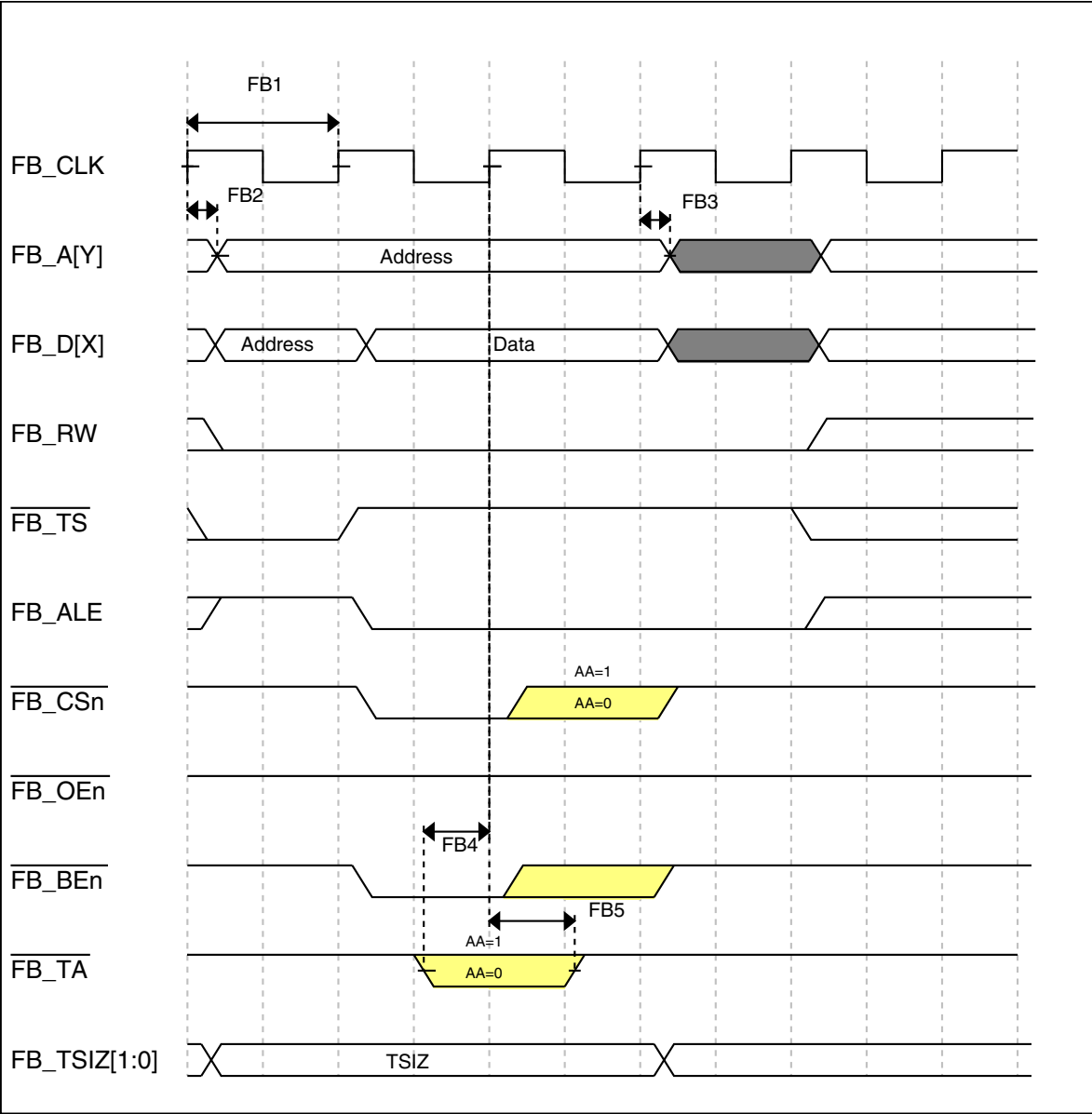


Figure 11. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 27](#) and [Table 28](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 29](#) and [Table 30](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode - All other modes	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	
C _{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

Table continues on the next page...

Table 27. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $Temp = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\text{ }\Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, $CFG2[ADHSC]$ must be set and $CFG1[ADLPC]$ must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

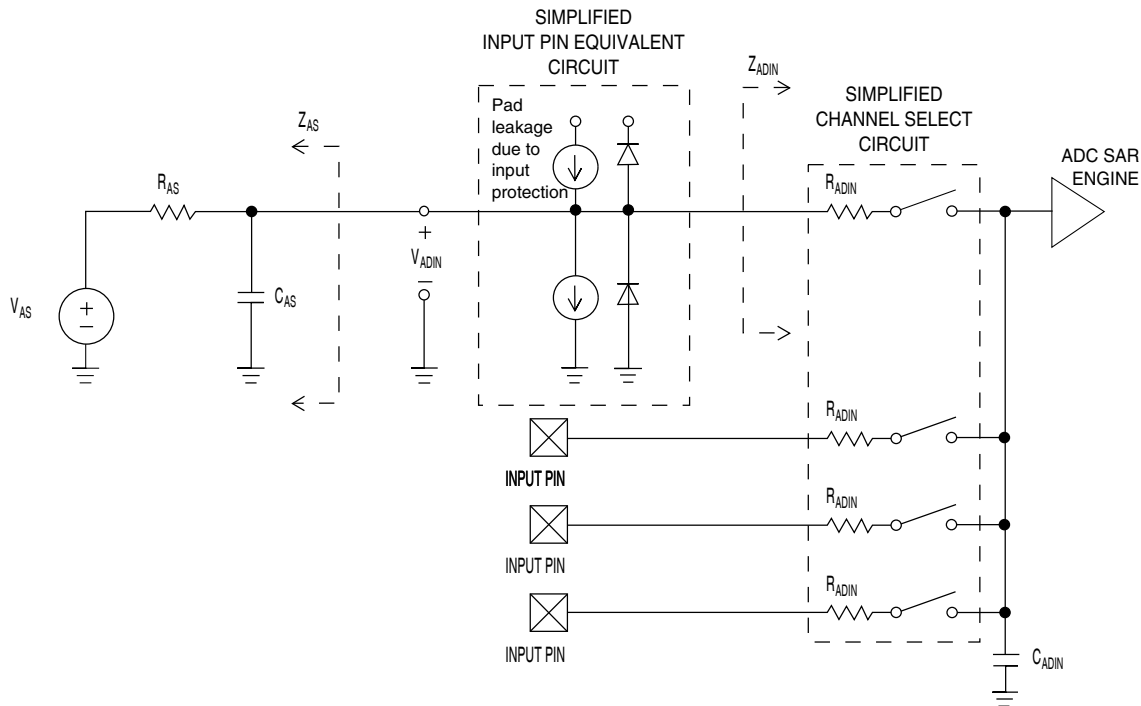


Figure 12. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	± 0.7 ± 0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	± 1.0 ± 0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤ 13-bit modes	— —	-1 to 0 —	— ± 0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{IN} \times R_{AS}$		mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

Typical ADC 16-bit Differential ENOB vs ADC Clock
100Hz, 90% FS Sine Input

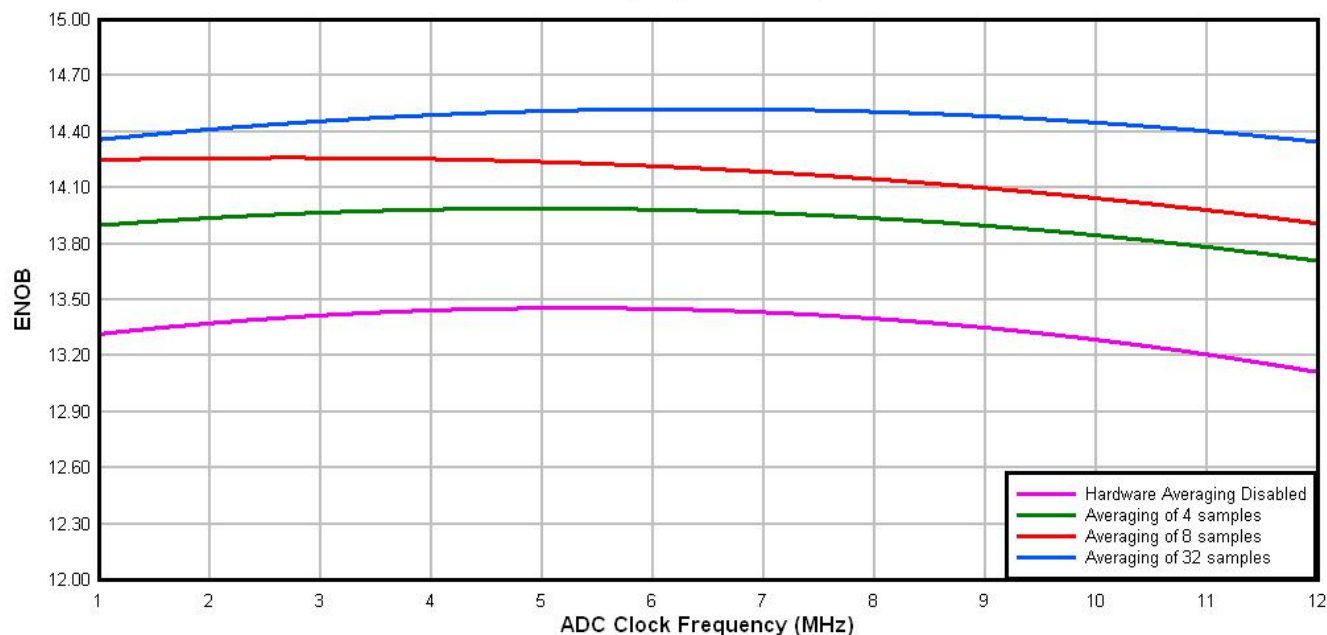

Figure 13. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Table 30. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
G	Gain ⁴	- PGAG=0 - PGAG=1 - PGAG=2 - PGAG=3 - PGAG=4 - PGAG=5 - PGAG=6	0.95	1	1.05		R _{AS} < 100Ω
BW	Input signal bandwidth	16-bit modes < 16-bit modes	—	—	4	kHz	
			—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode rejection ratio	- Gain=1 - Gain=64	—	-84	—	dB	V _{CM} = 500mVpp, f _{VCM} = 50Hz, 100Hz
			—	-85	—	dB	
V _{OFS}	Input offset voltage		—	0.2	—	mV	Output offset = V _{OFS} *(Gain+1)
T _{GSW}	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over full temperature range	- Gain=1 - Gain=64	—	6	10	ppm/°C	
			—	31	42	ppm/°C	
dG/dV _{DDA}	Gain drift over supply voltage	- Gain=1 - Gain=64	—	0.07	0.21	%/V	V _{DDA} from 1.71 to 3.6V
			—	0.14	0.31	%/V	
E _{IL}	Input leakage error	All modes	I _{in} × R _{AS}			mV	I _{in} = leakage current (refer to the MCU's voltage and current operating ratings)
V _{PP,DIFF}	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{\text{Gain}} \right)$ where V _X = V _{REFPGA} × 0.583			V	6
SNR	Signal-to-noise ratio	- Gain=1 - Gain=64	80	90	—	dB	16-bit differential mode, Average=32
			52	66	—	dB	
THD	Total harmonic distortion	- Gain=1 - Gain=64	85	100	—	dB	16-bit differential mode, Average=32, f _{in} =100Hz
			49	95	—	dB	

Table continues on the next page...

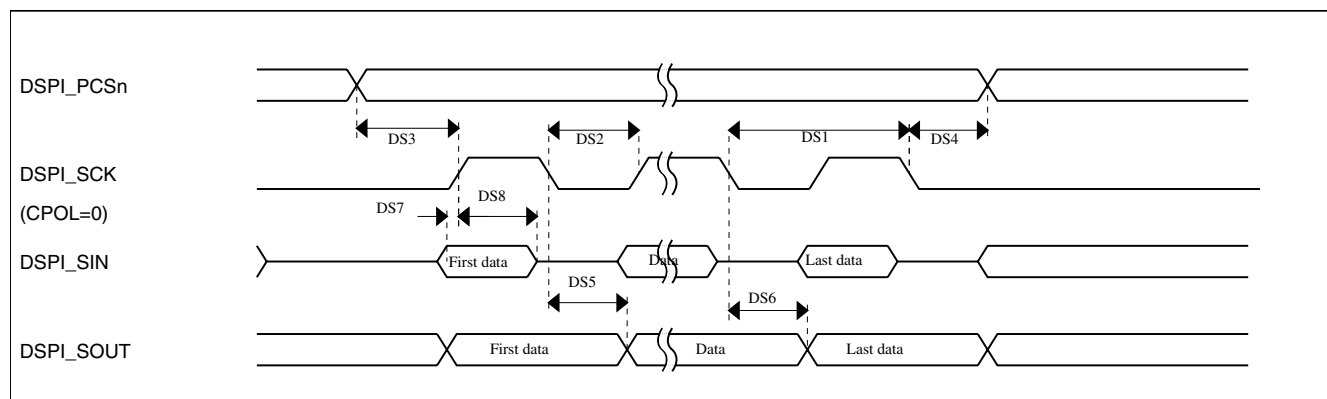


Figure 19. DSPI classic SPI timing — master mode

Table 41. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns

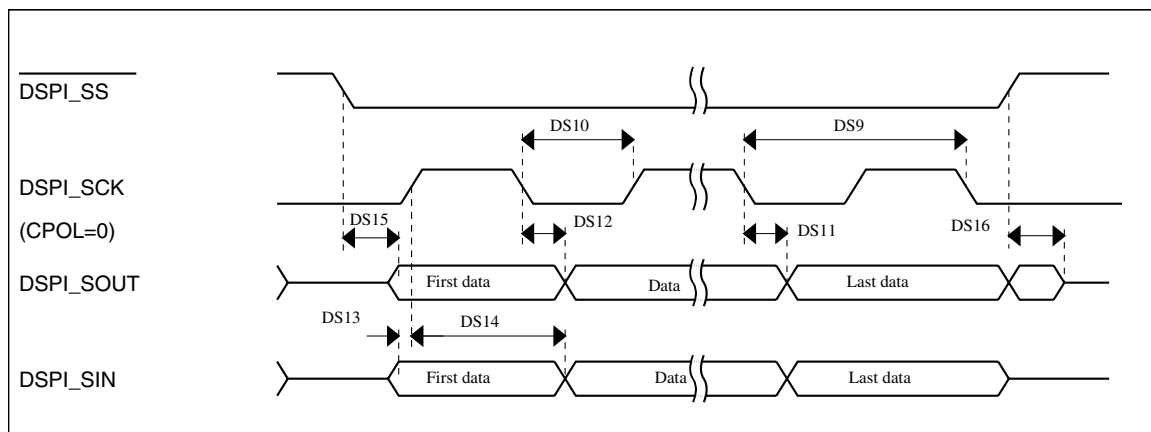


Figure 20. DSPI classic SPI timing — slave mode

6.8.6 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 42. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

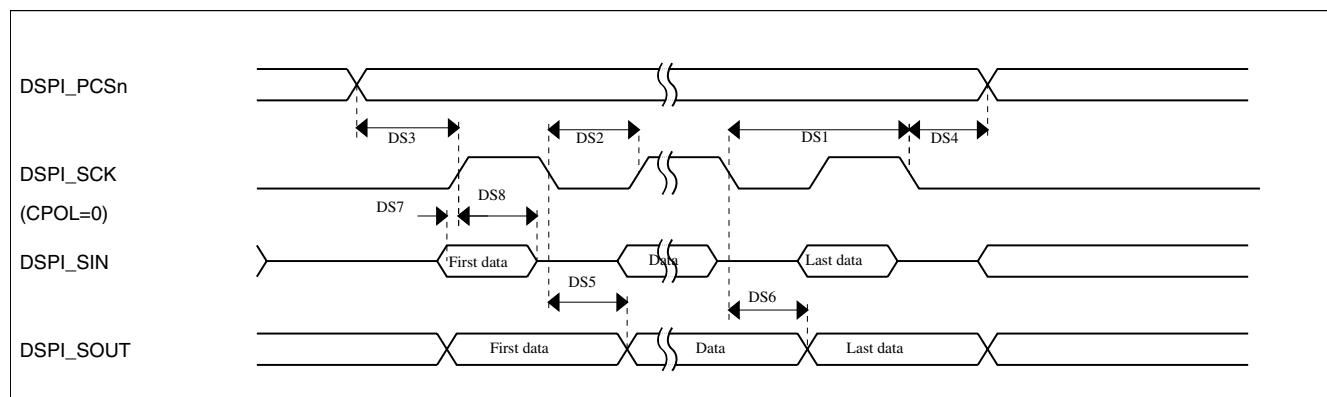


Figure 21. DSPI classic SPI timing — master mode

Table 43. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz

Table continues on the next page...

6.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 45. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
Card input clock					
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

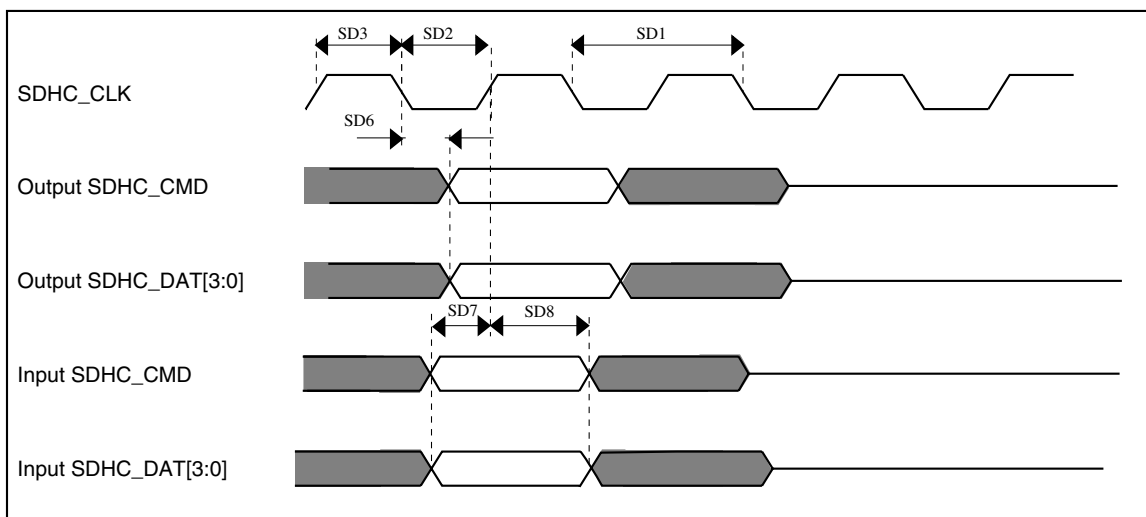


Figure 24. SDHC timing

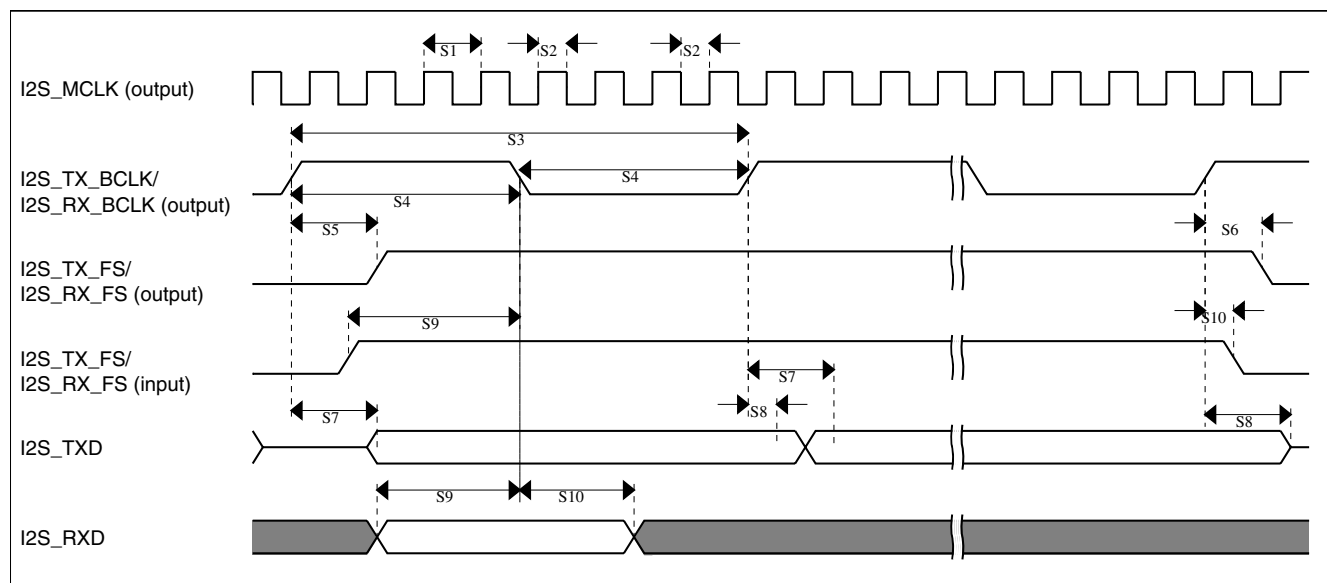


Figure 25. I2S/SAI timing — master modes

Table 47. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid - Multiple SAI Synchronous mode - All other modes	—	21	ns
		—	15	
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

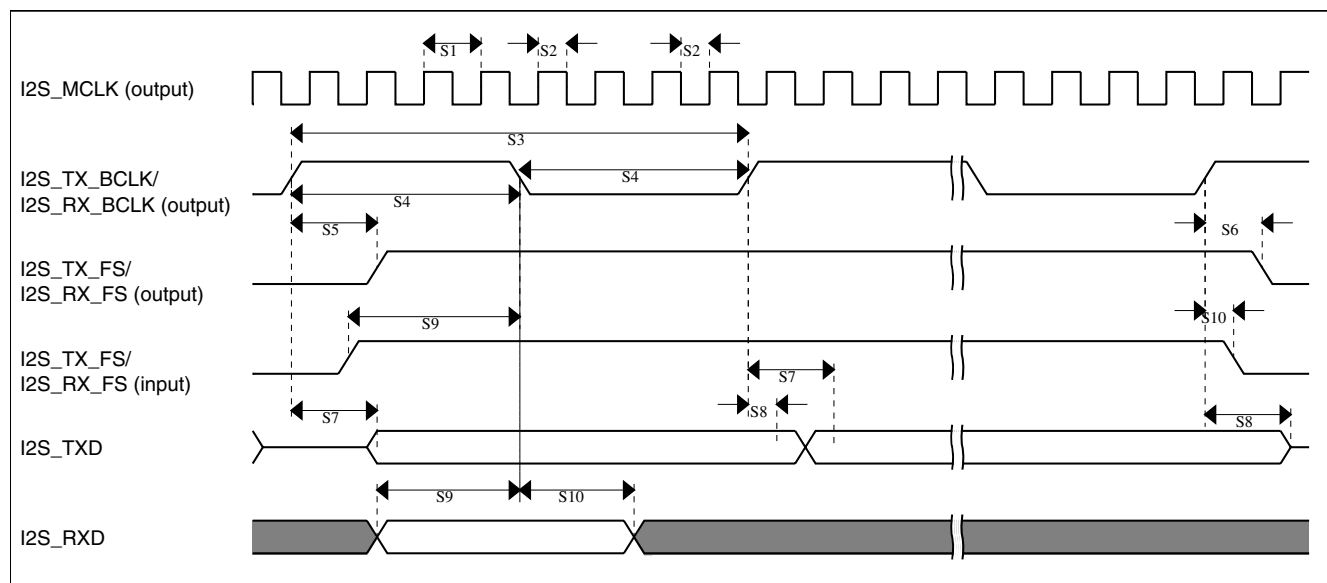


Figure 27. I2S/SAI timing — master modes

Table 49. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid - Multiple SAI Synchronous mode - All other modes	—	24 20.6	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

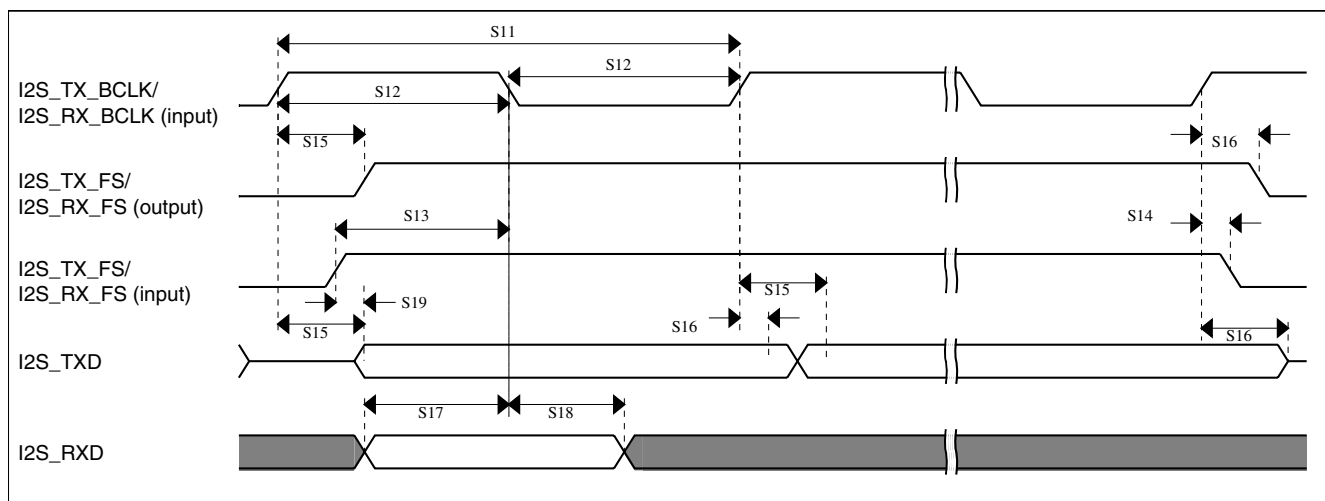


Figure 30. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 52. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f _{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C _{REF}	Internal reference capacitor	—	1	—	pF	
V _{DELTA}	Oscillator delta voltage	—	500	—	mV	2, 5
I _{REF}	Reference oscillator current source base current 2 μA setting (REFCHRG = 0) 32 μA setting (REFCHRG = 15)	—	2	3	μ A	2, 6
I _{ELE}	Electrode oscillator current source base current 2 μA setting (EXTCHRG = 0) 32 μA setting (EXTCHRG = 15)	—	2	3	μ A	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μ s	12
I _{TSI_RUN}	Current added in run mode	—	55	—	μ A	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μ A	13