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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

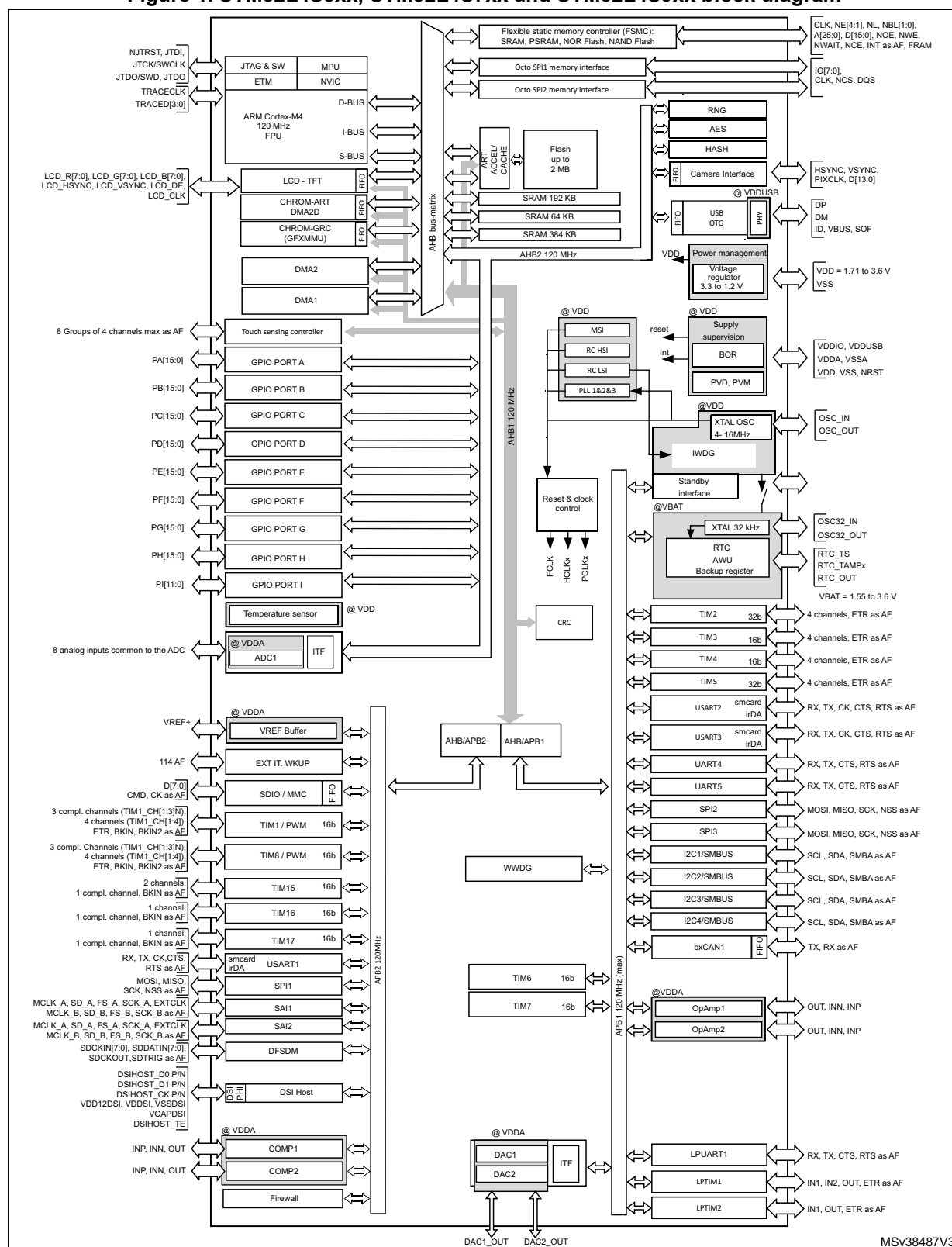
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s5vit6

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Figure 1. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx block diagram



Note: AF: alternate function on I/O pins.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
 - Internal clock sources: LSE, LSI, HSI16 or APB clock
 - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only).

3.32.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.32.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.32.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
98	A2	142	A11	B4	-	142	C4	A11	B4	PE1	I/O	FT	-	DCMI_D3, LCD_VSYNC, FMC_NBL1, TIM17_CH1, EVENTOUT	-
99	D3	143	A12	B3	99	143	A1	A12	B3	VSS	S	-	-	-	-
100	C4	144	B12	A3	100	144	B2	B12	A3	VDD	S	-	-	-	-
-	-	-	-	A2	-	-	-	-	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4 , EVENTOUT	-
-	-	-	-	B2	-	-	-	-	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	B1	-	-	-	-	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2 , CAN1_RX, EVENTOUT	-
-	-	-	-	A1	-	-	-	-	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1 , EVENTOUT	-

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (for example to drive a LED).
- After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
- NC (not-connected) balls must be left unconnected. However, PF8 and PF9 NC' IOs are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
- After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7⁽¹⁾ (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/L PTIM1	TIM1/2/3/4/ 5	SPI2/SAI1/I2C4/U SART2/OTG_FS/T IM1/8/OCTOSPIM _P1	I2C1/2/3/4/DC MI	SPI1/2/3/I2C4/DFS DM1/DCMI/OCTOS PIM_P1/2	SPI3/I2C3/DFS DM1/COMP1/O CTOSPIM_P2	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRAC ESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	DFSDM1_DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_ REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in [Figure 22: Current consumption measurement](#).

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0432 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
 - Voltage Range 1 Boost mode for $80\text{ MHz} < f_{HCLK} \leq 120\text{ MHz}$
 - Voltage Range 1 Normal mode for $26\text{ MHz} < f_{HCLK} \leq 80\text{ MHz}$

The parameters given in [Table 26](#) to [Table 33](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 22: General operating conditions](#).

**Table 30. Current consumption in Run and Low-power run modes,
code with data processing running from SRAM1**

Symbol	Parameter	Conditions		fHCLK	TYP					MAX ⁽¹⁾					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.75	4.85	6.45	9.30	4.70	5.6	7.6	11.0	17.0	mA
				16 MHz	2.20	2.55	3.65	5.20	8.10	3.20	4.1	6.1	9.4	16.0	
				8 MHz	1.20	1.55	2.65	4.25	7.10	1.70	2.7	4.7	8.0	14.0	
				4 MHz	0.74	1.10	2.15	3.75	6.60	1.20	2.0	4.0	7.3	14.0	
				2 MHz	0.49	0.85	1.95	3.50	6.35	0.79	1.6	3.6	6.9	13.0	
				1 MHz	0.37	0.73	1.80	3.40	6.20	0.61	1.4	3.4	6.7	13.0	
				100 KHz	0.26	0.62	1.70	3.25	6.10	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.00	18.50	20.00	22.50	26.50	19.00	21.0	24.0	28.0	36.0 ⁽²⁾	
			Range 1 Normal Mode	80 MHz	11.00	11.50	13.50	15.50	19.00	15.00	16.0	19.0	23.0	30.0 ⁽²⁾	
				72 MHz	10.00	10.50	12.00	14.00	18.00	13.00	15.0	18.0	22.0	29.0	
				64 MHz	9.10	9.60	11.00	13.00	16.50	12.00	13.0	16.0	20.0	27.0	
				48 MHz	7.20	7.70	9.20	11.00	14.50	11.00	12.0	15.0	19.0	26.0	
				32 MHz	4.90	5.40	6.85	8.80	12.50	7.30	8.5	12.0	16.0	23.0	
				24 MHz	3.75	4.25	5.65	7.65	11.00	5.60	6.7	9.3	14.0	21.0	
				16 MHz	2.60	3.10	4.50	6.45	9.90	4.10	5.2	7.7	12.0	19.0	
IDD (LPRun)	Supply current in Low-power run mode	fHCLK = fMSI all peripherals disable FLASH in power-down		2 MHz	435	885	2150	3950	7100	800	1800	4200	7800	15000	µA
				1 MHz	300	745	2000	3800	6950	580	1600	4000	7600	14000	
				400 KHz	225	655	1900	3700	6850	420	1400	3800	7500	14000	
				100 KHz	180	620	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

2. Guaranteed by test in production.

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
IDD (LPRun)	Supply current in Low-power run	fHCLK = fMSI = 2MHz all pripherals disable		Reduced code ⁽¹⁾	490	460	µA	245	230	µA/MHz
				Coremark	520	515		260	258	
				Dhrystone2.1	530	530		265	265	
				Fibonacci	470	495		235	248	
				While ⁽¹⁾	455	515		228	258	

1. Reduced code used for characterization results provided in [Table 26](#), [Table 28](#), [Table 30](#).



Table 41. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX ⁽¹⁾					Unit
		-	V _{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	245	420	1450	3850	10500	-	-	-	-	-	nA
			2.4 V	340	555	1750	4600	12500	-	-	-	-	-	
			3 V	465	730	2250	5900	15500	-	-	-	-	-	
			3.6 V	615	945	2850	7250	19000	-	-	-	-	-	
		RTC clocked by LSE quartz ⁽²⁾ in low drive mode	1.8 V	335	520	1550	4000	-	-	-	-	-	-	
			2.4 V	435	650	1850	4750	-	-	-	-	-	-	
			3 V	560	830	2350	6050	-	-	-	-	-	-	
			3.6 V	730	1050	2950	7400	-	-	-	-	-	-	
IDD(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz ⁽³⁾	3 V	0.5	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.

2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in [Table 44: Low-power mode wakeup timings](#).

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 49](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 49. HSE oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
$I_{DD(HSE)}$	HSE current consumption	During startup ⁽³⁾	-	-	5.5	mA
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF@}8\text{ MHz}$	-	0.44	-	
		$V_{DD} = 3\text{ V}$, $R_m = 45\ \Omega$, $CL = 10\text{ pF@}8\text{ MHz}$	-	0.45	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 5\text{ pF@}48\text{ MHz}$	-	0.68	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF@}48\text{ MHz}$	-	0.94	-	
		$V_{DD} = 3\text{ V}$, $R_m = 30\ \Omega$, $CL = 20\text{ pF@}48\text{ MHz}$	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.

2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 26](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Table 52. MSI oscillator characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta V_{DD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	$V_{DD}=1.62$ V to 3.6 V	-1.2	-	0.5	%
				$V_{DD}=2.4$ V to 3.6 V	-0.5	-		
			Range 4 to 7	$V_{DD}=1.62$ V to 3.6 V	-2.5	-	0.7	
				$V_{DD}=2.4$ V to 3.6 V	-0.8	-		
			Range 8 to 11	$V_{DD}=1.62$ V to 3.6 V	-5	-	1	
				$V_{DD}=2.4$ V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode ⁽³⁾	MSI mode	$T_A= -40$ to 85 °C		-	1	2	%
			$T_A= -40$ to 125 °C		-	2	4	
P_USB Jitter(MSI) ⁽⁶⁾	Period jitter for USB clock ⁽⁴⁾	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI) ⁽⁶⁾	Medium term jitter for USB clock ⁽⁵⁾	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI) ⁽⁶⁾	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI) ⁽⁶⁾	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 76. ADC accuracy - limited test conditions 2⁽¹⁾⁽²⁾⁽³⁾

Sym- bol	Parameter	Conditions ⁽⁴⁾		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	6.5	LSB
			Slow channel (max speed)	-	4	6.5	
		Differential	Fast channel (max speed)	-	3.5	5.5	
			Slow channel (max speed)	-	3.5	5.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	4.5	
			Slow channel (max speed)	-	1	5	
		Differential	Fast channel (max speed)	-	1.5	3	
			Slow channel (max speed)	-	1.5	3	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	6	
			Slow channel (max speed)	-	2.5	6	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	3.5	
			Slow channel (max speed)	-	1.5	3.5	
		Differential	Fast channel (max speed)	-	1	3	
			Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10	10.5	-	bits
			Slow channel (max speed)	10	10.5	-	
		Differential	Fast channel (max speed)	10.7	10.9	-	
			Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	62	65	-	dB
			Slow channel (max speed)	62	65	-	
		Differential	Fast channel (max speed)	66	67.4	-	
			Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	64	66	-	
			Slow channel (max speed)	64	66	-	
		Differential	Fast channel (max speed)	66.5	68	-	
			Slow channel (max speed)	66.5	68	-	

6.3.23 Voltage reference buffer characteristics

Table 81. VREFBUF characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046 ⁽³⁾	2.048	2.049 ⁽³⁾	
			$V_{RS} = 1$	2.498 ⁽³⁾	2.5	2.502 ⁽³⁾	
		Degraded mode ⁽²⁾	$V_{RS} = 0$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
			$V_{RS} = 1$	$V_{DDA} - 150 \text{ mV}$	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	± 0.05	± 0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	μF
esr	Equivalent Serial Resistor of Cloud	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	$2.8 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	$I_{load} = 500 \mu\text{A}$	-	200	1000	ppm/V
			$I_{load} = 4 \text{ mA}$	-	100	500	
I_{load_reg}	Load regulation	$500 \mu\text{A} \leq I_{load} \leq 4 \text{ mA}$	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	$-40^\circ\text{C} < T_J < +125^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	ppm/°C
		$0^\circ\text{C} < T_J < +50^\circ\text{C}$		-	-	$T_{coeff_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	$CL = 0.5 \mu\text{F}^{(4)}$		-	300	350	μs
		$CL = 1.1 \mu\text{F}^{(4)}$		-	500	650	
		$CL = 1.5 \mu\text{F}^{(4)}$		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase ⁽⁵⁾	-	-	-	8	-	mA

Table 82. COMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA}(COMP)$	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ± 100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	μA
			With 50 kHz ± 100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ± 100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	_(4)	nA

1. Guaranteed by design, unless otherwise specified.

2. Refer to [Table 25: Embedded internal voltage reference](#).

3. Guaranteed by characterization results.

4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in [Table 67: I/O static characteristics](#).

6.3.25 Operational amplifiers characteristics

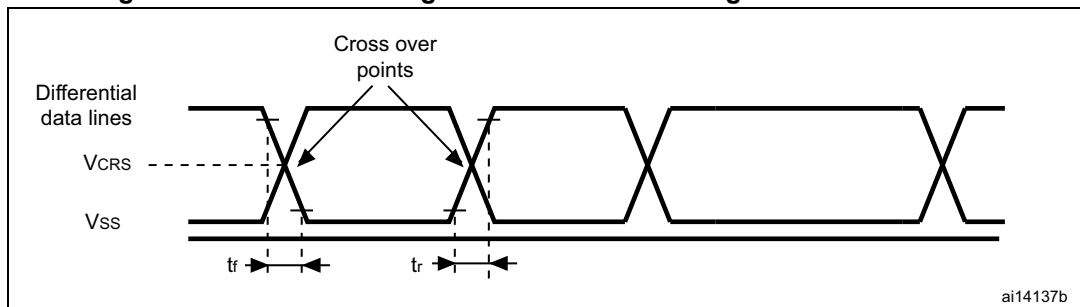
Table 83. OPAMP characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
$V_{I\text{OFFSET}}$	Input offset voltage	25 °C, No Load on output.	-	-	± 1.5	mV
		All voltage/Temp.	-	-	± 3	
$\Delta V_{I\text{OFFSET}}$	Input offset voltage drift	Normal mode	-	± 5	-	$\mu V/^{\circ}C$
		Low-power mode	-	± 10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1 \times V_{DDA}$)	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9 \times V_{DDA}$)	-	-	1	1.35	

Table 83. OPAMP characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	$C_{\text{LOAD}} \leq 50 \text{ pf}$, $R_{\text{LOAD}} \geq 4 \text{ k}\Omega$ follower configuration	-	5	10	μs
		Low-power mode	$C_{\text{LOAD}} \leq 50 \text{ pf}$, $R_{\text{LOAD}} \geq 20 \text{ k}\Omega$ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132 and UFBGA169 only)		-	-	(3)	nA
		Dedicated input (UFBGA132 and UFBGA169 only)	$T_J \leq 75 \text{ }^\circ\text{C}$	-	-	1	
			$T_J \leq 85 \text{ }^\circ\text{C}$	-	-	3	
			$T_J \leq 105 \text{ }^\circ\text{C}$	-	-	8	
			$T_J \leq 125 \text{ }^\circ\text{C}$	-	-	15	
PGA gain ⁽²⁾	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
R_{network}	R2/R1 internal resistance values in PGA mode ⁽⁴⁾	PGA Gain = 2		-	80/80	-	k Ω /k Ω
		PGA Gain = 4		-	120/40	-	
		PGA Gain = 8		-	140/20	-	
		PGA Gain = 16		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/2	-	MHz
		Gain = 4	-	-	GBW/4	-	
		Gain = 8	-	-	GBW/8	-	
		Gain = 16	-	-	GBW/16	-	

Figure 44. USB OTG timings – definition of data signal rise and fall time

Table 95. USB OTG electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_{rLS}	Rise time in LS ⁽²⁾	$C_L = 200 \text{ to } 600 \text{ pF}$	75	300	ns
t_{fLS}	Fall time in LS ⁽²⁾				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	80	125	%
t_{rFS}	Rise time in FS ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_{fFS}	Fall time in FS ⁽²⁾	$C_L = 50 \text{ pF}$			
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 96. USB BCD DC electrical characteristics⁽¹⁾

Driver characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	μA
	Secondary detection mode consumption	-	-	-		
RDAT_LKG	Data line leakage resistance	-	300	-	-	k Ω
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V

Figure 57. OctoSPI timing diagram - SDR mode

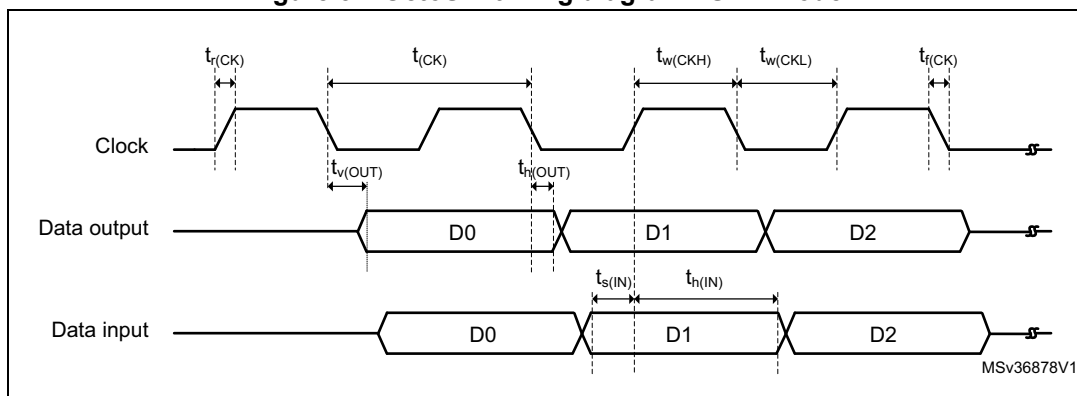


Figure 58. OctoSPI timing diagram - DDR mode

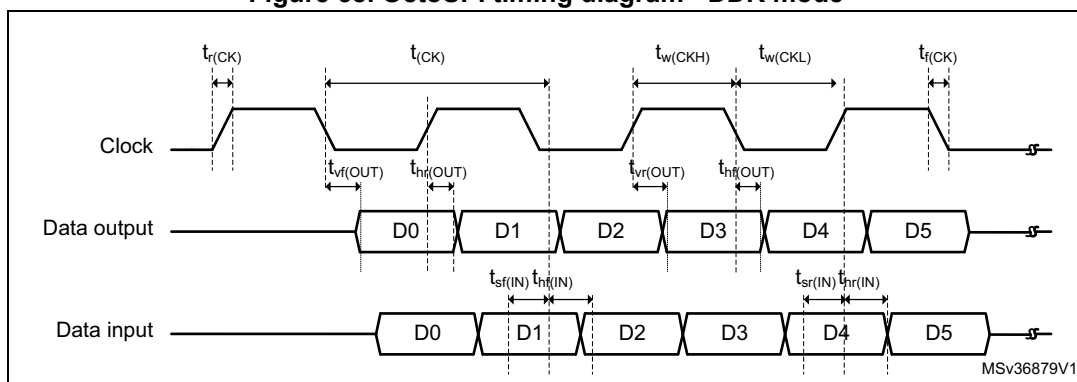
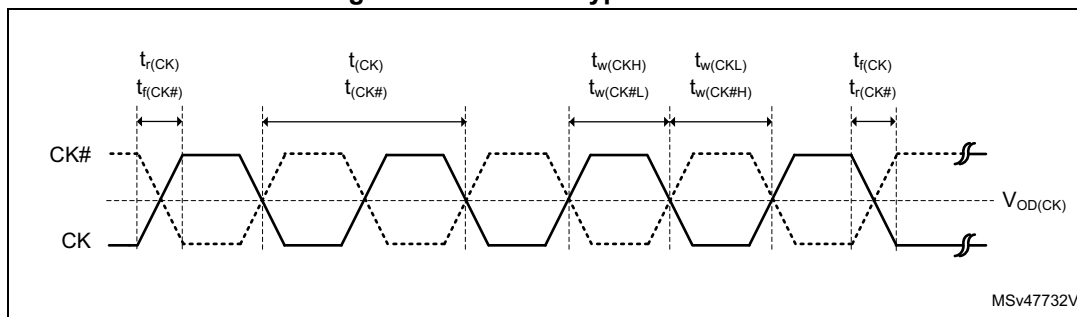
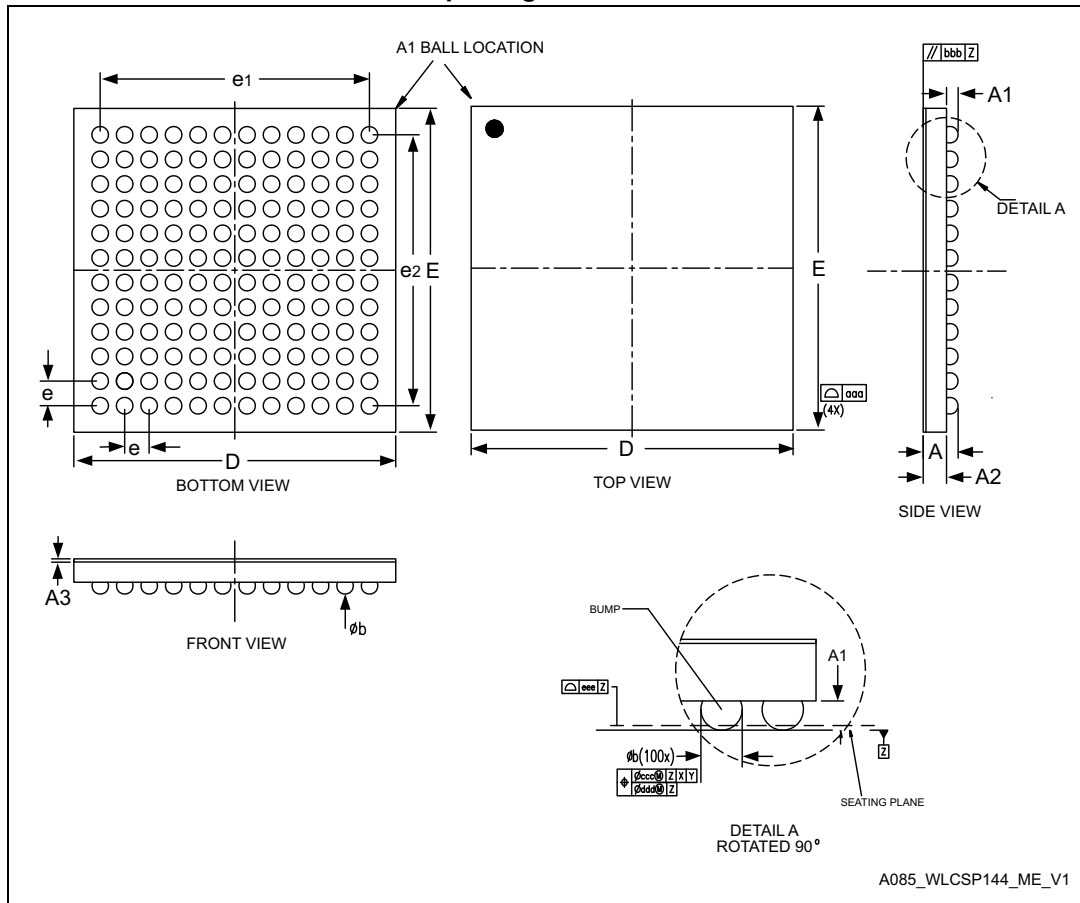


Figure 59. OctoSPI Hyperbus clock



7.4 WLCSP144 package information

Figure 76. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, package outline



1. Drawing is not to scale.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 128. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA144 -10 x 10 mm	53	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7 mm	52	
	Thermal resistance junction-ambient WLCSP144	30.1	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L4Sxxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

9 Revision history

Table 130. Document revision history

Date	Revision	Changes
10-Oct-2017	1	Initial release.
28-Nov-2017	2	Added: – Section 6.3.10: MIPI D-PHY characteristics – Section 6.3.11: MIPI D-PHY PLL characteristics – Section 6.3.12: MIPI D-PHY regulator characteristics Updated: – Cover page Features (Performance benchmark and Energy benchmark) – Table 4: STM32L4S5xx modes overview – Section 3.12: Clocks and startup – Figure 14: STM32L4S5xx WLCSP144 ballout⁽¹⁾ – Table 15: STM32L4Sxxx pin definitions
30-Apr-2018	3	Added: – Figure 5: Power-up/down sequence – Figure 61: OctoSPI Hyperbus read with double latency Updated: – Section 1: Introduction – Section 3.10.1: Power supply schemes – Table 8: Temperature sensor calibration values – Parameter column on Table 34: Current consumption in Sleep and Low-power sleep mode, Flash ON – Title of Table 35: Current consumption in Low-power sleep mode, Flash in power-down