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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s7aii6

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM3 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
HASH hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off. In Stop 2 mode, the content of SRAM3 is preserved or not depending on the RRSTP bit in PWR_CR1 register.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
66	D12	99	D2	G9	68	101	C12	D2	G13	PC9	I/O	FT_fl	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-
67	D11	100	D3	G8	69	102	D11	D3	E11	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, OTG_FS_SOF, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
68	D10	101	D4	F10	70	103	D10	D4	E12	PA9	I/O	FT_flu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
69	C12	102	D5	F9	71	104	C10	D5	D11	PA10	I/O	FT_flu	-	TIM1_CH3, SAI1_D1, DCMI_D1, USART1_RX, OTG_FS_ID, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
70	B12	103	C1	E13	72	105	B12	C1	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
71	A12	104	C2	D13	73	106	B11	C2	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
78	B11	111	C3	D9	80	113	C9	C3	D9	PC10	I/O	FT	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, DCMI_D8, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
79	C10	112	C4	E9	81	114	A9	C4	E9	PC11	I/O	FT	-	DCMI_D2, OCTOSPIM_P1_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
80	B10	113	B4	F8	82	115	D9	B4	F8	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
81	C9	114	A4	B8	83	116	C8	A4	B8	PD0	I/O	FT	-	SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, LCD_B4, FMC_D2, EVENTOUT	-
82	B9	115	C5	C8	84	117	B8	C5	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, LCD_B5, FMC_D3, EVENTOUT	-
83	C8	116	B5	D8	85	118	D8	B5	D8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, SDMMC1_CMD, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	D8	125	B7	D6	-	127	E6	B7	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	G3	126	-	E6	-	128	-	-	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS_NSS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	D7	127	A7	F6	-	129	D6	A7	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, OCTOSPIM_P2_NCS, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	C7	128	D8	G7	-	-	C6	D8	G6	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, LCD_R0, FMC_A24, EVENTOUT	-
-	C6	129	-	G6	-	-	-	-	-	PG14	I/O	FT_fs	-	I2C1_SCL, LCD_R1, FMC_A25, EVENTOUT	-
-	F7	130	-	-	-	130	A7	-	-	VSS	S	-	-	-	-
-	G7	131	A8	B6	-	131	A6	A8	B6	VDDIO2	S	-	-	-	-
-	K1	132	-	C6	-	132	-	-	C6	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, OCTOSPIM_P2_DQS, DCMI_D13, EVENTOUT	-
89	A8	133	B8	A6	91	133	B6	B8	A6	PB3 (JTDO/TRACESWO)	I/O	FT_la	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, OTG_FS_CRS_SYNC, SAI1_SCK_B, EVENTOUT	COMP2_INM

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPIM_P1_CLK	-	-	DFSDM1_CKOUT	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port B	PB0	-	-	OCTOSPIM_P1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_ RTS_DE	-	OCTOSPIM_P1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPIM_P1_DQS	LCD_B1	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRS_SYNC	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_ DE	TSC_G2_IO1	DCMI_D12	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	DCMI_D5	-	TIM8_BKIN2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC	DSI_TE	FMC_NL	TIM8_BKIN	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_ CKIN	CAN1_RX	DCMI_D6	LCD_B1	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_ CDIR	CAN1_TX	DCMI_D7	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPIM_P1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPIM_P1_NCS	DSI_TE	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RT S_DE	TSC_G1_IO1	-	-	-	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CT S	TSC_G1_IO2	-	-	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	-	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6(4)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		UFBGA169	-	-	385	
		UFBGA132	-	-	364	
		WLCSP144	-	-	664	
P_D	Power dissipation at T_A = 125 °C for suffix 3(4)	LQFP144	-	-	156	mW
		LQFP100	-	-	119	
		UFBGA169	-	-	96	
		UFBGA132	-	-	91	
		WLCSP144	-	-	831	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(5)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

Table 39. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	290	735	2050	3800	6950	560	1600	4500	8700	16000	µA
			2.4 V	295	735	2050	3850	6950	560	1600	4500	8700	17000	
			3 V	295	735	2050	3850	7000	570	1600	4500	8800	17000	
			3.6 V	295	740	2050	3850	7000	570	1600	4500	8800	17000 (2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 40. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	125	380	1900	5200	13500	340	1100	5300	15000	41000	nA
			2.4 V	135	440	2200	6050	15500	350	1300	6100	18000	47000	
			3 V	150	535	2700	7500	19500	370	1500	7100	21000	54000	
			3.6 V	190	665	3200	8850	23000	400	1900	8400	24000	62000	
		With independent watchdog	1.8 V	295	-	-	-	-	-	-	-	-	-	
			2.4 V	355	-	-	-	-	-	-	-	-	-	
			3 V	420	-	-	-	-	-	-	-	-	-	
			3.6 V	510	-	-	-	-	-	-	-	-	-	

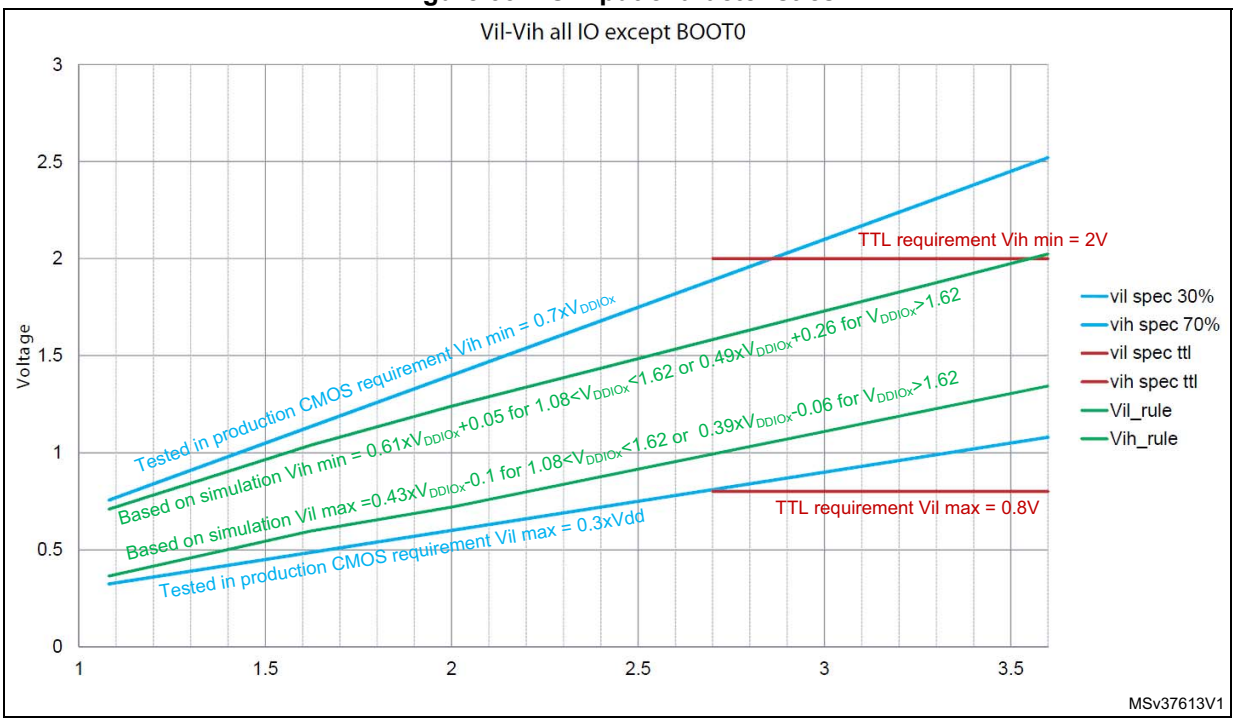
Table 67. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u, PB2 and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 33: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. Max(V_{DDXXX}) is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table*.
5. All TX_xx IO except FT_lu, FT_u, PB2 and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:
   $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 83: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 33* for standard I/Os, and in *Figure 33* for 5 V tolerant I/Os.

Figure 33. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

Table 75. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 78. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 88. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	8.33	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 120 MHz	0	60	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	0.00833	546.13	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	-	35.77	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 89. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 90. WWDG min/max timeout value at 120 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0341	2.1845	ms
2	1	0.0683	4.3691	
4	2	0.1356	8.7381	
8	3	0.2731	17.4763	

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 115. LTDC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK} D_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V	-	83	MHz
		1.71 V < V_{DD} < 3.6 V	-	50	
	LTDC clock output duty cycle	-	45	55	%
tw(CLKH) tw(CLKL)	Clock high time Clock low time	-	tw(CLK)/2-0.5	tw(CLK)/2+0.5	-
t_v(DATA)	Data output valid time	-	-	6	
t_h(DATA)	Data output hold time	-	0	-	
t_v(HSYNC) t_v(VSYNC) t_v(DE)	HSYNC/VSYNC/DE output valid time	-	-	3	
t_h(HSYNC) t_h(VSYNC) t_h(DE)	HSYNC/VSYNC/DE output hold time	-	0	-	

1. Guaranteed by characterization results.

6.3.35 SD/SDIO/MMC card host interfaces (SDMMC)

Unless otherwise specified, the parameters given in Table xx for SDIO are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 22: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD} Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 116. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1)

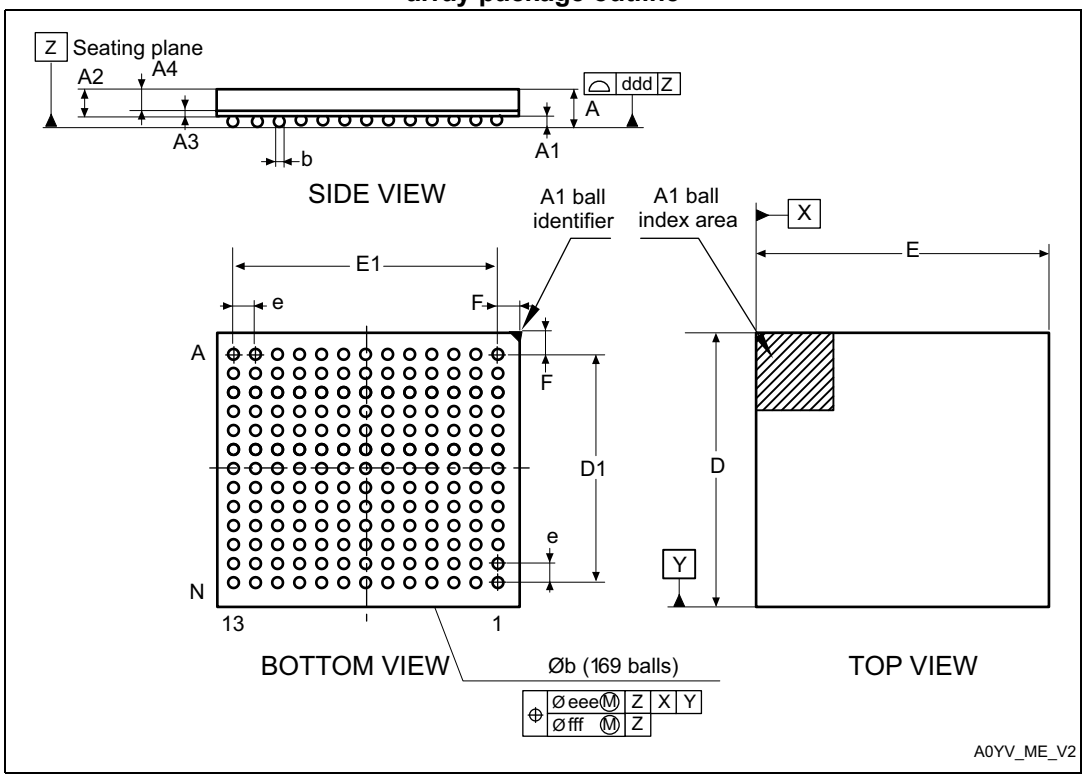
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	66	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA169 package information

Figure 67. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 118. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

Table 118. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 68. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

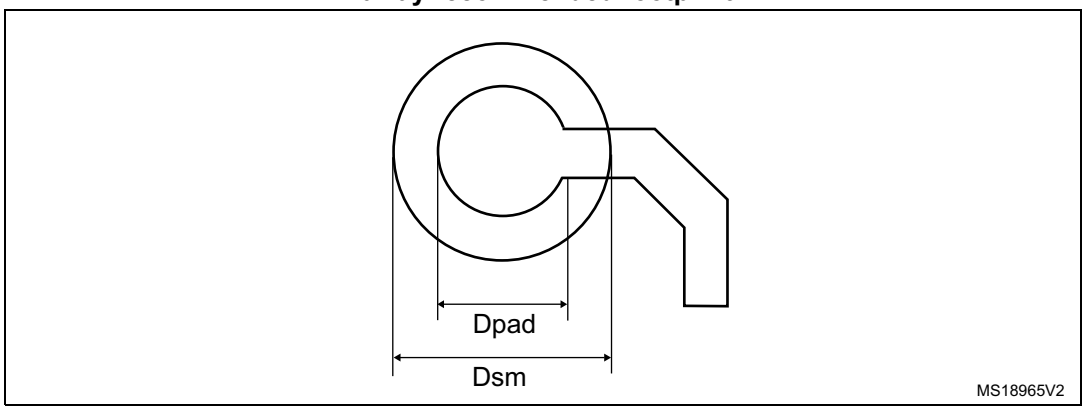


Table 119. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

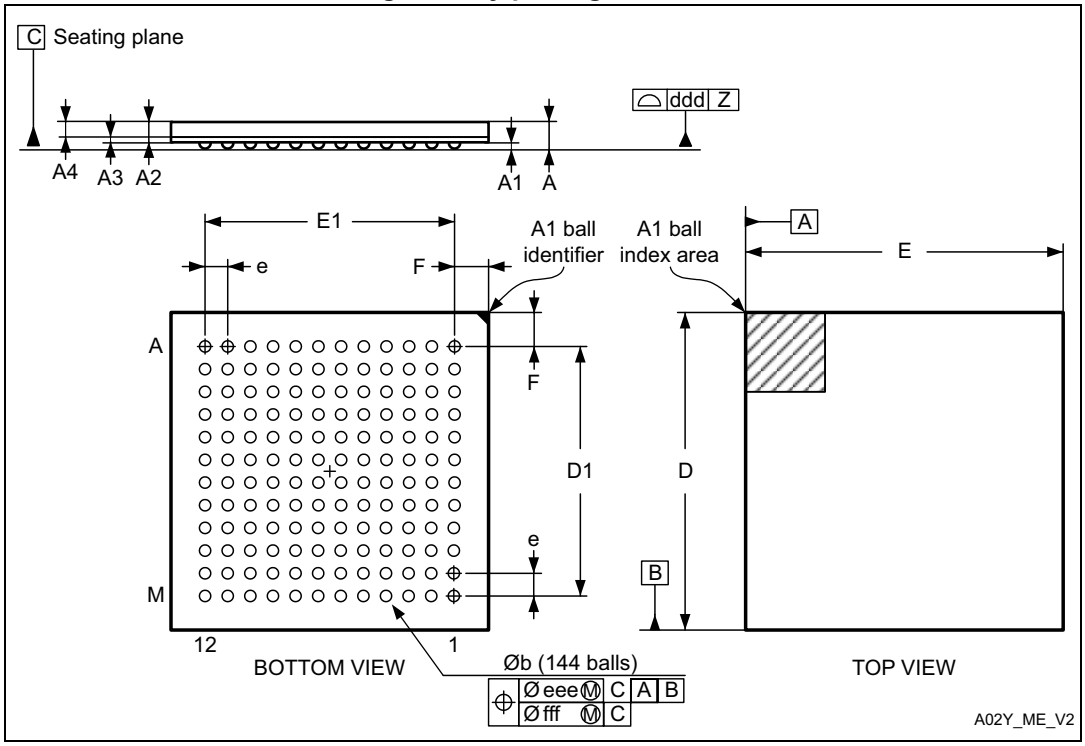
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

7.2 UFBGA144 package information

Figure 70. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 120. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data

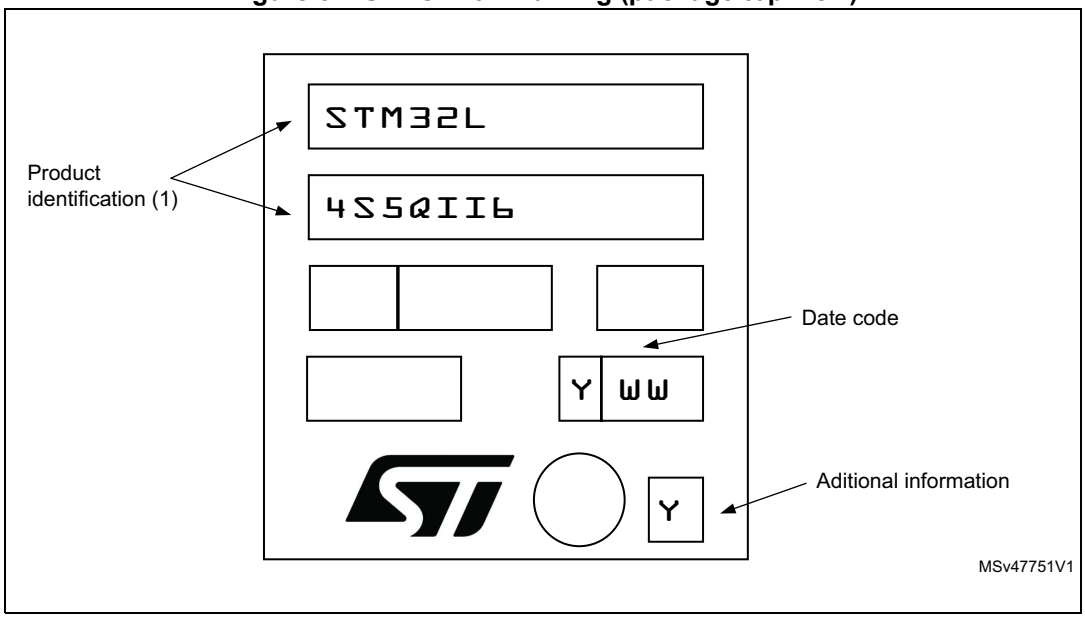
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.360	0.400	0.440	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.2736	0.2756	0.2776
D1	8.750	8.800	8.850	0.2343	0.2362	0.2382
E	9.950	10.000	10.050	0.2736	0.2756	0.2776
E1	8.750	8.800	8.850	0.2343	0.2362	0.2382
e	0.750	0.800	0.850	-	0.0197	-
F	0.550	0.600	0.650	0.0177	0.0197	0.0217

UFBGA132 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 81. UFBGA132 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 128. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14mm	42	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA144 -10 x 10 mm	53	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7 mm	52	
	Thermal resistance junction-ambient WLCSP144	30.1	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L4Sxxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.