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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s7vit6

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts (continued)

Peripheral	S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
LCD - TFT	No	Yes		No		Yes		No	Yes	
MIPI DSI Host(2)	No		Yes	No			Yes	No		Yes
Random number generator	Yes									
AES + HASH	Yes									
GPIOs Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1									
	16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage	1.71 to 3.6 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA 132	LQFP 144 WLCSP144	LQFP 144	LQFP 144, UFBGA 144 WLCSP 144	UFBGA169		
Bootloader	USART 1	USART 2	USART 3	SPI1	SPI2	I2C1	I2C2	I2C3	CAN1	USB through DFU

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4S9xx sales types.

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xxdevices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 95 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 36 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.21 Voltage reference buffer (VREFBUF)

The STM32L4Sxxx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

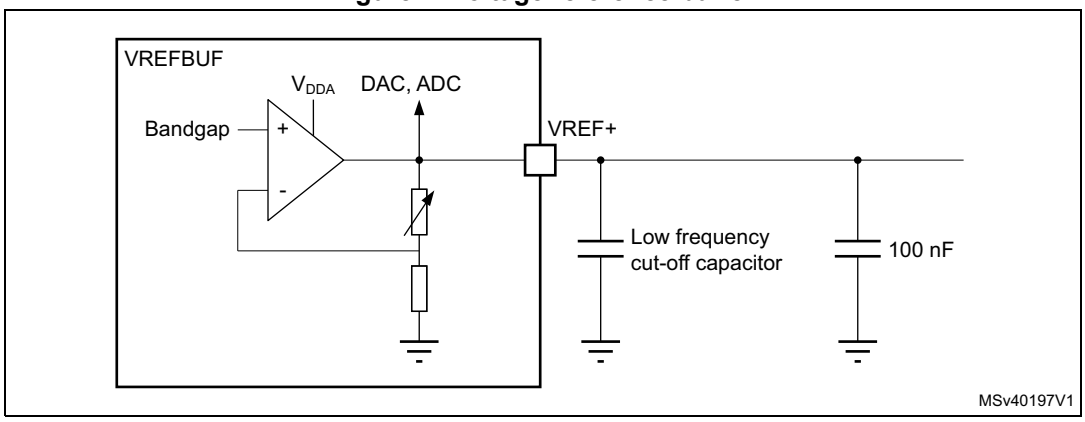
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 7. Voltage reference buffer



3.22 Comparators (COMP)

The STM32L4Sxxx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.23 Operational amplifier (OPAMP)

The STM32L4Sxxx devices embed two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.24 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.25 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- Two displays layers with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

3.26 DSI Host (DSIHOST)

The DSI Host is a dedicated IP that interfaces with the MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

The interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI)
  - Used to transmit information in full bandwidth in the Adapted Command Mode (DBI) through a custom mode
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli

3.33 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (alarm, wake-up timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.34 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to *Table 11: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
33	K5	44	L9	H5	31	41	L5	L9	K4	PC4	I/O	FT_a	-	USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM, ADC1_IN13
34	L5	45	K8	J5	-	-	K5	K8	-	PC5	I/O	FT_a	-	SAI1_D3, USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
35	M5	46	M9	K5	32	42	M5	M9	N4	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN15
36	M6	47	H7	L5	33	43	J5	H7	L5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, OCTOSPIM_P1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
37	L6	48	J7	N5	34	44	H5	J7	N5	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPIM_P1_DQS, LCD_B1, EVENTOUT	COMP1_INP
-	K6	49	K7	M5	-	45	K6	K7	M5	PF11	I/O	FT	-	LCD_DE, DCMI_D12, DSI_TE, EVENTOUT	-
-	J7	50	L8	N6	-	46	G5	L8	N6	PF12	I/O	FT	-	OCTOSPIM_P2_DQS, LCD_B0, FMC_A6, EVENTOUT	-
-	-	51	M8	-	-	47	M1	M8	-	VSS	S	-	-	-	-
-	-	52	L7	N7	-	48	M6	L7	N7	VDD	S	-	-	-	-
-	K7	53	M7	M6	-	49	J6	M7	M6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, LCD_B1, FMC_A7, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
98	A2	142	A11	B4	-	142	C4	A11	B4	PE1	I/O	FT	-	DCMI_D3, LCD_VSYNC, FMC_NBL1, TIM17_CH1, EVENTOUT	-
99	D3	143	A12	B3	99	143	A1	A12	B3	VSS	S	-	-	-	-
100	C4	144	B12	A3	100	144	B2	B12	A3	VDD	S	-	-	-	-
-	-	-	-	A2	-	-	-	-	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	B2	-	-	-	-	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	B1	-	-	-	-	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT	-
-	-	-	-	A1	-	-	-	-	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, PF8 and PF9 NC' IOs are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_P1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_P2_DQS	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_P1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_P2_NCS	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	OCTOSPIM_P2_DQS	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	OCTOSPIM_P2_NCS	-	-
	PI9	-	-	-	-	-	OCTOSPIM_P2_IO2	-	-
	PI10	-	-	-	-	-	OCTOSPIM_P2_IO1	-	-
	PI11	-	-	-	-	-	OCTOSPIM_P2_IO0	-	-

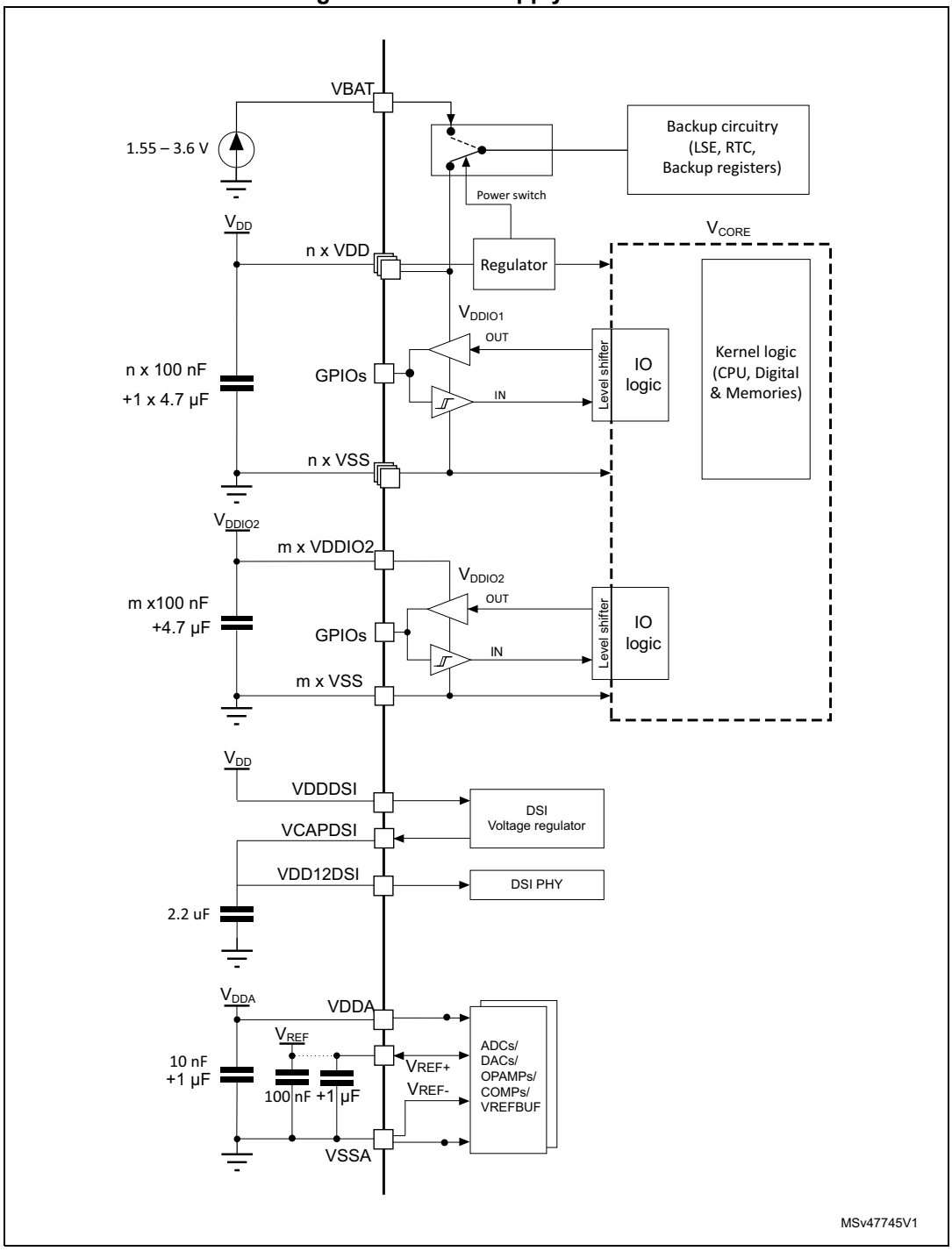
1. Refer to *Table 17* for AF8 to AF15.

Table 18. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
AHB1	0x4002 F000 - 0x47FF FFFF	~127 MB	Reserved
	0x4002 C000 - 0x4002 EFFF	12 KB	GFXMMU
	0x4002 BC00 - 0x4002 BFFF	1 KB	Reserved
	0x4002 B000 - 0x4002 BBFF	3 KB	DMA2D
	0x4002 4400 - 0x4002 AFFF	26 KB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0800 - 0x4002 0BFF	1 KB	DMAMUX1
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
APB2	0x4001 7400 - 0x4001 FFFF	33 KB	Reserved
	0x4001 6C00 - 0x4001 73FF	1 KB	DSIHOST
	0x4001 6800 - 0x4001 6BFF	1 KB	LCD-TFT
	0x4001 6000 - 0x4001 67FF	2 KB	DFSDM1
	0x4001 5C00 - 0x4001 5FFF	1 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	SAI2
	0x4001 5400 - 0x4001 57FF	1 KB	SAI1
	0x4001 4C00 - 0x4001 53FF	2 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2000 - 0x4001 2BFF	3 KB	Reserved

6.1.6 Power supply scheme

Figure 21. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	4.00	4.10	mA	154	158	µA/MHz
				Coremark	4.15	3.80		160	146	
				Dhrystone2.1	4.40	4.00		169	154	
				Fibonacci	3.80	3.60		146	138	
				While(1)	3.15	3.15		121.2	121.2	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	13.0	13.0	mA	163	163	µA/MHz
				Coremark	13.0	12.0		163	150	
				Dhrystone2.1	14.0	12.5		175	156	
				Fibonacci	11.5	11.0		144	138	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	18.0	16.0		150	133	
				Dhrystone2.1	19.0	16.5		158	138	
				Fibonacci	16.0	15.0		133	125	
				While(1)	16.5	16.5		138	138	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	595	590	µA	298	295	µA/MHz
				Coremark	620	580		310	290	
				Dhrystone2.1	645	655		323	328	
				Fibonacci	670	580		335	290	
				While(1)	470	685		235	343	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 33. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	3.35	mA	129	µA/MHz
				Coremark	3.10		119	
				Dhrystone2.1	3.65		140	
				Fibonacci	3.20		123	
				While(1)	2.85		110	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.0	mA	138	µA/MHz
				Coremark	10.5		131	
				Dhrystone2.1	12.5		156	
				Fibonacci	10.5		131	
				While(1)	9.40		118	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.0	mA	150	µA/MHz
				Coremark	16.5		138	
				Dhrystone2.1	19.5		163	
				Fibonacci	17.5		146	
				While(1)	15.0		125	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	435	µA	218	µA/MHz
				Coremark	395		198	
				Dhrystone2.1	470		235	
				Fibonacci	425		213	
				While(1)	455		228	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

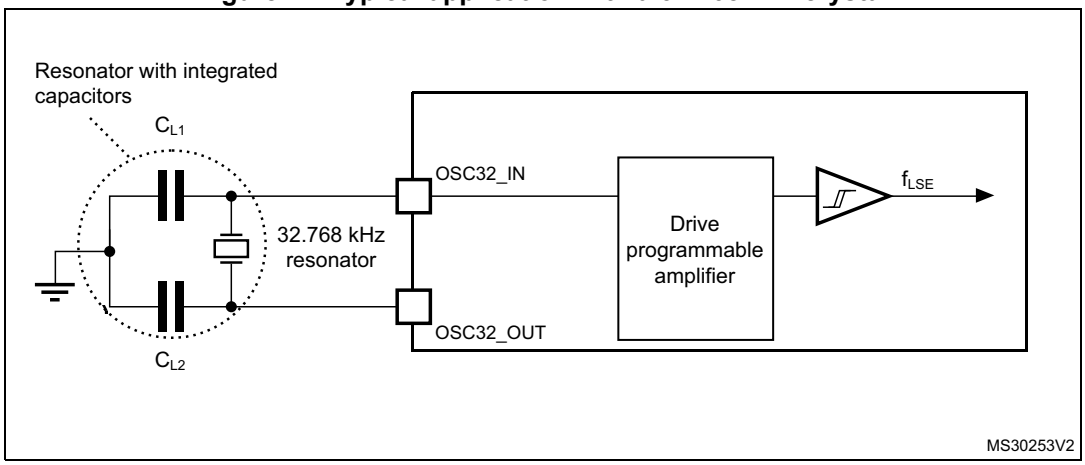
Table 50. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 27. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.21 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 73* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 73. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

The maximum value of R_{AIN} can be found in *Table 74: Maximum ADC RAIN*.

Table 74. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

Table 93. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	13	
		1.08 V ≤ V_{DD} ≤ 1.32 V	-	9	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2.5	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	6.5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	25	
		Slave transmitter (after enable edge) 1.08 V < V_{DD} <1.32 V	-	50	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns

Table 120. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 71. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package recommended footprint

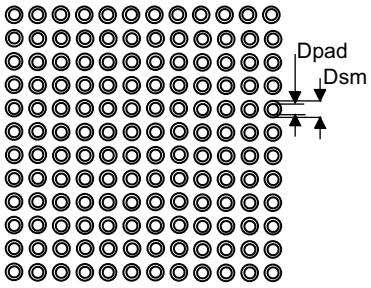


Table 121. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

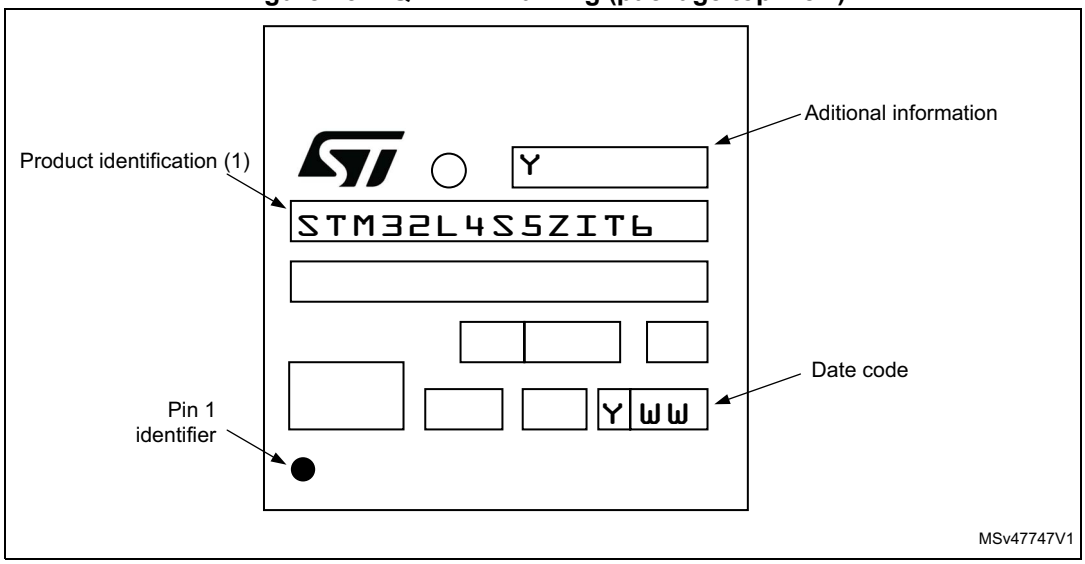
Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

LQFP144 device marking

The following figures gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 75. LQFP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.