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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	131
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s9aii6

- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Hyperbus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.45 OctoSPI IO manager (OctoSPIIOM)

The OctoSPI IO Manager is a low level interface allowing:

- Efficient OctoSPI pin assignment with a full IO Matrix (before alternate function map)
- Multiplexing single/dual/quad/octal SPI interface over the same bus

The OctoSPI IO Manager has the following features:

- Support up to two single/dual/quad/octal SPI Interface
- Support up to eight ports for pin assignment
- Fully programmable IO matrix for pin assignment by function (data/control/clock)
- Muxer for Single/Dual/Quad/Octal SPI interface multiplexing over the same bus

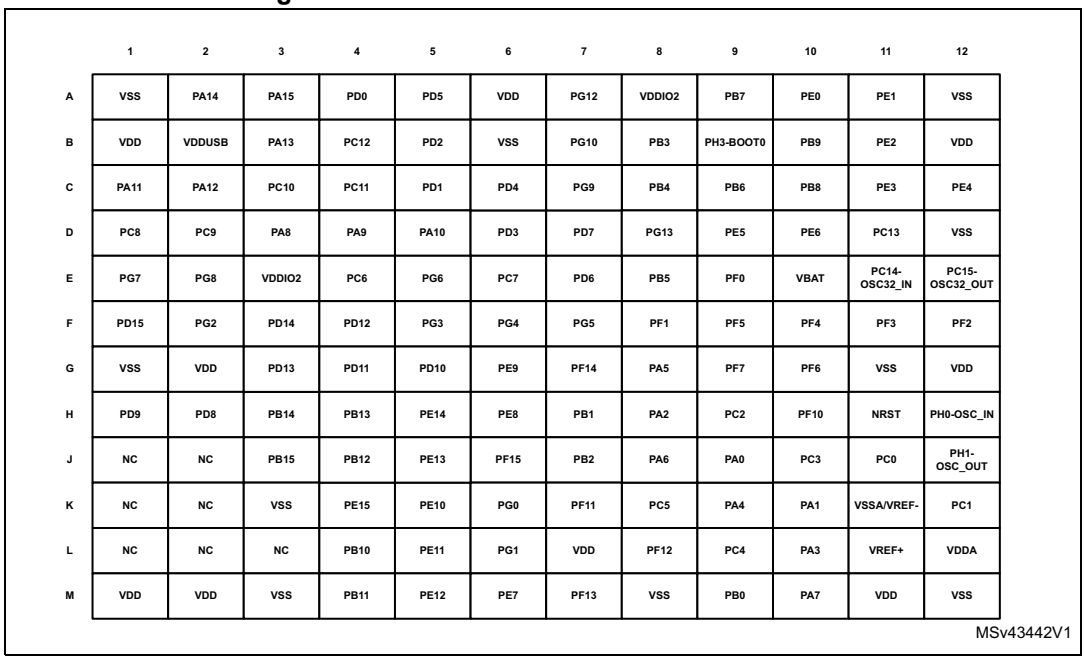
3.46 Development support

3.46.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 14. STM32L4S5xx WLCSP144 ballout(1)

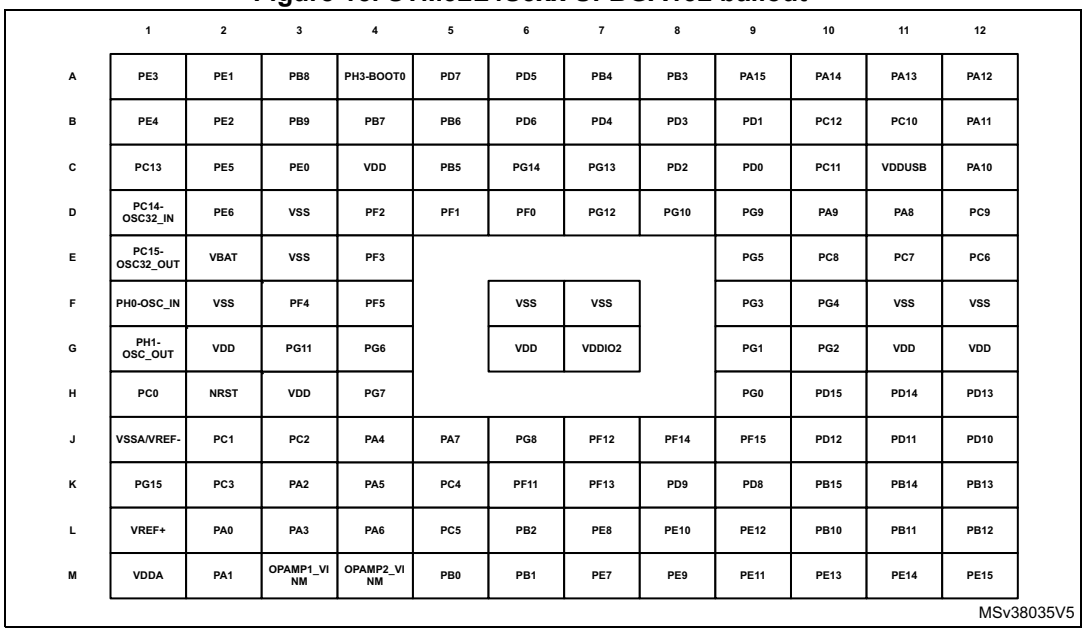


	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	NC	NC	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	NC	NC	VSS	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	NC	NC	NC	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv43442V1

1. The above figure shows the package top view.
   NC (not-connected) balls must be left unconnected.

Figure 15. STM32L4S5xx UFBGA132 ballout(1)



	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv38035V5

1. The above figure shows the package top view.

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
66	D12	99	D2	G9	68	101	C12	D2	G13	PC9	I/O	FT_fl	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-
67	D11	100	D3	G8	69	102	D11	D3	E11	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, OTG_FS_SOF, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
68	D10	101	D4	F10	70	103	D10	D4	E12	PA9	I/O	FT_flu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
69	C12	102	D5	F9	71	104	C10	D5	D11	PA10	I/O	FT_flu	-	TIM1_CH3, SAI1_D1, DCMI_D1, USART1_RX, OTG_FS_ID, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
70	B12	103	C1	E13	72	105	B12	C1	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
71	A12	104	C2	D13	73	106	B11	C2	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	D8	125	B7	D6	-	127	E6	B7	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	G3	126	-	E6	-	128	-	-	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS_NSS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	D7	127	A7	F6	-	129	D6	A7	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, OCTOSPIM_P2_NCS, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	C7	128	D8	G7	-	-	C6	D8	G6	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, LCD_R0, FMC_A24, EVENTOUT	-
-	C6	129	-	G6	-	-	-	-	-	PG14	I/O	FT_fs	-	I2C1_SCL, LCD_R1, FMC_A25, EVENTOUT	-
-	F7	130	-	-	-	130	A7	-	-	VSS	S	-	-	-	-
-	G7	131	A8	B6	-	131	A6	A8	B6	VDDIO2	S	-	-	-	-
-	K1	132	-	C6	-	132	-	-	C6	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, OCTOSPIM_P2_DQS, DCMI_D13, EVENTOUT	-
89	A8	133	B8	A6	91	133	B6	B8	A6	PB3 (JTDO/TRACESWO)	I/O	FT_la	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, OTG_FS_CRS_SYNC, SAI1_SCK_B, EVENTOUT	COMP2_INM

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	OCTOSPIM_P2_NCS	-	-
	PI9	-	-	-	-	-	OCTOSPIM_P2_IO2	-	-
	PI10	-	-	-	-	-	OCTOSPIM_P2_IO1	-	-
	PI11	-	-	-	-	-	OCTOSPIM_P2_IO0	-	-

1. Refer to *Table 17* for AF8 to AF15.

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF)

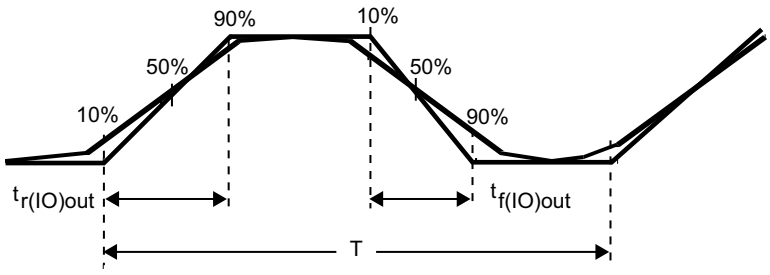
Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.40	3.80	4.90	6.55	9.45	3.9	4.8	6.8	11.0	17.0	mA
				16 MHz	2.20	2.55	3.70	5.30	8.20	2.6	3.4	5.4	8.7	15.0	
				8 MHz	1.25	1.60	2.70	4.30	7.20	1.6	2.3	4.3	7.6	14.0	
				4 MHz	0.740	1.10	2.20	3.80	6.70	1.0	1.8	3.8	7.1	13.0	
				2 MHz	0.495	0.860	1.95	3.55	6.45	0.7	1.5	3.5	6.8	13.0	
				1 MHz	0.370	0.740	1.85	3.45	6.35	0.6	1.4	3.4	6.6	13.0	
				100 KHz	0.265	0.630	1.75	3.35	6.25	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.5	19.5	21.0	23.0	27.0	21.0	23.0	26.0	30.0	38.0	
			Range 1 Normal Mode	80 MHz	11.5	12.0	13.5	15.5	19.0	13.0	14.0	17.0	21.0	28.0	
				72 MHz	10.5	11.0	12.5	14.5	18.0	12.0	13.0	16.0	20.0	27.0	
				64 MHz	9.25	9.75	11.0	13.5	17.0	11.0	12.0	14.0	18.0	26.0	
				48 MHz	7.35	7.85	9.30	11.5	15.0	8.3	9.3	12.0	16.0	23.0	
				32 MHz	5.00	5.50	6.95	8.95	12.5	5.7	6.7	9.2	14.0	21.0	
				24 MHz	3.85	4.35	5.75	7.75	11.5	4.4	5.4	7.9	12.0	19.0	
				16 MHz	2.65	3.15	4.55	6.55	10.0	3.1	4.1	6.6	11.0	18.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	490	910	2200	4050	7250	690	1600	4000	7700	14000	µA
				1 MHz	305	770	2050	3900	7100	490	1500	3900	7500	14000	
				400 KHz	250	695	2000	3800	7000	430	1400	3800	7500	14000	
				100 KHz	210	645	1950	3750	7000	380	1400	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 43. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	USART2 independent clock domain	5.35	5	4.15	4.5	µA/MHz
	USART2 APB clock domain	3	2.75	2.5	2.5	
	USART3 independent clock domain	6.35	6	5	5.5	
	USART3 APB clock domain	2.6	2.4	2.1	2.5	
	UART4 independent clock domain	5.15	4.9	3.75	4.5	
	UART4 APB clock domain	2.5	2.25	2.1	2.5	
	UART5 independent clock domain	5.4	5	4.15	5	
	UART5 APB clock domain	2.4	2.25	2.1	2	
	WWDG	0.75	0.625	0.835	0.5	
	All APB1 on	110	100	84	97	
APB2	AHB to APB2 bridge	0.185	0.15	0.125	0.5	µA/MHz
	DFSDM	9.5	9	7.5	8.5	
	DSI independent clock domain	33	34.5	29.5	NA	
	DSI APB clock domain	13	7.15	29	NA	
	FW	0.665	0.625	0.5	0.5	
	LTDC independent clock domain	35.5	34.5	40	NA	
	LTDC APB clock domain	18	17	14	NA	
	SAI1 independent clock domain	3.1	2.9	2.5	3	
	SAI1 APB clock domain	2.6	2.4	1.9	2	
	SAI2 independent clock domain	3.15	3	2.55	3	
	SAI2 APB clock domain	2.6	2.4	1.9	2.5	
	SPI1	2.25	2.15	1.75	1	
	SYSCFG/VREFBUF/COMP	0.565	0.6	0.5	0.5	

Figure 34. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 69: I/O AC characteristics*.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

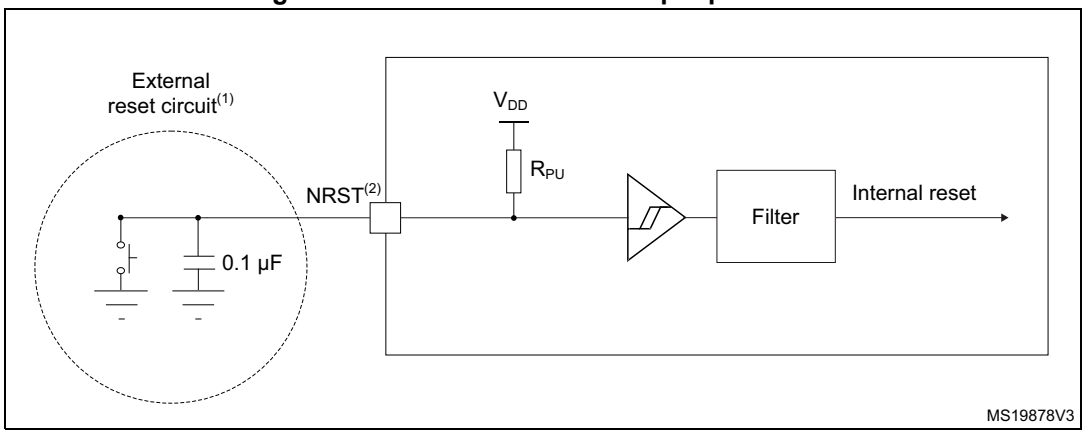
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 70. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 35. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 70: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 71. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.20 Analog switches booster

Table 72. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

Table 73. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
   Refer to *Section 4: Pinouts and pin description* for further details.

Table 76. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 80. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 80. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

Figure 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

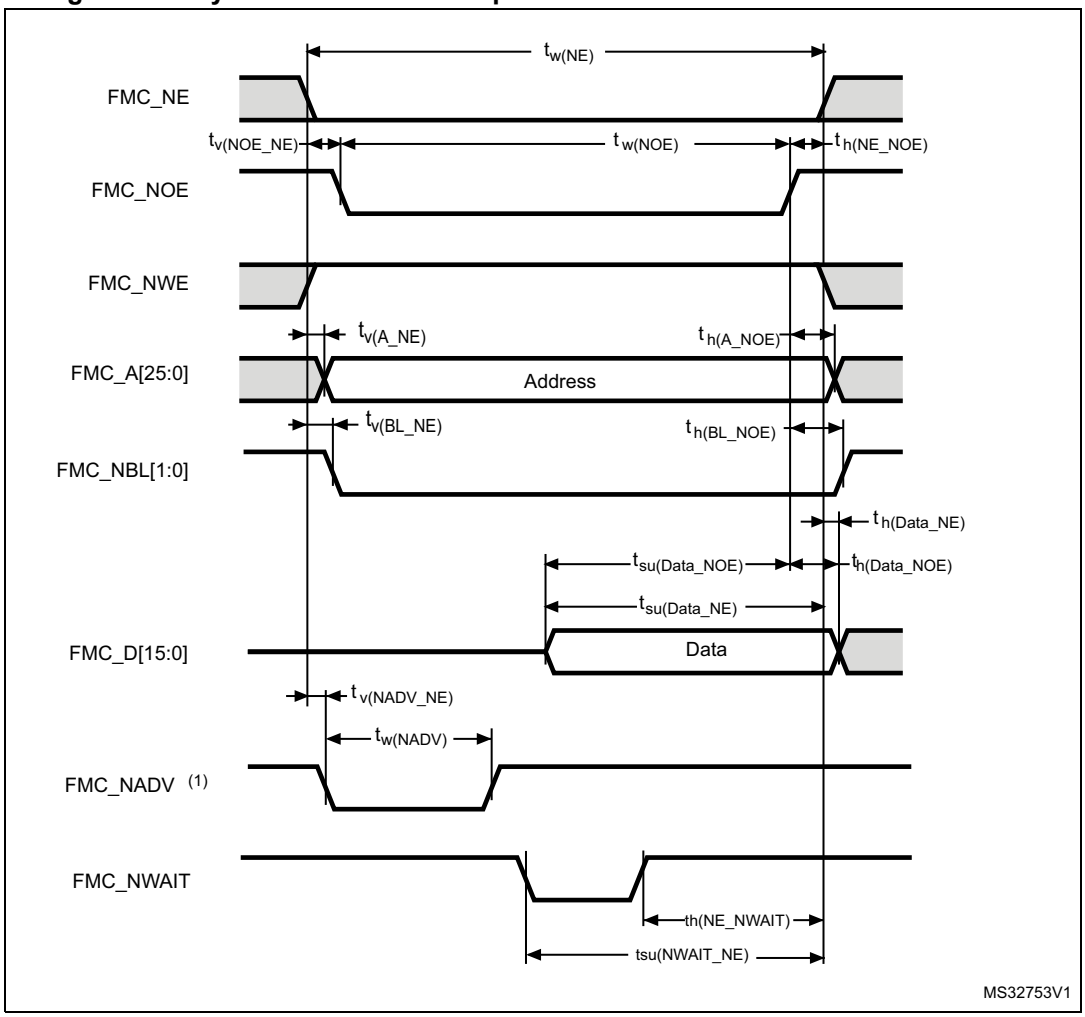


Figure 57. OctoSPI timing diagram - SDR mode

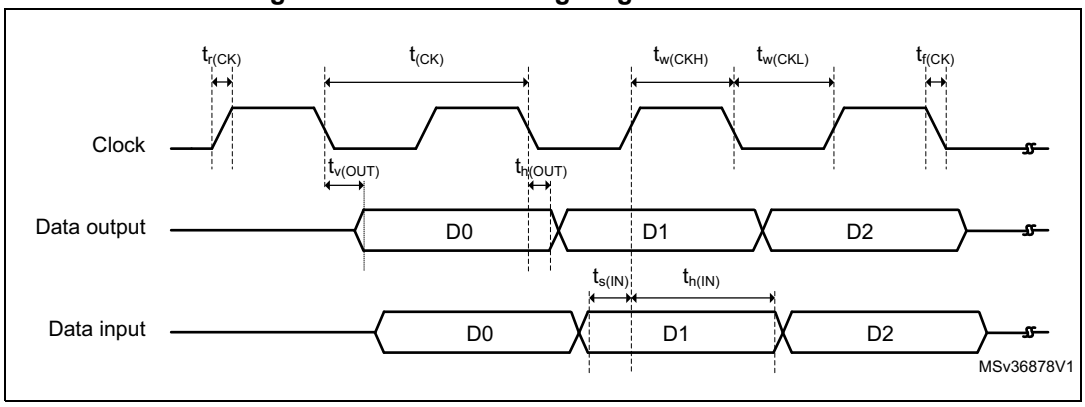


Figure 58. OctoSPI timing diagram - DDR mode

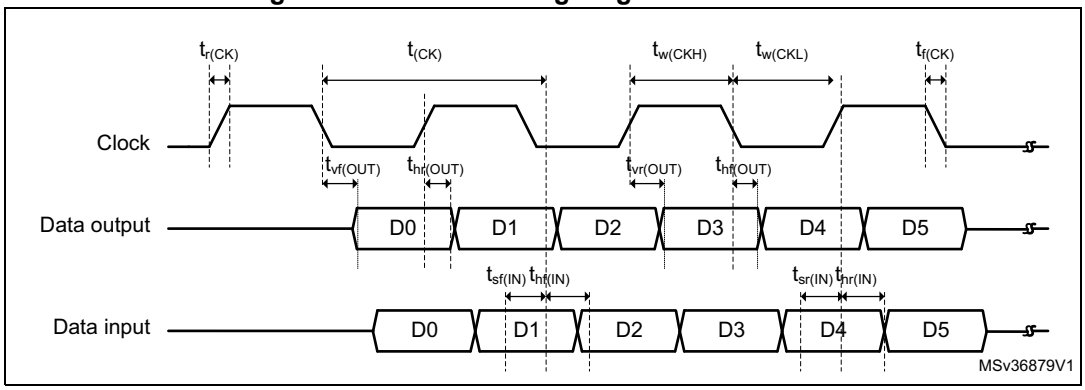
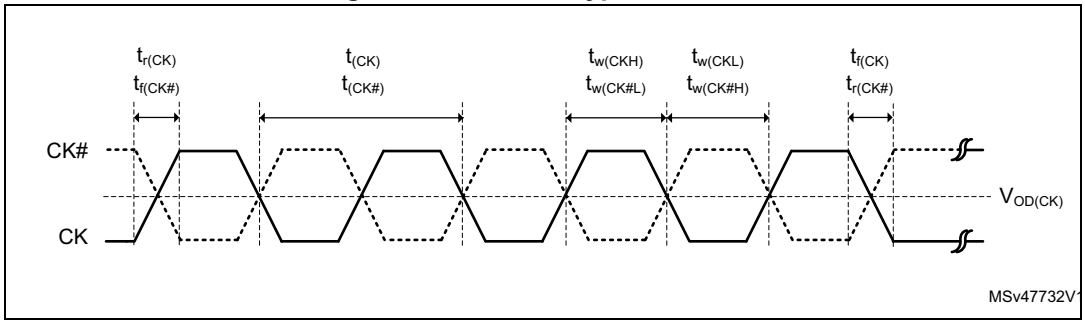


Figure 59. OctoSPI Hyperbus clock



See the different SDMMC diagrams in *Figure 64*, *Figure 65* and *Figure 66* below.

Figure 64. SDIO high-speed mode

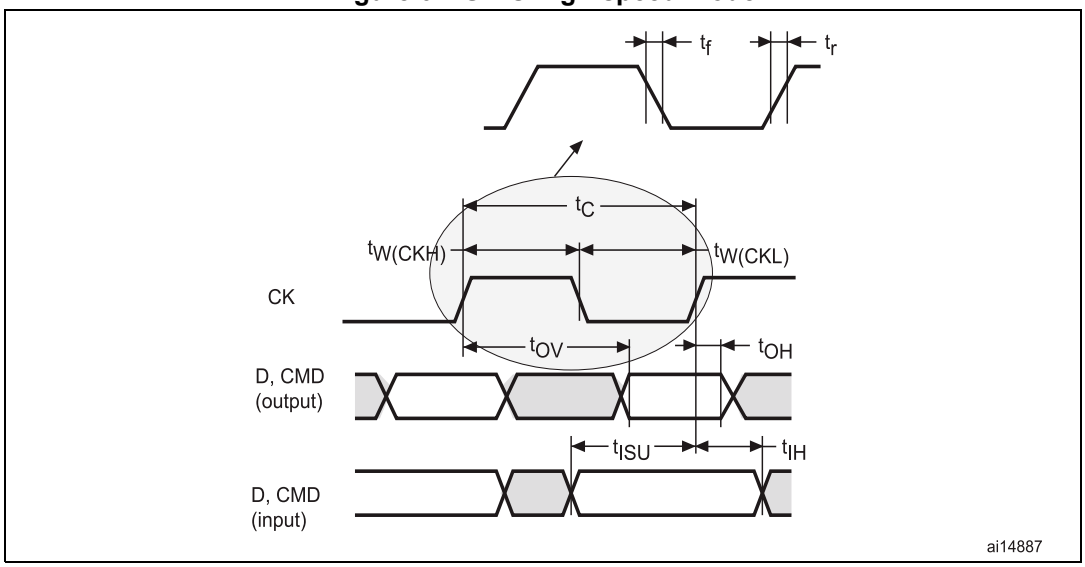


Figure 65. SD default mode

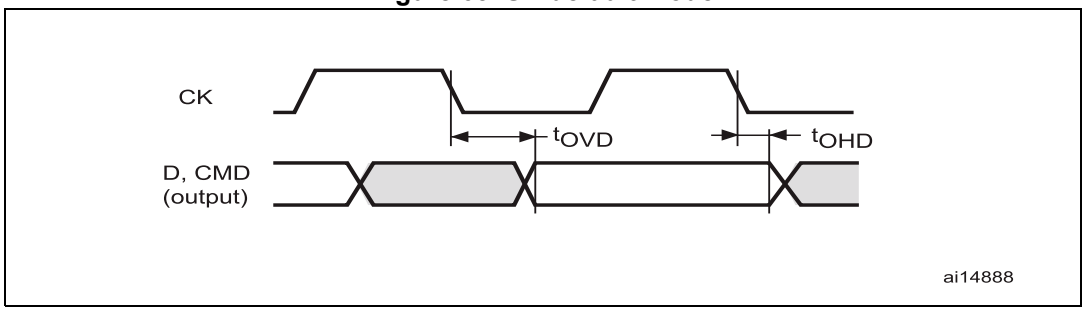


Figure 66. DDR mode

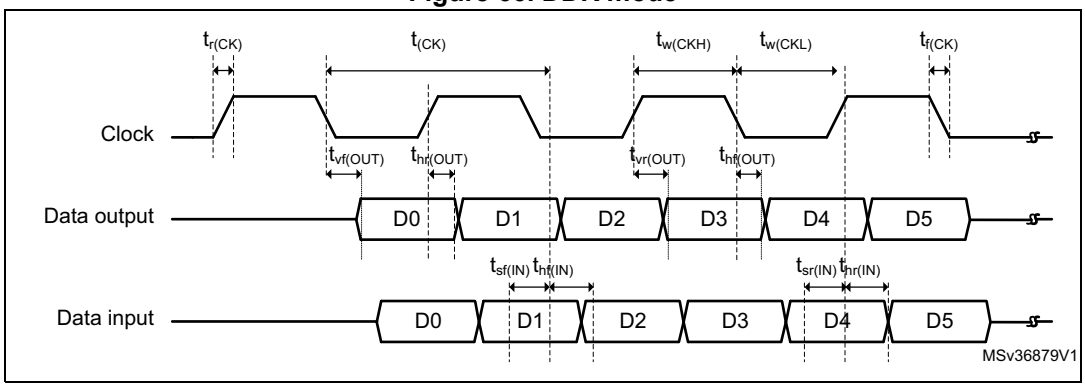
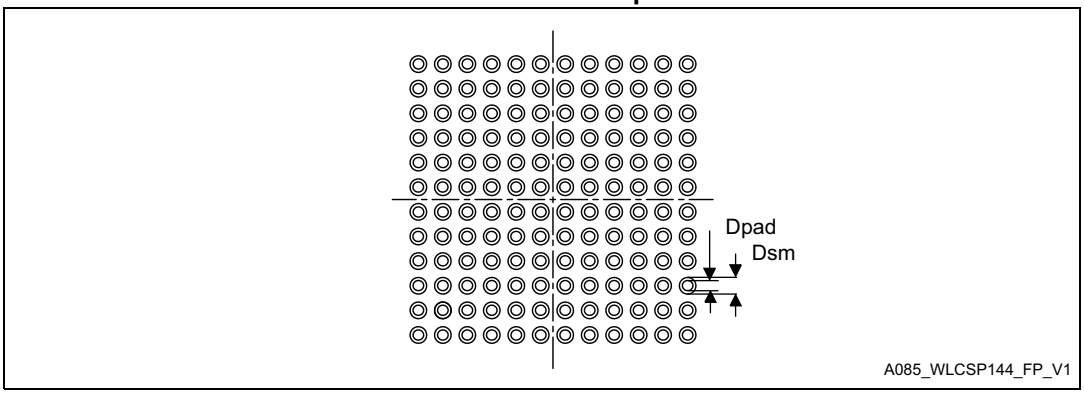


Table 123. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.0010	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	5.22	5.24	5.26	0.205	0.206	0.207
E	5.22	5.24	5.26	0.205	0.206	0.207
e	-	0.40	-	-	0.016	-
e1	-	4.40	-	-	0.173	-
e2	-	4.40	-	-	0.173	-
F	-	0.420[3]	-	-	0.0165	-
G	-	0.420[4]	-	-	0.0165	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. A3 value is guaranteed by technology design value.
3. This value is calculated from over value D and e1.
4. This value is calculated from over value E and e2.

Figure 77. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended footprint



1. Dimensions are expressed in millimeters.