

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 77 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s9vit6 |

# List of tables

**Table 8. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV) | 0x1FFF 75A8 - 0x1FFF 75A9 |
| TS_CAL2 | TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV) | 0x1FFF 75CA - 0x1FFF 75CB |

### 3.19.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 9. Internal voltage reference calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT | Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV) | 0x1FFF 75AA - 0x1FFF 75AB |

### 3.19.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware enables the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC1_IN18. As the $V_{BAT}$ voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the $V_{BAT}$ voltage.

## 3.20 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

## 3.27 Digital filter for sigma-delta modulators (DFSDM)

The STM32L4Sxxx devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (pulse density modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16-bit input resolution):
  - Internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high-value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - Monitoring continuously each input serial channel

**Table 10. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1, TIM8 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General-purpose | TIM2, TIM5 | 32-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM3, TIM4 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.32.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.32.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

## 3.35 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L4Sxxx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

**Table 12. USART/UART/LPUART features**

| USART modes/features(1) | USART1 | USART2 | USART3 | UART4 | UART5 | LPUART1 |
|---|---|---|---|---|---|---|
| Hardware flow control for modem | X | X | X | X | X | X |
| Continuous communication using DMA | X | X | X | X | X | X |
| Multiprocessor communication | X | X | X | X | X | X |
| Synchronous mode | X | X | X | - | - | - |
| Smartcard mode | X | X | X | - | - | - |
| Single-wire half-duplex communication | X | X | X | X | X | X |
| IrDA SIR ENDEC block | X | X | X | X | X | - |
| LIN mode | X | X | X | X | X | - |
| Dual clock domain | X | X | X | X | X | X |
| Wakeup from Stop 0 / Stop 1 modes | X | X | X | X | X | X |
| Wakeup from Stop 2 mode | - | - | - | - | - | X |
| Receiver timeout interrupt | X | X | X | X | X | - |
| Modbus communication | X | X | X | X | X | - |
| Auto baud rate detection | X (4 modes) | | | | | - |
| Driver enable | X | X | X | X | X | X |
| LPUART/USART data length | 7, 8 and 9 bits | | | | | |

1. X = supported.

The CAN peripheral supports:

- CAN protocol version 2.0 A, B Active
- Bit rates of up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - Scalable filter banks: 28 filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

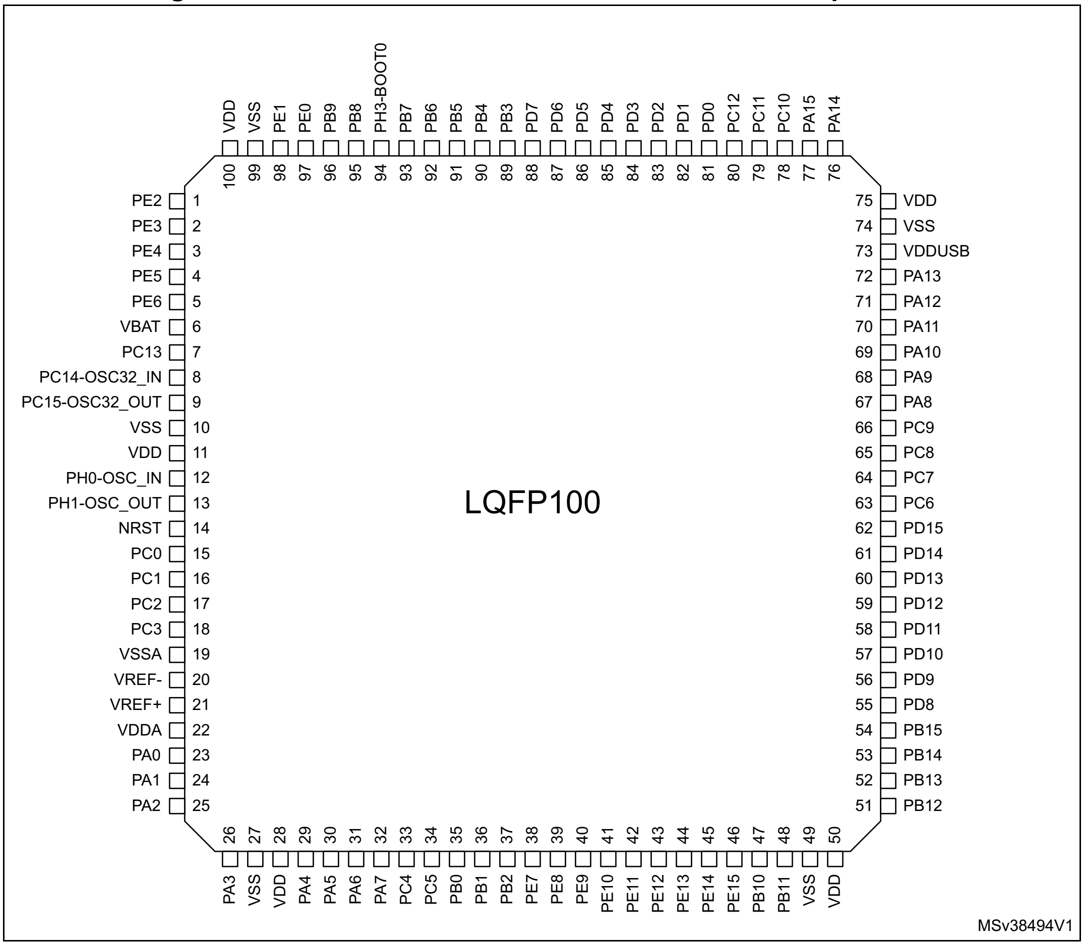
## 3.40 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

**Figure 16. STM32L4S5xx and STM32L4S7xx LQFP100 pinout(1)**




1. The above figure shows the package top view.

**Table 14. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | TT | 3.6 V tolerant I/O |
| | B | Dedicated BOOT0 pin |
| | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | **Option for TT or FT I/Os** | |
| | _f (1) | I/O, Fm+ capable |
| | _l (2) | I/O, with LCD function supplied by $V_{LCD}$ |
| | _u (3) | I/O, with USB function supplied by $V_{DDUSB}$ |
| | _a (4) | I/O, with Analog switch function supplied by $V_{DDA}$ |
| | _s (5) | I/O supplied only by $V_{DDIO2}$ |
| Notes | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions: Alternate functions | Functions selected through GPIOx_AFR registers | |
| Pin functions: Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in *Table 15* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 15* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 15* are: FT_u, FT_lu.
4. The related I/O structures in *Table 15* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Table 15. STM32L4Sxxx pin definitions (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 33 | K5 | 44 | L9 | H5 | 31 | 41 | L5 | L9 | K4 | PC4 | I/O | FT_a | - | USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT | COMP1_INM, ADC1_IN13 |
| 34 | L5 | 45 | K8 | J5 | - | - | K5 | K8 | - | PC5 | I/O | FT_a | - | SAI1_D3, USART3_RX, EVENTOUT | COMP1_INP, ADC1_IN14, WKUP5 |
| 35 | M5 | 46 | M9 | K5 | 32 | 42 | M5 | M9 | N4 | PB0 | I/O | TT_la | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT | OPAMP2_VOUT, ADC1_IN15 |
| 36 | M6 | 47 | H7 | L5 | 33 | 43 | J5 | H7 | L5 | PB1 | I/O | FT_a | - | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, OCTOSPIM_P1_IO0, LPTIM2_IN1, EVENTOUT | COMP1_INM, ADC1_IN16 |
| 37 | L6 | 48 | J7 | N5 | 34 | 44 | H5 | J7 | N5 | PB2 | I/O | FT_a | - | RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPIM_P1_DQS, LCD_B1, EVENTOUT | COMP1_INP |
| - | K6 | 49 | K7 | M5 | - | 45 | K6 | K7 | M5 | PF11 | I/O | FT | - | LCD_DE, DCMI_D12, DSI_TE, EVENTOUT | - |
| - | J7 | 50 | L8 | N6 | - | 46 | G5 | L8 | N6 | PF12 | I/O | FT | - | OCTOSPIM_P2_DQS, LCD_B0, FMC_A6, EVENTOUT | - |
| - | - | 51 | M8 | - | - | 47 | M1 | M8 | - | VSS | S | - | - | - | - |
| - | - | 52 | L7 | N7 | - | 48 | M6 | L7 | N7 | VDD | S | - | - | - | - |
| - | K7 | 53 | M7 | M6 | - | 49 | J6 | M7 | M6 | PF13 | I/O | FT | - | I2C4_SMBA, DFSDM1_DATIN6, LCD_B1, FMC_A7, EVENTOUT | - |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 59 | J10 | 81 | F4 | K11 | - | 85 | G9 | F4 | J8 | PD12 | I/O | FT_fl | - | TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_R7, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT | - |
| 60 | H12 | 82 | G3 | K13 | - | 86 | G10 | G3 | H8 | PD13 | I/O | FT_fl | - | TIM4_CH2, I2C4_SDA, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT | - |
| - | - | 83 | G1 | H12 | - | 87 | - | G1 | H12 | VSS | S | - | - | - | - |
| - | - | 84 | G2 | G13 | - | 88 | G12 | G2 | H13 | VDD | S | - | - | - | - |
| 61 | H11 | 85 | F3 | K10 | 63 | 89 | G8 | F3 | H11 | PD14 | I/O | FT | - | TIM4_CH3, LCD_B2, FMC_D0, EVENTOUT | - |
| 62 | H10 | 86 | F1 | H11 | 64 | 90 | G7 | F1 | H10 | PD15 | I/O | FT | - | TIM4_CH4, LCD_B3, FMC_D1, EVENTOUT | - |
| - | G10 | 87 | F2 | J12 | - | 91 | F12 | F2 | H9 | PG2 | I/O | FT_s | - | SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT | - |
| - | F9 | 88 | F5 | J11 | - | 92 | F7 | F5 | G8 | PG3 | I/O | FT_s | - | SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT | - |
| - | F10 | 89 | F6 | J10 | - | 93 | F10 | F6 | G7 | PG4 | I/O | FT_s | - | SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT | - |
| - | E9 | 90 | F7 | J9 | - | 94 | F8 | F7 | G9 | PG5 | I/O | FT_s | - | SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT | - |
| - | G4 | 91 | E5 | G11 | - | 95 | F9 | E5 | G12 | PG6 | I/O | FT_s | - | OCTOSPIM_P1_DQS, I2C3_SMBA, LPUART1_RTS_DE, LCD_R1, DSI_TE, EVENTOUT | - |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 72 | A11 | 105 | B3 | A11 | 74 | 107 | B10 | B3 | A11 | PA13 (JTMS/SWDIO) | I/O | FT | (4) | JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT | - |
| 73 | C11 | 106 | B2 | E12 | 75 | 108 | C11 | B2 | D12 | VDDUSB | S | - | - | - | - |
| 74 | F11 | 107 | A1 | C12 | 76 | 109 | A12 | A1 | C12 | VSS | S | - | - | - | - |
| 75 | G11 | 108 | B1 | C13 | 77 | 110 | A11 | B1 | C13 | VDD | S | - | - | - | - |
| - | - | - | - | E11 | - | - | - | - | - | PH6 | I/O | FT | - | I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8, EVENTOUT | - |
| - | - | - | - | D12 | - | - | - | - | - | PH7 | I/O | FT_f | - | I2C3_SCL, DCMI_D9, EVENTOUT | - |
| - | - | - | - | D11 | - | - | - | - | C11 | PH9 | I/O | FT | - | I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0, EVENTOUT | - |
| - | - | - | - | B13 | - | - | - | - | B13 | PH12 | I/O | FT | - | TIM5_CH3, OCTOSPIM_P2_IO7, DCMI_D3, EVENTOUT | - |
| - | - | - | - | A13 | - | - | - | - | A13 | PH14 | I/O | FT | - | TIM8_CH2N, DCMI_D4, EVENTOUT | - |
| - | - | - | - | B12 | - | - | - | - | B12 | PH15 | I/O | FT | - | TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11, EVENTOUT | - |
| - | - | - | - | A12 | - | - | - | - | A12 | PI0 | I/O | FT | - | TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13, EVENTOUT | - |
| - | - | - | - | C11 | - | - | - | - | - | PI8 | I/O | FT | - | OCTOSPIM_P2_NCS, DCMI_D12, EVENTOUT | - |
| - | - | - | - | B11 | - | - | - | - | B11 | PI1 | I/O | FT | - | SPI2_SCK, DCMI_D8, EVENTOUT | - |

**Table 18. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx memory map and peripheral register boundary addresses(1) (continued)**

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| APB1 | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0C00- 0x4000 0FFF | 1 KB | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | 1 KB | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

1. The gray color is used for reserved boundary addresses.

**Table 22. General operating conditions (continued)**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6[4] | LQFP144 | - | - | 625 | mW |
| | | LQFP100 | - | - | 476 | |
| | | UFBGA169 | - | - | 385 | |
| | | UFBGA132 | - | - | 364 | |
| | | WLCSP144 | - | - | 664 | |
| $P_D$ | Power dissipation at $T_A$ = 125 °C for suffix 3[4] | LQFP144 | - | - | 156 | mW |
| | | LQFP100 | - | - | 119 | |
| | | UFBGA169 | - | - | 96 | |
| | | UFBGA132 | - | - | 91 | |
| | | WLCSP144 | - | - | 831 | |
| TA | Ambient temperature for the suffix 6 version | Maximum power dissipation | | –40 | 85 | °C |
| | | Low-power dissipation[5] | | –40 | 105 | |
| | Ambient temperature for the suffix 3 version | Maximum power dissipation | | –40 | 125 | |
| | | Low-power dissipation[5] | | –40 | 130 | |
| TJ | Junction temperature range | Suffix 6 version | | –40 | 105 | °C |
| | | Suffix 3 version | | –40 | 130 | |

1. When RESET is released functionality is guaranteed down to $V_{BOR0}$ Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN($V_{DD}$, $V_{DDA}$, $V_{DDIO2}$, $V_{DDUSB}$)+3.6 V and 5.5V.
3. For operation with voltage higher than Min ($V_{DD}$, $V_{DDA}$, $V_{DDIO2}$, $V_{DDUSB}$) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.7: Thermal characteristics*).
5. In low-power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.7: Thermal characteristics*).

### 6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 25. Embedded internal voltage reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | $-40$ °C < $T_A$ < +130 °C | 1.182 | 1.212 | 1.232 | V |
| $t_{S\_vrefint}$ (1) | ADC sampling time when reading the internal reference voltage | - | 4(2) | - | - | µs |
| $t_{start\_vrefint}$ | Start time of reference voltage buffer when ADC is enable | - | - | 8 | 12(2) | µs |
| $I_{DD}(V_{REFINTBUF})$ | $V_{REFINT}$ buffer consumption from $V_{DD}$ when converted by ADC | - | - | 12.5 | 20(2) | µA |
| $\Delta V_{REFINT}$ | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V | - | 5 | 7.5(2) | mV |
| $T_{Coeff}$ | Average temperature coefficient | $-40$°C < $T_A$ < +130°C | - | 30 | 50(2) | ppm/°C |
| $A_{Coeff}$ | Long term stability | 1000 hours, T = 25°C | - | 300 | 1000(2) | ppm |
| $V_{DDCoeff}$ | Average voltage coefficient | 3.0 V < $V_{DD}$ < 3.6 V | - | 250 | 1200(2) | ppm/V |
| $V_{REFINT\_DIV1}$ | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$ | 1/2 reference voltage | | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$ | 3/4 reference voltage | | 74 | 75 | 76 | |

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

### 6.3.9 PLL characteristics

The parameters given in *Table 55* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 55. PLL, PLLSAI1, PLLSAI2 characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock[2] | - | 2.66 | - | 16 | MHz |
| | PLL input clock duty cycle | - | 45 | - | 55 | % |
| $f_{PLL\_P\_OUT}$ | PLL multiplier output clock P | Voltage scaling Range 1 Normal mode | 2.0645 | - | 80 | MHz |
| | | Voltage scaling Range 1 Boost mode | 2.0645 | - | 120 | |
| | | Voltage scaling Range 2 | 2.0645 | - | 26 | |
| $f_{PLL\_Q\_OUT}$ | PLL multiplier output clock Q | Voltage scaling Range 1 Normal mode | 8 | - | 80 | |
| | | Voltage scaling Range 1 Boost mode | 8 | - | 120 | |
| | | Voltage scaling Range 2 | 8 | - | 26 | |
| $f_{PLL\_R\_OUT}$ | PLL multiplier output clock R | Voltage scaling Range 1 Normal mode | 8 | - | 80 | |
| | | Voltage scaling Range 1 Boost mode | 8 | - | 120 | |
| | | Voltage scaling Range 2 | 8 | - | 26 | |
| $f_{VCO\_OUT}$ | PLL VCO output | Voltage scaling Range 1 | 64 | - | 344 | |
| | | Voltage scaling Range 2 | 64 | - | 128 | |
| $t_{LOCK}$ | PLL lock time | - | - | 15 | 40 | μs |
| Jitter | RMS cycle-to-cycle jitter | System clock 80 MHz | - | 40 | - | ±ps |
| | RMS period jitter | | - | 30 | - | |
| $I_{DD}(PLL)$ | PLL power consumption on $V_{DD}$[1] | VCO freq = 64 MHz | - | 150 | 200 | μA |
| | | VCO freq = 96 MHz | - | 200 | 260 | |
| | | VCO freq = 192 MHz | - | 300 | 380 | |
| | | VCO freq = 344 MHz | - | 520 | 650 | |

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

### 6.3.10 MIPI D-PHY characteristics

The parameters given in *Table 56* and *Table 57* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22*.

**Table 69. I/O AC characteristics(1)(2) (continued)**

| Speed | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 | Fmax | Maximum frequency | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 50 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 25 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 5 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 100(3) | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 37.5 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 5 | |
| | Tr/Tf | Output rise and fall time | C=50 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 5.8 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 11 | |
| | | | C=50 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 28 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 2.5 | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 5 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 12 | |
| 11 | Fmax | Maximum frequency | C=30 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 120(3) | MHz |
| | | | C=30 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 50 | |
| | | | C=30 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 10 | |
| | | | C=10 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 180(3) | |
| | | | C=10 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 75 | |
| | | | C=10 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 10 | |
| | Tr/Tf | Output rise and fall time | C=30 pF, 2.7 V≤$V_{DDIOx}$≤3.6 V | - | 3.3 | ns |
| | | | C=30 pF, 1.62 V≤$V_{DDIOx}$≤2.7 V | - | 6 | |
| | | | C=30 pF, 1.08 V≤$V_{DDIOx}$≤1.62 V | - | 16 | |
| Fm+ | Fmax | Maximum frequency | C=50 pF, 1.6 V≤$V_{DDIOx}$≤3.6 V | - | 1 | MHz |
| | Tf | Output fall time(4) | | - | 5 | ns |

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to $I^2C$ specification.

**Table 73. ADC characteristics(1) (2) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{LATR}$ | Trigger conversion latency Regular and injected channels without conversion abort | CKMODE = 00 | 1.5 | 2 | 2.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | - | - | 2.0 | |
| | | CKMODE = 10 | - | - | 2.25 | |
| | | CKMODE = 11 | - | - | 2.125 | |
| $t_{LATRINJ}$ | Trigger conversion latency Injected channels aborting a regular conversion | CKMODE = 00 | 2.5 | 3 | 3.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | - | - | 3.0 | |
| | | CKMODE = 10 | - | - | 3.25 | |
| | | CKMODE = 11 | - | - | 3.125 | |
| $t_s$ | Sampling time | $f_{ADC}$ = 80 MHz | 0.03125 | - | 8.00625 | µs |
| | | - | 2.5 | - | 640.5 | $1/f_{ADC}$ |
| $t_{ADCVREG\_STUP}$ | ADC voltage regulator start-up time | - | - | - | 20 | µs |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 80 MHz Resolution = 12 bits | 0.1875 | - | 8.1625 | µs |
| | | Resolution = 12 bits | ts + 12.5 cycles for successive approximation = 15 to 653 | | | $1/f_{ADC}$ |
| $I_{DDA}(ADC)$ | ADC consumption from the $V_{DDA}$ supply | fs = 5 Msps | - | 730 | 830 | µA |
| | | fs = 1 Msps | - | 160 | 220 | |
| | | fs = 10 ksps | - | 16 | 50 | |
| $I_{DDV\_S}(ADC)$ | ADC consumption from the $V_{REF+}$ single ended mode | fs = 5 Msps | - | 130 | 160 | µA |
| | | fs = 1 Msps | - | 30 | 40 | |
| | | fs = 10 ksps | - | 0.6 | 2 | |
| $I_{DDV\_D}(ADC)$ | ADC consumption from the $V_{REF+}$ differential mode | fs = 5 Msps | - | 260 | 310 | µA |
| | | fs = 1 Msps | - | 60 | 70 | |
| | | fs = 10 ksps | - | 1.3 | 3 | |

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4V). It is disable when $V_{DDA}$ ≥ 2.4 V.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package.
Refer to *Section 4: Pinouts and pin description* for further details.

Table 76. ADC accuracy - limited test conditions 2[1][2][3]

| Sym-bol | Parameter | Conditions[4] | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ET | Total unadjusted error | ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ $V_{DDA}$ | Single ended | Fast channel (max speed) | - | 4 | 6.5 | LSB |
| | | | | Slow channel (max speed) | - | 4 | 6.5 | |
| | | | Differential | Fast channel (max speed) | - | 3.5 | 5.5 | |
| | | | | Slow channel (max speed) | - | 3.5 | 5.5 | |
| EO | Offset error | | Single ended | Fast channel (max speed) | - | 1 | 4.5 | |
| | | | | Slow channel (max speed) | - | 1 | 5 | |
| | | | Differential | Fast channel (max speed) | - | 1.5 | 3 | |
| | | | | Slow channel (max speed) | - | 1.5 | 3 | |
| EG | Gain error | | Single ended | Fast channel (max speed) | - | 2.5 | 6 | |
| | | | | Slow channel (max speed) | - | 2.5 | 6 | |
| | | | Differential | Fast channel (max speed) | - | 2.5 | 3.5 | |
| | | | | Slow channel (max speed) | - | 2.5 | 3.5 | |
| ED | Differential linearity error | | Single ended | Fast channel (max speed) | - | 1 | 1.5 | |
| | | | | Slow channel (max speed) | - | 1 | 1.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 1.2 | |
| | | | | Slow channel (max speed) | - | 1 | 1.2 | |
| EL | Integral linearity error | | Single ended | Fast channel (max speed) | - | 1.5 | 3.5 | |
| | | | | Slow channel (max speed) | - | 1.5 | 3.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 3 | |
| | | | | Slow channel (max speed) | - | 1 | 2.5 | |
| ENOB | Effective number of bits | | Single ended | Fast channel (max speed) | 10 | 10.5 | - | bits |
| | | | | Slow channel (max speed) | 10 | 10.5 | - | |
| | | | Differential | Fast channel (max speed) | 10.7 | 10.9 | - | |
| | | | | Slow channel (max speed) | 10.7 | 10.9 | - | |
| SINAD | Signal-to-noise and distortion ratio | | Single ended | Fast channel (max speed) | 62 | 65 | - | dB |
| | | | | Slow channel (max speed) | 62 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 66 | 67.4 | - | |
| | | | | Slow channel (max speed) | 66 | 67.4 | - | |
| SNR | Signal-to-noise ratio | | Single ended | Fast channel (max speed) | 64 | 66 | - | |
| | | | | Slow channel (max speed) | 64 | 66 | - | |
| | | | Differential | Fast channel (max speed) | 66.5 | 68 | - | |
| | | | | Slow channel (max speed) | 66.5 | 68 | - | |

**Table 83. OPAMP characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LOAD}$ | Drive current | Normal mode | $V_{DDA} \geq 2$ V | - | - | 500 | µA |
| | | Low-power mode | | - | - | 100 | |
| $I_{LOAD\_PGA}$ | Drive current in PGA mode | Normal mode | $V_{DDA} \geq 2$ V | - | - | 450 | |
| | | Low-power mode | | - | - | 50 | |
| $R_{LOAD}$ | Resistive load (connected to VSSA or to VDDA) | Normal mode | $V_{DDA} < 2$ V | 4 | - | - | kΩ |
| | | Low-power mode | | 20 | - | - | |
| $R_{LOAD\_PGA}$ | Resistive load in PGA mode (connected to VSSA or to $V_{DDA}$) | Normal mode | $V_{DDA} < 2$ V | 4.5 | - | - | |
| | | Low-power mode | | 40 | - | - | |
| $C_{LOAD}$ | Capacitive load | - | | - | - | 50 | pF |
| CMRR | Common mode rejection ratio | Normal mode | | - | -85 | - | dB |
| | | Low-power mode | | - | -90 | - | |
| PSRR | Power supply rejection ratio | Normal mode | $C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC | 70 | 85 | - | dB |
| | | Low-power mode | $C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC | 72 | 90 | - | |
| GBW | Gain Bandwidth Product | Normal mode | $V_{DDA} \geq 2.4$ V (OPA_RANGE = 1) | 550 | 1600 | 2200 | kHz |
| | | Low-power mode | | 100 | 420 | 600 | |
| | | Normal mode | $V_{DDA} < 2.4$ V (OPA_RANGE = 0) | 250 | 700 | 950 | |
| | | Low-power mode | | 40 | 180 | 280 | |
| SR(2) | Slew rate (from 10 and 90% of output voltage) | Normal mode | $V_{DDA} \geq 2.4$ V | - | 700 | - | V/ms |
| | | Low-power mode | | - | 180 | - | |
| | | Normal mode | $V_{DDA} < 2.4$ V | - | 300 | - | |
| | | Low-power mode | | - | 80 | - | |
| AO | Open loop gain | Normal mode | | 55 | 110 | - | dB |
| | | Low-power mode | | 45 | 110 | - | |
| $V_{OHSAT}$(2) | High saturation voltage | Normal mode | $I_{load}$ = max or $R_{load}$ = min Input at $V_{DDA}$. | $V_{DDA}$ - 100 | - | - | mV |
| | | Low-power mode | | $V_{DDA}$ - 50 | - | - | |
| $V_{OLSAT}$(2) | Low saturation voltage | Normal mode | $I_{load}$ = max or $R_{load}$ = min Input at 0. | - | - | 100 | |
| | | Low-power mode | | - | - | 50 | |
| $\varphi_m$ | Phase margin | Normal mode | | - | 74 | - | ° |
| | | Low-power mode | | - | 66 | - | |

**Figure 49. Synchronous multiplexed NOR/PSRAM read timings**