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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s9zij6

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts

Peripheral		S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
Flash memory		2 Mbytes									
SRAM	System	640 (192 + 64 + 384) Kbytes									
	Backup	128 bytes									
External memory controller for static memories (FSMC)		Yes(1)			Yes						
OctoSPI		2									
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low-power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
Comm. interfaces	SPI	3									
	I^2C	4									
	USART/UART UART LPUART	3 2 1									
	SAI	2									
	CAN	1									
	USB OTG FS	Yes									
	SDMMC	Yes									
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes									
Chrom-ART Accelerator™		Yes									
Chrom-GRC™		No	Yes		No		Yes		No	Yes	

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts (continued)

Peripheral	S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
LCD - TFT	No	Yes		No		Yes		No	Yes	
MIPI DSI Host(2)	No		Yes	No			Yes	No		Yes
Random number generator	Yes									
AES + HASH	Yes									
GPIOs Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1									
	16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage	1.71 to 3.6 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA 132	LQFP 144 WLCSP144	LQFP 144	LQFP 144, UFBGA 144 WLCSP 144	UFBGA169		
Bootloader	USART 1	USART 2	USART 3	SPI1	SPI2	I2C1	I2C2	I2C3	CAN1	USB through DFU

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4S9xx sales types.

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM3 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be

3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

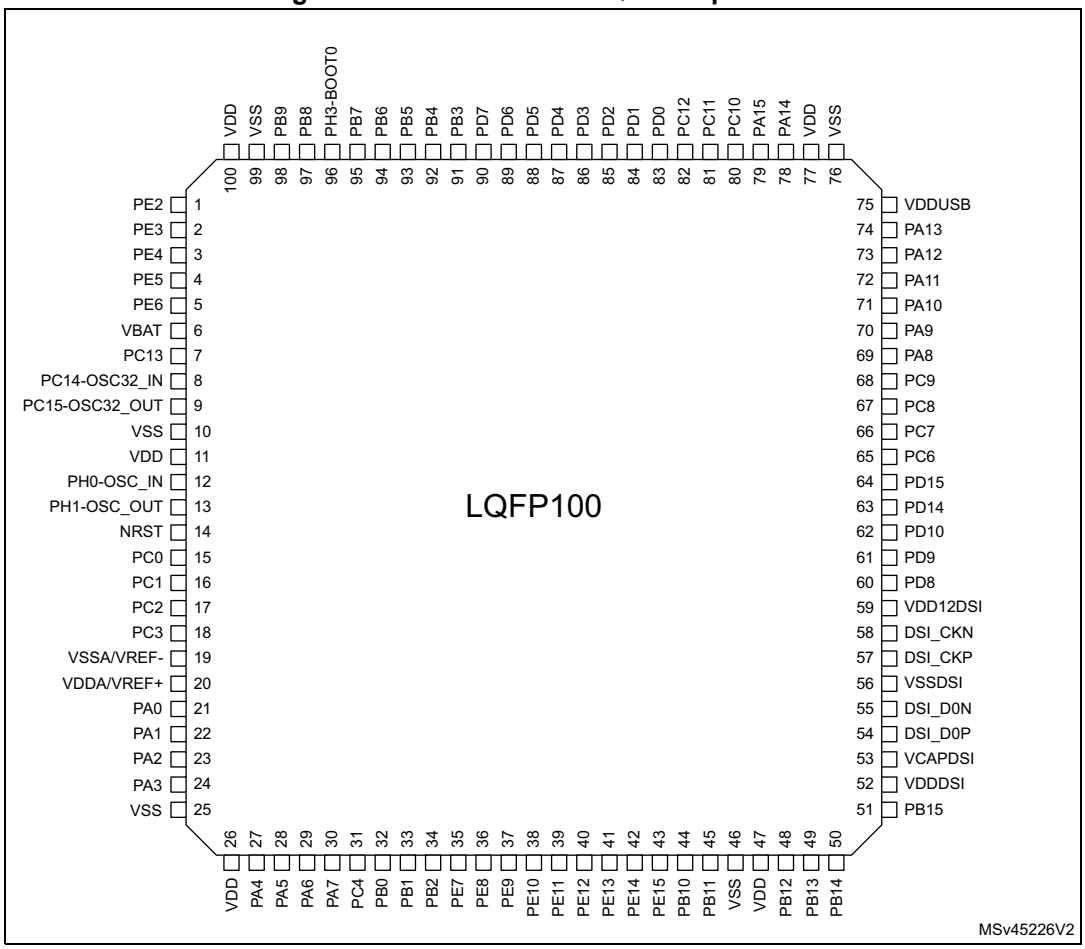
The DMA supports:

- 14 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

Figure 17. STM32L4S9xx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	BGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
48	L11	70	M4	H8	45	66	K9	M4	H7	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, OCTOSPIM_P1_NCS, DSI_TE, COMP2_OUT, EVENTOUT	-
-	-	-	-	K9	-	-	-	-	K8	PH4	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_DQS, EVENTOUT	-
-	-	-	-	L9	-	-	-	-	L9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK, EVENTOUT	-
-	-	-	-	N10	-	-	-	-	N10	PH8	I/O	FT_f	-	I2C3_SDA, OCTOSPIM_P2_IO3, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	M9	-	-	-	-	M9	PH10	I/O	FT	-	TIM5_CH1, OCTOSPIM_P2_IO5, DCMI_D1, EVENTOUT	-
-	-	-	-	M10	-	-	-	-	M10	PH11	I/O	FT	-	TIM5_CH2, OCTOSPIM_P2_IO6, DCMI_D2, EVENTOUT	-
-	-	-	-	C2	-	-	-	-	C2	VSS	S	-	-	-	-
49	F12	71	M3	A7	46	67	M12	M3	A7	VSS	S	-	-	-	-
50	G12	72	M1	N11	47	68	L11	M1	N11	VDD	S	-	-	-	-
51	L12	73	J4	N12	48	69	L10	J4	N12	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	3.40	3.60	mA	131	138	µA/MHz
				Coremark	3.90	3.95		150	152	
				Dhrystone2.1	4.25	4.30		163	165	
				Fibonacci	3.65	3.90		140	150	
				While(1)	3.15	3.15		121	121	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.5	12.5	mA	144	156	µA/MHz
				Coremark	13.5	13.5		169	169	
				Dhrystone2.1	14.5	14.5		181	181	
				Fibonacci	12.5	14.0		156	175	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	21.5	21.5		179	179	
				Dhrystone2.1	22.5	22.5		188	188	
				Fibonacci	20.0	21.0		167	175	
				While(1)	16.5	16.5		138	138	

Table 33. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	3.35	mA	129	µA/MHz
				Coremark	3.10		119	
				Dhrystone2.1	3.65		140	
				Fibonacci	3.20		123	
				While(1)	2.85		110	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.0	mA	138	µA/MHz
				Coremark	10.5		131	
				Dhrystone2.1	12.5		156	
				Fibonacci	10.5		131	
				While(1)	9.40		118	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.0	mA	150	µA/MHz
				Coremark	16.5		138	
				Dhrystone2.1	19.5		163	
				Fibonacci	17.5		146	
				While(1)	15.0		125	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	435	µA	218	µA/MHz
				Coremark	395		198	
				Dhrystone2.1	470		235	
				Fibonacci	425		213	
				While(1)	455		228	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 43. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	I2C1 APB clock domain	1.4	1.4	1.25	2	µA/MHz
	I2C2 independent clock domain	3.5	3.4	2.5	3.5	
	I2C2 APB clock domain	1.4	1.25	1.25	1	
	I2C3 independent clock domain	3.25	3.15	2.9	3	
	I2C3 APB clock domain	1.15	1	0.835	1	
	I2C4 independent clock domain	3.5	3.25	2.75	3	
	I2C4 APB clock domain	1.35	1.25	1	1.5	
	LPUART1 independent clock domain	3.15	3	2.45	3	
	LPUART1 APB clock domain	1.65	1.5	1.3	1.5	
	LPTIM1 independent clock domain	3.6	3.5	2.9	3	
	LPTIM1 APB clock domain	1	0.875	0.835	1	
	LPTIM2 independent clock domain	3.4	3.25	2.55	3.5	
	LPTIM2 APB clock domain	1.1	1	0.79	1	
	OPAMP	0.415	0.375	0.415	0.5	
	PWR	0.5	0.375	0.415	0.5	
	RTCAPB	1.25	1.15	1.25	1	
	SPI2	2.6	2.4	2.1	2.5	
	SPI3	3	2.75	2.5	3	
	TIM2	6.15	5.75	4.65	4.5	
	TIM3	5.25	4.9	4.15	5	
	TIM4	5.15	4.75	4.15	5	
	TIM5	6.5	6	5	6	
	TIM6	1.35	1.15	1.25	1	
	TIM7	1.25	1.15	0.835	1	

Table 43. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	USART2 independent clock domain	5.35	5	4.15	4.5	µA/MHz
	USART2 APB clock domain	3	2.75	2.5	2.5	
	USART3 independent clock domain	6.35	6	5	5.5	
	USART3 APB clock domain	2.6	2.4	2.1	2.5	
	UART4 independent clock domain	5.15	4.9	3.75	4.5	
	UART4 APB clock domain	2.5	2.25	2.1	2.5	
	UART5 independent clock domain	5.4	5	4.15	5	
	UART5 APB clock domain	2.4	2.25	2.1	2	
	WWDG	0.75	0.625	0.835	0.5	
	All APB1 on	110	100	84	97	
APB2	AHB to APB2 bridge	0.185	0.15	0.125	0.5	µA/MHz
	DFSDM	9.5	9	7.5	8.5	
	DSI independent clock domain	33	34.5	29.5	NA	
	DSI APB clock domain	13	7.15	29	NA	
	FW	0.665	0.625	0.5	0.5	
	LTDC independent clock domain	35.5	34.5	40	NA	
	LTDC APB clock domain	18	17	14	NA	
	SAI1 independent clock domain	3.1	2.9	2.5	3	
	SAI1 APB clock domain	2.6	2.4	1.9	2	
	SAI2 independent clock domain	3.15	3	2.55	3	
	SAI2 APB clock domain	2.6	2.4	1.9	2.5	
	SPI1	2.25	2.15	1.75	1	
	SYSCFG/VREFBUF/COMP	0.565	0.6	0.5	0.5	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 49*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 49. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 26*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

6.3.13 Flash memory characteristics

Table 60. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	41.8	43	
		Fast programming	30.4	31	
t_{ERASE}	Page (4 Kbytes) erase time	-	22	24.5	
t_{prog_bank}	One bank (1 Mbyte) programming time	Normal programming	10.7	11	s
		Fast programming	7.7	8	
t_{ME}	Mass erase time (one or two banks)	-	22.1	25	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 61. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 67. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u, PB2 and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

6.3.22 Digital-to-Analog converter characteristics

Table 79. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 79. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Figure 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

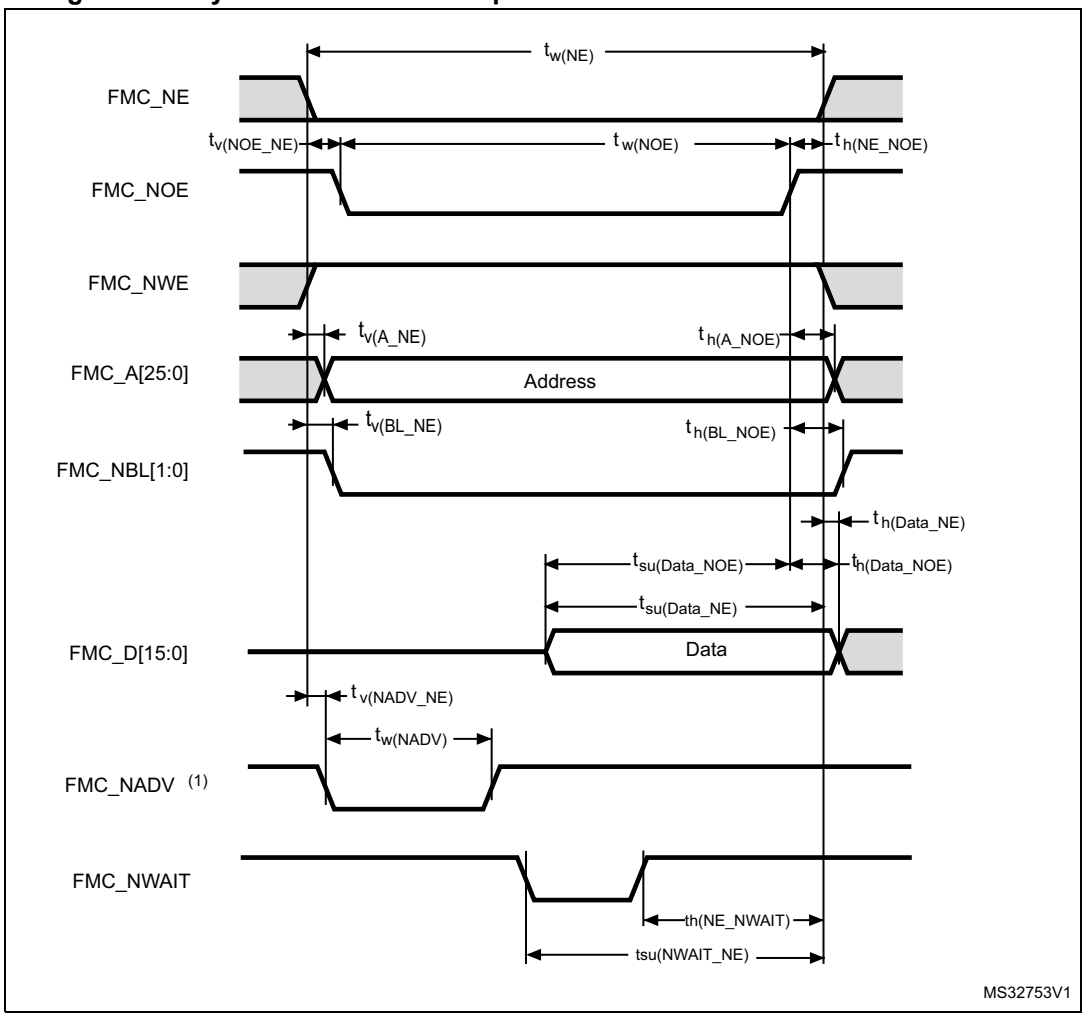


Figure 48. Asynchronous multiplexed PSRAM/NOR write waveforms

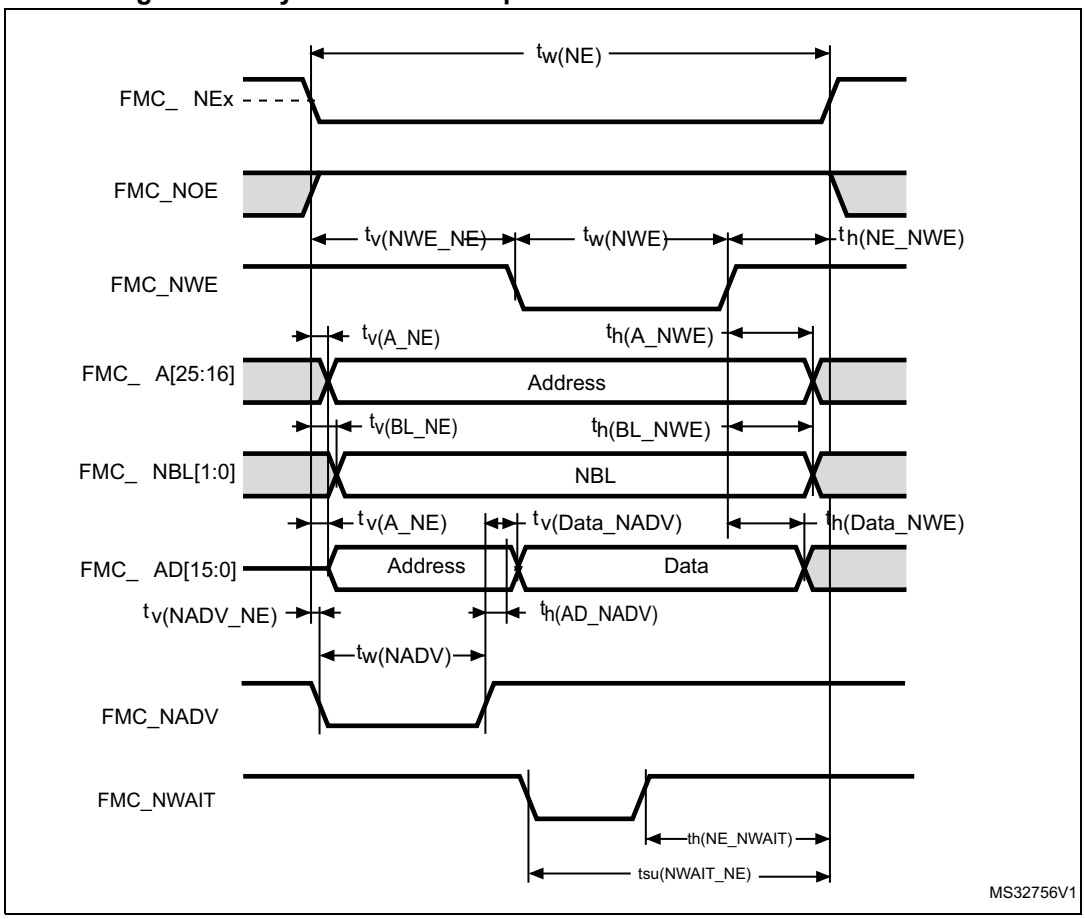


Table 103. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$5T_{HCLK}$-0.5	$5T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}+0.5	T_{HCLK}+1.5	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}-3	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	0	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK}+2	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+0.5	-	

Table 105. Synchronous multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	4	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Table 113. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+0.5$	
$t_{v(CK)}$	Clock valid time	-		-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-		$t_{(CK)}/2-0.5$	-	-	
$t_{w(CS)}$	Chip select high time	-		3 x $t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-		0	-	-	
$t_{v(DS)}$	Data storbe input valid time	-		0	-	-	
$t_{h(DS)}$	Data storbe input hold time	-		0	-	-	
$t_{v(RWDS)}$	Data storbe output valid time	-		-	-	3 x $t_{(CK)}$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		-3.5	-	$t_{(CK)}/2-5.75$(3)	
		Voltage Range 2		-5.5	-	$t_{(CK)}/2-9$(3)	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		5.75	-	-	
		Voltage Range 2		9	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	ns
			DHQC = 1 Pres=1,2 ...		tpclk/4+1.5	tpclk/4+2.25	
		Voltage Range 2	DHQC = 0		8	11	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	0.5	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-1.75	-	-	
		Voltage Range 2	DHQC = 0	0.75	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Data input setup time maximum does not take into account Data level switching duration.

Figure 57. OctoSPI timing diagram - SDR mode

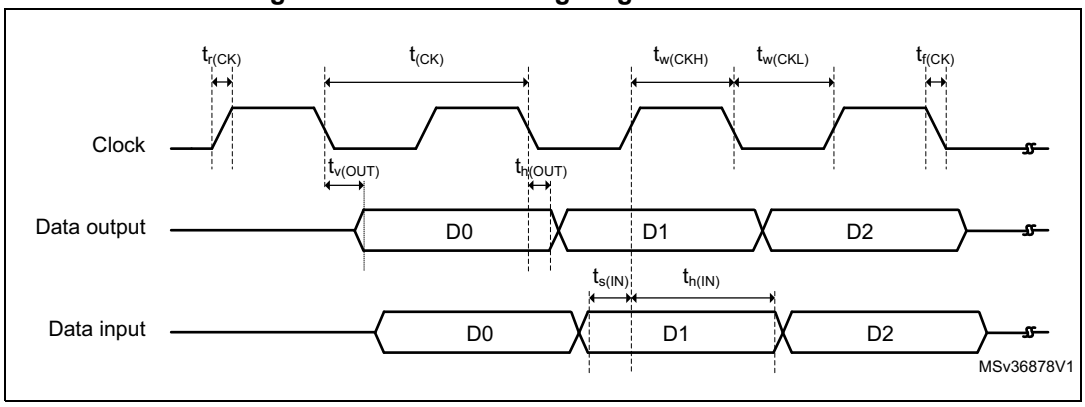


Figure 58. OctoSPI timing diagram - DDR mode

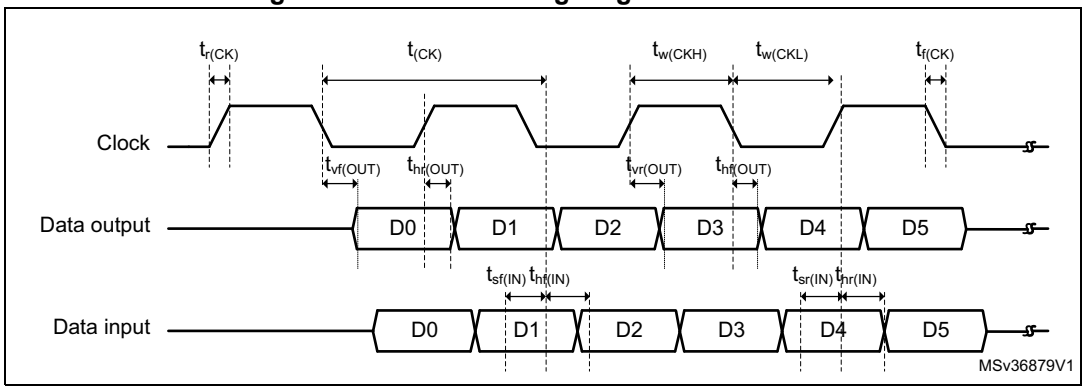


Figure 59. OctoSPI Hyperbus clock