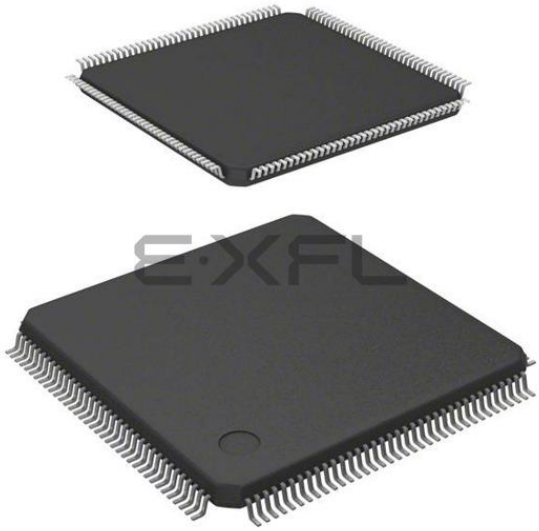

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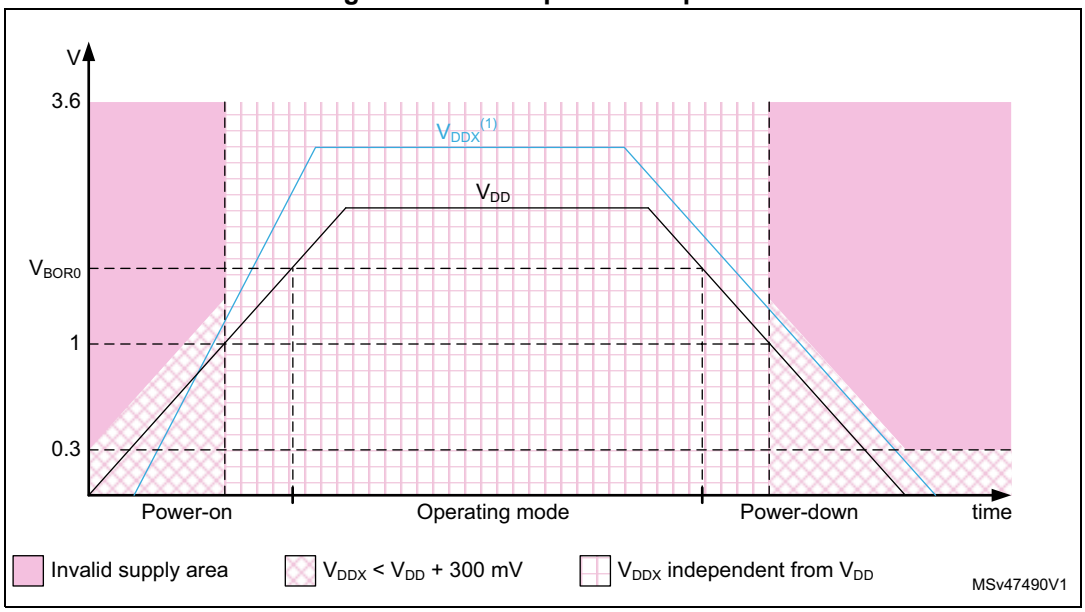
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 112 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s9zit6 |

**Figure 5. Power-up/down sequence**




1. $V_{DDX}$ refers to any power supply among $V_{DDA}$, $V_{DDIO2}$, $V_{DDUSB}$ and $V_{LCD}$.

### 3.10.2 Power supply supervisor

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage $V_{DD}$ is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the VPVD threshold.

An interrupt can be generated when $V_{DD}$ drops below the VPVD threshold and/or when $V_{DD}$ is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages $V_{DDA}$, $V_{DDUSB}$, $V_{DDIO2}$ with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

### 3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes SRAM2 in standby with RAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 120 MHz.

## 3.15 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

## 3.16 Chrom-ART Accelerator™ (DMA2D)

Chrom-ART Accelerator™ (DMA2D) is a graphic accelerator that offers an advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4 bpp color mode up to 32 bpp direct color. It embeds a dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

## 3.17 Chrom-GRC™ (GFXMMU)

The Chrom-GRC™ (GFXMMU) is a graphical oriented memory management unit aimed to:

- Optimize memory usage according to the display shape
- Manage packing/unpacking for 24 bpp frame buffers

The Chrom-GRC™ features:

- Fully programmable display shape to physically store only the visible pixel
- Up to four virtual buffers
- Each virtual buffer have 4096 bytes per line and 1024 lines
- Each virtual buffer can be physically mapped to any system memory
- 24 bpp packing unit to store unpacked 24bpp data in a packed 24 bpp
- Packing/un-packing management per buffer
- Interrupt in case of buffer overflow (1 per buffer)
- Interrupt in case of memory transfer error

**Table 15. STM32L4Sxxx pin definitions**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| - | - | - | - | M11 | - | - | - | - | M11 | VSS | S | - | - | - | - |
| - | - | - | - | C1 | - | - | - | - | C1 | VDD | S | - | - | - | - |
| - | - | - | - | C3 | - | - | - | - | C3 | PI11 | I/O | FT | - | OCTOSPIM_P2_IO0, EVENTOUT | - |
| 1 | B2 | 1 | B11 | D3 | 1 | 1 | C3 | B11 | D3 | PE2 | I/O | FT_l | - | TRACECK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, LCD_R0, FMC_A23, SAI1_MCLK_A, EVENTOUT | - |
| 2 | A1 | 2 | C11 | D2 | 2 | 2 | B3 | C11 | D2 | PE3 | I/O | FT_l | - | TRACED0, TIM3_CH1, OCTOSPIM_P1_DQS, TSC_G7_IO2, LCD_R1, FMC_A19, SAI1_SD_B, EVENTOUT | - |
| 3 | B1 | 3 | C12 | D1 | 3 | 3 | D3 | C12 | D1 | PE4 | I/O | FT | - | TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, LCD_B0, FMC_A20, SAI1_FS_A, EVENTOUT | - |
| 4 | C2 | 4 | D9 | E4 | 4 | 4 | C2 | D9 | E4 | PE5 | I/O | FT | - | TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, LCD_G0, FMC_A21, SAI1_SCK_A, EVENTOUT | - |
| 5 | D2 | 5 | D10 | E3 | 5 | 5 | D4 | D10 | E3 | PE6 | I/O | FT | - | TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7, LCD_G1, FMC_A22, SAI1_SD_A, EVENTOUT | RTC_TAMP3, WKUP3 |
| 6 | E2 | 6 | E10 | E2 | 6 | 6 | B1 | E10 | E2 | VBAT | S | - | - | - | - |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 18 | K2 | 29 | J10 | K1 | 18 | 27 | J3 | J10 | K1 | PC3 | I/O | FT_a | - | LPTIM1_ETR, SAI1_D1, SPI2_MOSI, OCTOSPIM_P1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT | ADC1_IN4 |
| 19 | - | 30 | - | - | - | - | - | - | - | VSSA | S | - | - | - | - |
| 20 | - | 31 | - | - | - | - | - | - | - | VREF- | S | - | - | - | - |
| - | J1 | - | K11 | K2 | 19 | 28 | K1 | K11 | K2 | VSSA/VREF- | S | - | - | - | - |
| 21 | L1 | 32 | L11 | L1 | - | 29 | K2 | L11 | L1 | VREF+ | S | - | - | - | VREFBUF_OUT |
| 22 | M1 | 33 | L12 | L2 | - | 30 | L1 | L12 | L2 | VDDA | S | - | - | - | - |
| - | - | - | - | - | 20 | - | - | - | - | VDDA/VREF+ | S | - | - | - | - |
| 23 | L2 | 34 | J9 | K3 | 21 | 31 | K3 | J9 | K3 | PA0 | I/O | FT_a | - | TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS_NSS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT | OPAMP1_VINP, ADC1_IN5, RTC_TAMP2, WKUP1 |
| - | M3 | - | - | M1 | - | - | - | - | - | OPAMP1_VINM | I | TT | - | - | - |
| 24 | M2 | 35 | K10 | N2 | 22 | 32 | L2 | K10 | M1 | PA1 | I/O | FT_la | - | TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, OCTOSPIM_P1_DQS, TIM15_CH1N, EVENTOUT | OPAMP1_VINM, ADC1_IN6 |
| 25 | K3 | 36 | H8 | N1 | 23 | 33 | L3 | H8 | N1 | PA2 | I/O | FT_la | - | TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, OCTOSPIM_P1_NCS, SAI2_EXTCLK, TIM15_CH1, EVENTOUT | ADC1_IN7, WKUP4/LSCO |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 90 | A7 | 134 | C8 | A5 | 92 | 134 | A5 | C8 | A5 | PB4 (NJTRST) | I/O | FT_fa | (4) | NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS_NSS, UART5_RTS_DE, TSC_G2_IO1, DCMI_D12, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT | COMP2_INP |
| 91 | C5 | 135 | E8 | B5 | 93 | 135 | B5 | E8 | B5 | PB5 | I/O | FT_la | - | LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT | - |
| 92 | B5 | 136 | C9 | C5 | 94 | 136 | D5 | C9 | C5 | PB6 | I/O | FT_fa | - | LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, DFSDM1_DATIN5, USART1_TX, TSC_G2_IO3, DCMI_D5, SAI1_FS_B, TIM16_CH1N, EVENTOUT | COMP2_INP |

Table 16. Alternate function AF0 to AF7[1]

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | OTG_FS/SYS_AF | TIM1/2/5/8/LPTIM1 | TIM1/2/3/4/5 | SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1 | I2C1/2/3/4/DCMI | SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2 | SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2 | USART1/2/3 |
| Port A | PA0 | - | TIM2_CH1 | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS_NSS |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | I2C1_SMBA | SPI1_SCK | - | USART2_RTS_DE |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | - | - | - | - | USART2_TX |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | SAI1_CK1 | - | - | - | USART2_RX |
| | PA4 | - | - | - | OCTOSPIM_P1_NCS | - | SPI1_NSS | SPI3_NSS | USART2_CK |
| | PA5 | - | TIM2_CH1 | TIM2_ETR | TIM8_CH1N | - | SPI1_SCK | - | - |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | DCMI_PIXCLK | SPI1_MISO | - | USART3_CTS_NSS |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | I2C3_SCL | SPI1_MOSI | - | - |
| | PA8 | MCO | TIM1_CH1 | - | SAI1_CK2 | - | - | - | USART1_CK |
| | PA9 | - | TIM1_CH2 | - | SPI2_SCK | - | DCMI_D0 | - | USART1_TX |
| | PA10 | - | TIM1_CH3 | - | SAI1_D1 | - | DCMI_D1 | - | USART1_RX |
| | PA11 | - | TIM1_CH4 | TIM1_BKIN2 | - | - | SPI1_MISO | - | USART1_CTS_NSS |
| | PA12 | - | TIM1_ETR | - | - | - | SPI1_MOSI | - | USART1_RTS_DE |
| | PA13 | JTMS/SWDIO | IR_OUT | - | - | - | - | - | - |
| | PA14 | JTCK/SWCLK | LPTIM1_OUT | - | - | I2C1_SMBA | I2C4_SMBA | - | - |
| | PA15 | JTDI | TIM2_CH1 | TIM2_ETR | USART2_RX | - | SPI1_NSS | SPI3_NSS | USART3_RTS_DE |

**Table 41. Current consumption in Shutdown mode (continued)**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{DD}$ | 25°C | 55°C | 85°C | 105°C | 125°C | 25°C | 55°C | 85°C | 105°C | 125°C | |
| $I_{DD}$ (Shutdown with RTC) | Supply current in Shutdown mode (backup registers retained) RTC enabled | RTC clocked by LSE bypassed at 32768 Hz | 1.8 V | 245 | 420 | 1450 | 3850 | 10500 | - | - | - | - | - | nA |
| | | | 2.4 V | 340 | 555 | 1750 | 4600 | 12500 | - | - | - | - | - | |
| | | | 3 V | 465 | 730 | 2250 | 5900 | 15500 | - | - | - | - | - | |
| | | | 3.6 V | 615 | 945 | 2850 | 7250 | 19000 | - | - | - | - | - | |
| | | RTC clocked by LSE quartz(2) in low drive mode | 1.8 V | 335 | 520 | 1550 | 4000 | - | - | - | - | - | - | |
| | | | 2.4 V | 435 | 650 | 1850 | 4750 | - | - | - | - | - | - | |
| | | | 3 V | 560 | 830 | 2350 | 6050 | - | - | - | - | - | - | |
| | | | 3.6 V | 730 | 1050 | 2950 | 7400 | - | - | - | - | - | - | |
| $I_{DD}$(wakeup from Shutdown) | Supply current during wakeup from Shutdown mode | Wakeup clock is MSI = 4 MHz(3) | 3 V | 0.5 | - | - | - | - | - | - | - | - | - | mA |

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 44: Low-power mode wakeup timings*.

**Table 43. Peripheral current consumption (continued)**

| Peripheral | | Range 1 Boost Mode | Range 1 Normal Mode | Range 2 | Low-power run and sleep | Unit |
|---|---|---|---|---|---|---|
| AHB (Cont.) | GPIOI | 1.6 | 1.4 | 1.25 | 2 | µA/MHz |
| | HASH1 | 2.6 | 2.4 | 2 | 3 | |
| | OTG_FS independent clock domain | 25.5 | 28 | NA | NA | |
| | OTG_FS AHB clock domain | 18 | 16.5 | NA | NA | |
| | OSPIM independent clock domain | 0.15 | 0.115 | 0.084 | 0.5 | |
| | OSPIM AHB clock domain | 0.665 | 0.625 | 0.54 | 1 | |
| | OSPI1 independent clock domain | 2.5 | 2.4 | 2.1 | 2.5 | |
| | OSPI1 AHB clock domain | 6.15 | 5.75 | 4.6 | 5.5 | |
| | OSPI2 independent clock domain | 1.9 | 1.65 | 1.25 | 1 | |
| | OSPI2 AHB clock domain | 5.5 | 5.25 | 4.15 | 5.5 | |
| | RNG independent clock domain | 3.9 | 4.25 | NA | NA | |
| | RNG AHB clock domain | 2.65 | 2.5 | NA | NA | |
| | SDMMC1 independent clock domain | 24.5 | 23.5 | NA | NA | |
| | SDMMC1 AHB clock domain | 23.5 | 22 | NA | NA | |
| | SRAM1 | 2.65 | 2.65 | 2.1 | 2 | |
| | SRAM2 | 2.25 | 2 | 1.75 | 2 | |
| | SRAM3 | 5.35 | 5 | 4.25 | 5.5 | |
| | TSC | 1.85 | 1.75 | 1.65 | 1 | |
| | All AHB Peripherals | 165 | 150 | 125 | 145 | |
| APB1 | AHB to APB1 bridge | 0.084 | 0.25 | 0.165 | 0.5 | µA/MHz |
| | CAN1 | 4.85 | 4.5 | 3.75 | 4.5 | |
| | CRS | 0.335 | 0.25 | 0.415 | 0.5 | |
| | DAC1 | 2.75 | 2.5 | 2.1 | 2.5 | |
| | I2C1 independent clock domain | 3.75 | 3.4 | 2.9 | 2.5 | |

**Table 44. Low-power mode wakeup timings(1) (continued)**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{WUSTBY}$ | Wakeup time from Standby mode to Run mode | Range 1 | Wakeup clock MSI = 8 MHz | 30.7 | 47.8 | µs |
| | | | Wakeup clock MSI = 4 MHz | 40.4 | 55.6 | |
| $t_{WUSTBY\ SRAM2}$ | Wakeup time from Standby with SRAM2 to Run mode | Range 1 | Wakeup clock MSI = 8 MHz | 32.1 | 49.1 | |
| | | | Wakeup clock MSI = 4 MHz | 41.5 | 55.5 | |
| $t_{WUSHDN}$ | Wakeup time from Shutdown mode to Run mode | Range 1 | Wakeup clock MSI = 4 MHz | 265.0 | 339.4 | |

1. Guaranteed by characterization results.

**Table 45. Regulator modes transition times(1)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WULPRUN}$ | Wakeup time from Low- power run mode to Run mode(2) | Code run with MSI 2 MHz | 5 | 7 | µs |
| $t_{VOST}$ | Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3) | Code run with MSI 24 MHz | 20 | 40 | |

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

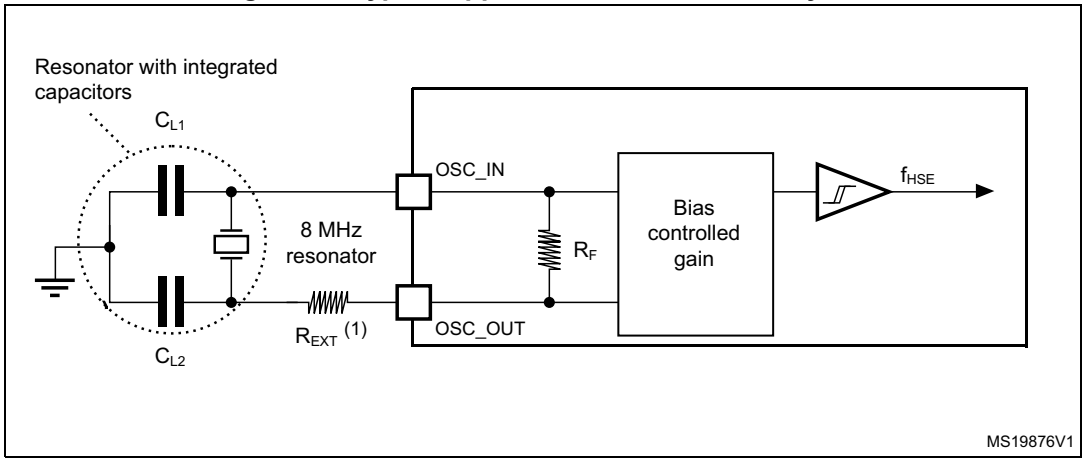
**Table 46. Wakeup time using USART/LPUART(1)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUUSART}$ $t_{WULPUART}$ | Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI | Stop mode 0 | - | 1.7 | µs |
| | | Stop mode 1/2 | - | 8.5 | |

1. Guaranteed by characterization results.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 26. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 50*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 19: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 19: Voltage characteristics*).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

**Table 68. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$-0.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 1.3 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$-1.3 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V | - | 0.45 | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$-0.45 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx}$ ≥ 1.08 V | - | 0.35 x $V_{DDIOx}$ | |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | 0.65x$V_{DDIOx}$ | - | |
| $V_{OLFM+}$(3) | Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option) | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | |
| | | $\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V | - | 0.4 | |
| | | $\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx}$ ≥ 1.08 V | - | 0.4 | |

1. The $I_{IO}$ current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{IO}$.

**Table 78. ADC accuracy - limited test conditions 4(1)(2)(3)**

| Sym-bol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ET | Total unadjusted error | ADC clock frequency ≤ 26 MHz, 1.65 V ≤ $V_{DDA}$ = VREF+ ≤ 3.6 V, Voltage scaling Range 2 | Single ended | Fast channel (max speed) | - | 5 | 5.4 | LSB |
| | | | | Slow channel (max speed) | - | 4 | 5 | |
| | | | Differential | Fast channel (max speed) | - | 4 | 5 | |
| | | | | Slow channel (max speed) | - | 3.5 | 4.5 | |
| EO | Offset error | | Single ended | Fast channel (max speed) | - | 2 | 4 | |
| | | | | Slow channel (max speed) | - | 2 | 4 | |
| | | | Differential | Fast channel (max speed) | - | 2 | 3.5 | |
| | | | | Slow channel (max speed) | - | 2 | 3.5 | |
| EG | Gain error | | Single ended | Fast channel (max speed) | - | 4 | 4.5 | |
| | | | | Slow channel (max speed) | - | 4 | 4.5 | |
| | | | Differential | Fast channel (max speed) | - | 3 | 4 | |
| | | | | Slow channel (max speed) | - | 3 | 4 | |
| ED | Differential linearity error | | Single ended | Fast channel (max speed) | - | 1 | 1.5 | |
| | | | | Slow channel (max speed) | - | 1 | 1.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 1.2 | |
| | | | | Slow channel (max speed) | - | 1 | 1.2 | |
| EL | Integral linearity error | | Single ended | Fast channel (max speed) | - | 2.5 | 3 | |
| | | | | Slow channel (max speed) | - | 2.5 | 3 | |
| | | | Differential | Fast channel (max speed) | - | 2 | 2.5 | |
| | | | | Slow channel (max speed) | - | 2 | 2.5 | |
| ENOB | Effective number of bits | | Single ended | Fast channel (max speed) | 10.2 | 10.5 | - | bits |
| | | | | Slow channel (max speed) | 10.2 | 10.5 | - | |
| | | | Differential | Fast channel (max speed) | 10.6 | 10.7 | - | |
| | | | | Slow channel (max speed) | 10.6 | 10.7 | - | |
| SINAD | Signal-to-noise and distortion ratio | | Single ended | Fast channel (max speed) | 63 | 65 | - | dB |
| | | | | Slow channel (max speed) | 63 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 65 | 66 | - | |
| | | | | Slow channel (max speed) | 65 | 66 | - | |
| SNR | Signal-to-noise ratio | | Single ended | Fast channel (max speed) | 64 | 65 | - | |
| | | | | Slow channel (max speed) | 64 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 66 | 67 | - | |
| | | | | Slow channel (max speed) | 66 | 67 | - | |

### 6.3.26 Temperature sensor characteristics

**Table 84. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{TS}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(2) | Average slope | 2.3 | 2.5 | 2.7 | mV/°C |
| $V_{30}$ | Voltage at 30°C (±5 °C)(3) | 0.742 | 0.76 | 0.785 | V |
| $t_{START}$ (TS_BUF)(1) | Sensor Buffer Start-up time in continuous mode(4) | - | 8 | 15 | µs |
| $t_{START}$(1) | Start-up time when entering in continuous mode(4) | - | 70 | 120 | µs |
| $t_{S\_temp}$(1) | ADC sampling time when reading the temperature | 5 | - | - | µs |
| $I_{DD}$(TS)(1) | Temperature sensor consumption from $V_{DD}$, when selected by ADC | - | 4.7 | 7 | µA |

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at $V_{DDA}$ = 3.0 V ±10 mV. The $V_{30}$ ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

### 6.3.27 $V_{BAT}$ monitoring characteristics

**Table 85. $V_{BAT}$ monitoring characteristics**

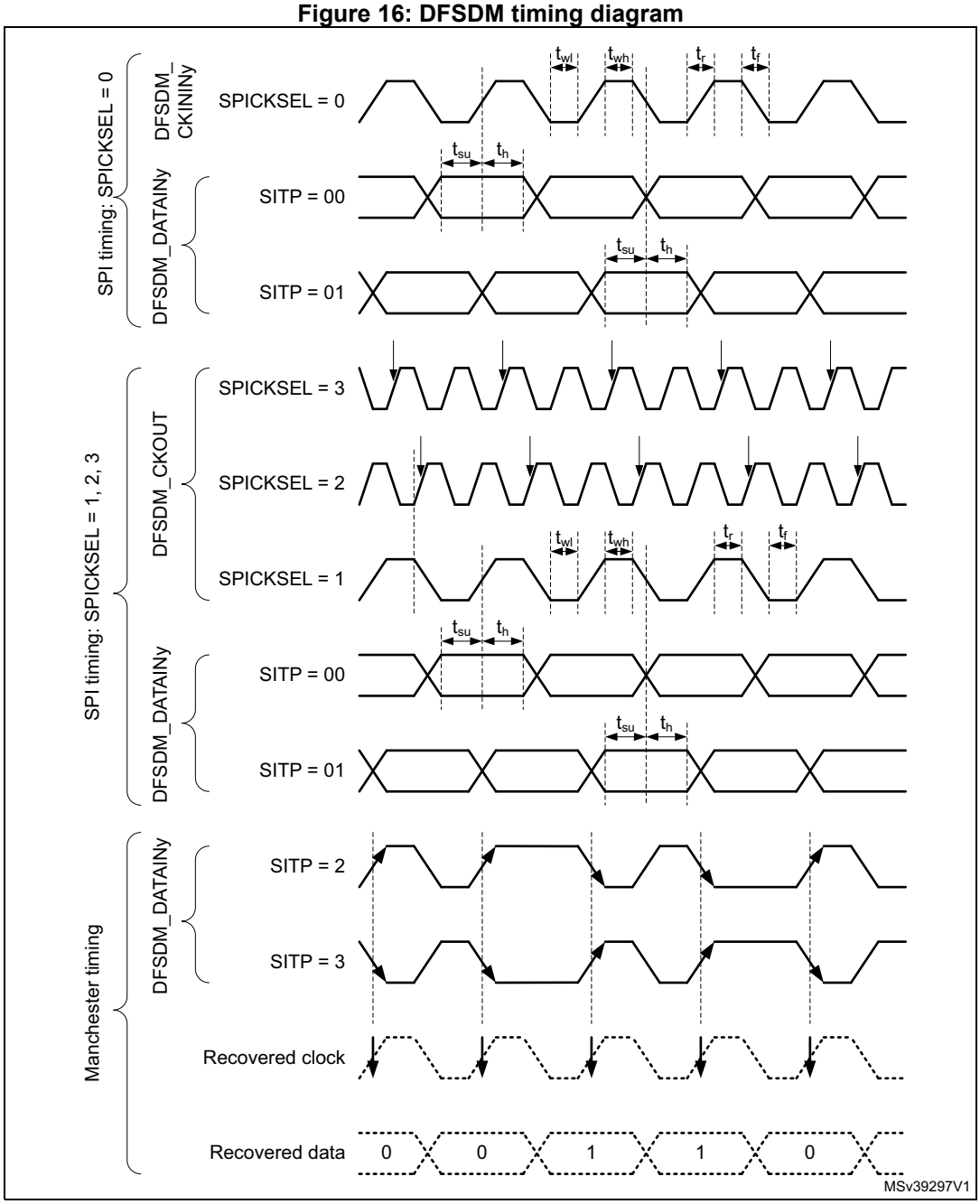
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 39 | - | kΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 3 | - | - |
| Er(1) | Error on Q | -10 | - | 10 | % |
| $t_{S\_vbat}$(1) | ADC sampling time when reading the VBAT | 12 | - | - | µs |

1. Guaranteed by design.

**Table 86. $V_{BAT}$ charging characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{BC}$ | Battery charging resistor | VBRS = 0 | - | 5 | - | kΩ |
| | | VBRS = 1 | - | 1.5 | - | |

**Figure 16: DFSDM timing diagram**




## 6.3.29 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.17: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 93* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x $V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

**Table 96. USB BCD DC electrical characteristics(1) (continued)**

| Driver characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| VLGC | Logic threshold | - | 0.8 | - | 2.0 | V |
| VDAT_REF | Data detect voltage | - | 0.25 | - | 0.4 | V |
| VDP_SRC | D+ source voltage | - | 0.5 | - | 0.7 | V |
| VDM_SRC | D- source voltage | - | 0.5 | - | 0.7 | V |
| IDP_SINK | D+ sink current | - | 25 | - | 175 | µA |
| IDM_SINK | D- sink current | - | 25 | - | 175 | µA |

1. Guaranteed by design

### CAN (controller area network) interface

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

## 6.3.31 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 97* to *Table 110* for the FMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x $V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

### Asynchronous waveforms and timings

*Figure 45* through *Figure 48* represent asynchronous waveforms and *Table 97* through *Table 104* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

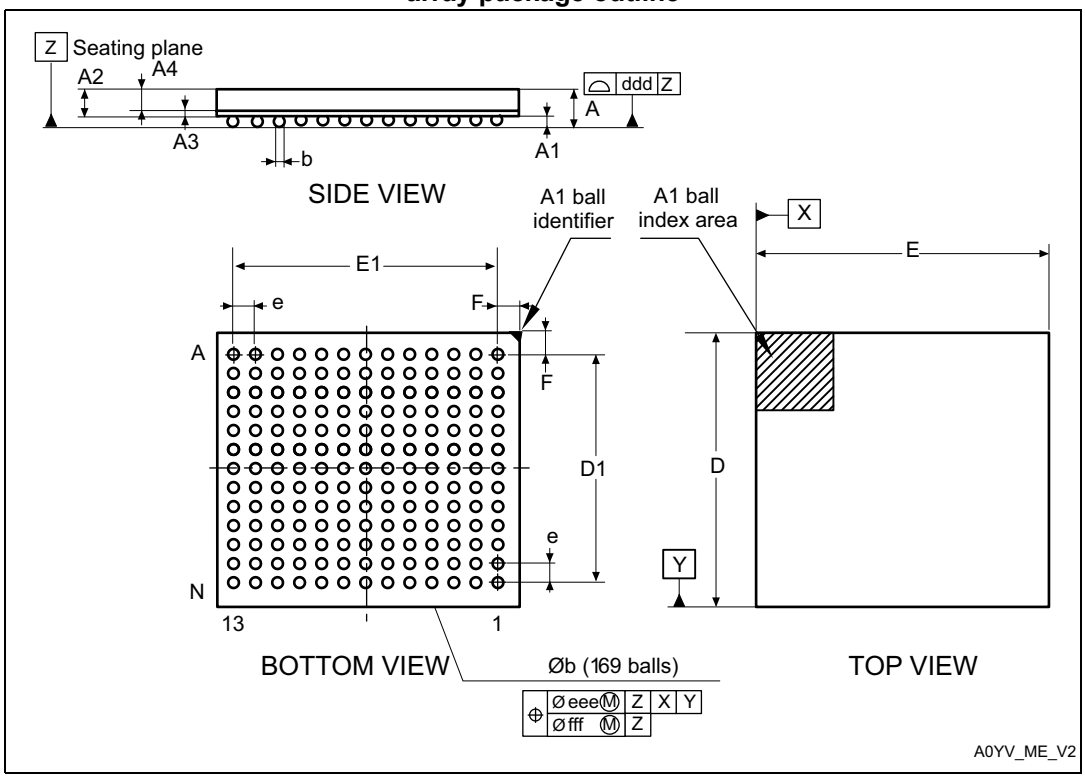
In all timing tables, the THCLK is the HCLK clock period.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 UFBGA169 package information

**Figure 67. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 118. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data**

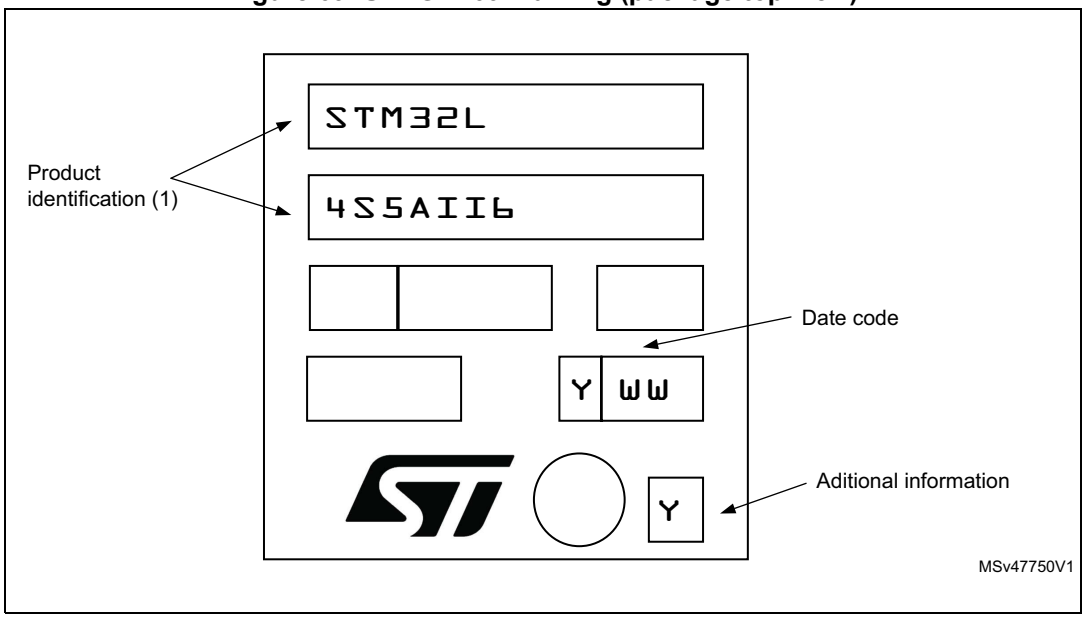
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | - | 0.130 | - | - | 0.0051 | - |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |

### UFBGA169 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 69. UFBGA169 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.