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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 112 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-UFBGA, WLCSP |
| Supplier Device Package | 144-WLCSP (5.24x5.24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4s9ziy6tr |

**Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts (continued)**

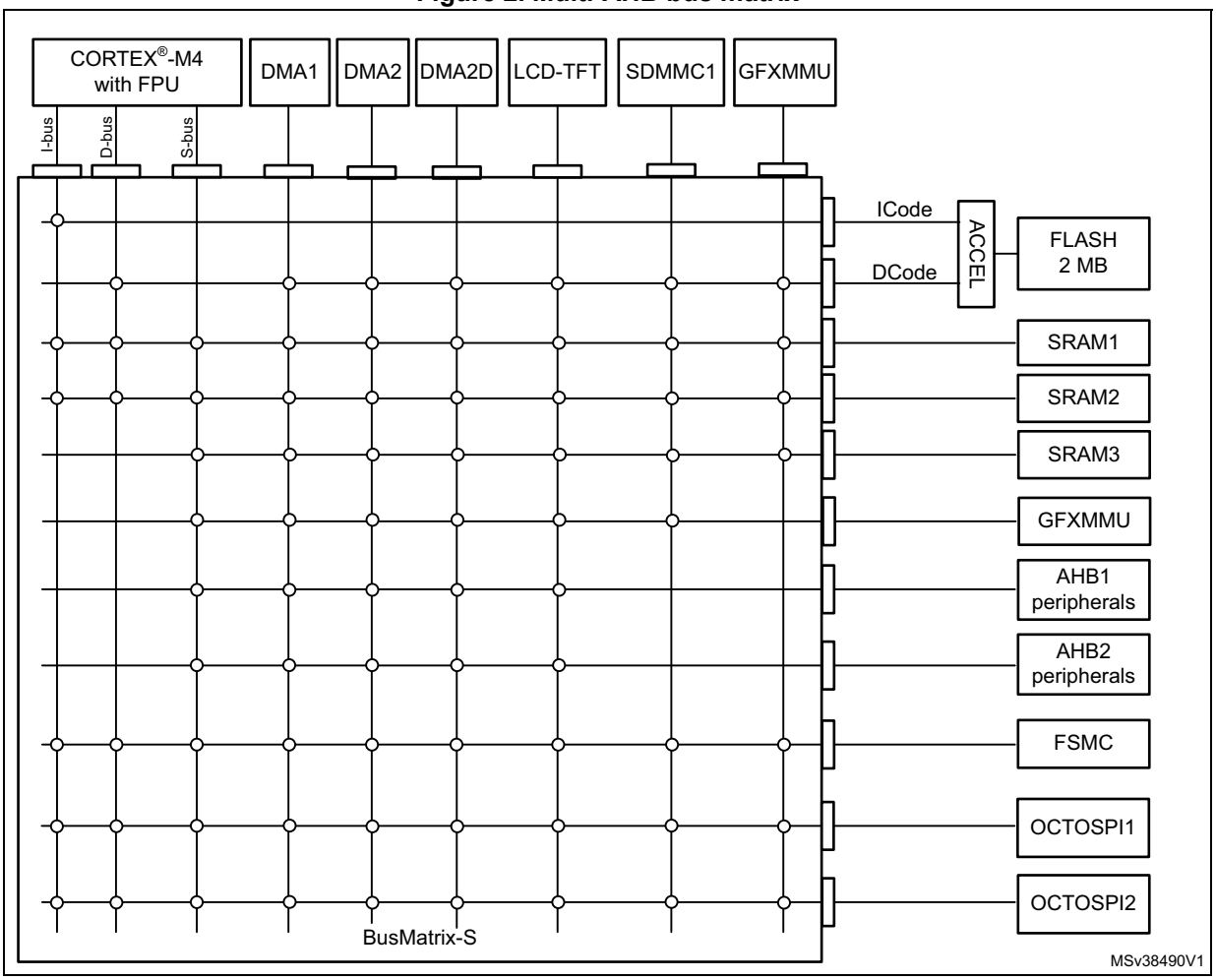
| Peripheral | S5VI | S7VI | S9VI | S5QI | S5ZI | S7ZI | S9ZI | S5AI | S7AI | S9AI |
|---|---|---|---|---|---|---|---|---|---|---|
| LCD - TFT | No | Yes | | No | | Yes | | No | Yes | |
| MIPI DSI Host(2) | No | | Yes | No | | | Yes | No | | Yes |
| Random number generator | Yes | | | | | | | | | |
| AES + HASH | Yes | | | | | | | | | |
| GPIOs<br>Wakeup pins<br>Nb of I/Os down to 1.08 V | 83<br>5<br>0 | | 77<br>4<br>0 | 110<br>5<br>14 | 115<br>5<br>14 | | 112<br>5<br>11 | 140<br>5<br>14 | | 131<br>4<br>13 |
| Capacitive sensing<br>Number of channels | 21 | | 18 | 24 | | | | | | |
| 12-bit ADCs<br>Number of channels | 1 | | | | | | | | | |
| | 16 | | 14 | 16 | | | | | | 14 |
| 12-bit DAC<br>Number of channels | 2<br>2 | | | | | | | | | |
| Internal voltage reference buffer | Yes | | | | | | | | | |
| Analog comparator | 2 | | | | | | | | | |
| Operational amplifiers | 2 | | | | | | | | | |
| Max. CPU frequency | 120 MHz | | | | | | | | | |
| Operating voltage | 1.71 to 3.6 V | | | | | | | | | |
| Operating temperature | Ambient operating temperature: -40 to 85 °C / -40 to 125 °C | | | | | | | | | |
| Packages | LQFP100 | | | UFBGA 132 | LQFP 144 WLCSP144 | LQFP 144 | LQFP 144, UFBGA 144 WLCSP 144 | UFBGA169 | | |
| Bootloader | USART 1 | USART 2 | USART 3 | SPI1 | SPI2 | I2C1 | I2C2 | I2C3 | CAN1 | USB through DFU |

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4S9xx sales types.

## 3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, DMA2D, SDMMC1, LCD-TFT and GFXMMU) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 2. Multi-AHB bus matrix**

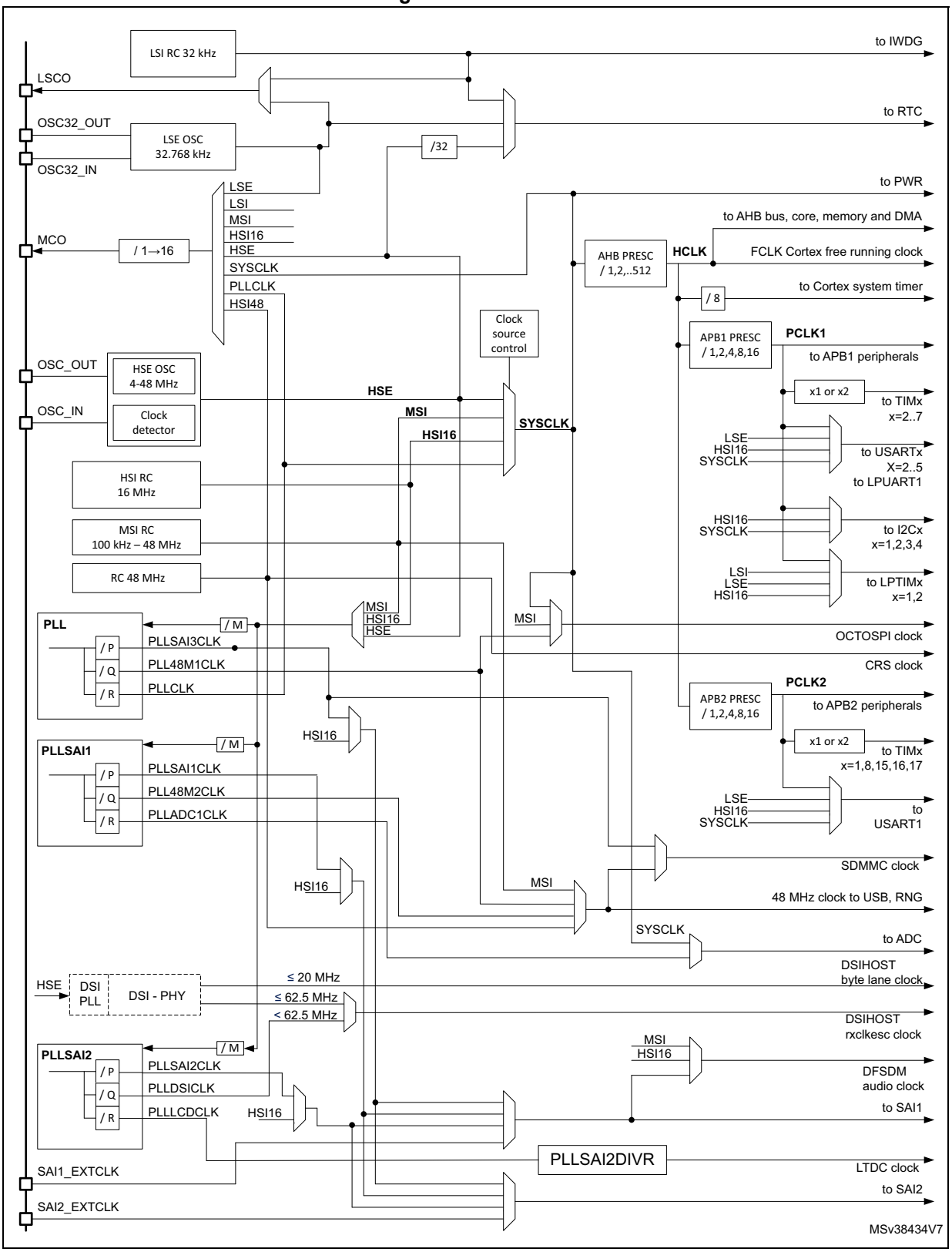



## 3.7 Firewall

These devices embed a firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

**Figure 6. Clock tree**



## 3.25 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- Two displays layers with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

## 3.26 DSI Host (DSIHOST)

The DSI Host is a dedicated IP that interfaces with the MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

The interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI)
  - Used to transmit information in full bandwidth in the Adapted Command Mode (DBI) through a custom mode
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli

**Table 10. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1, TIM8 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General-purpose | TIM2, TIM5 | 32-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM3, TIM4 | 16-bit | Up, down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.32.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

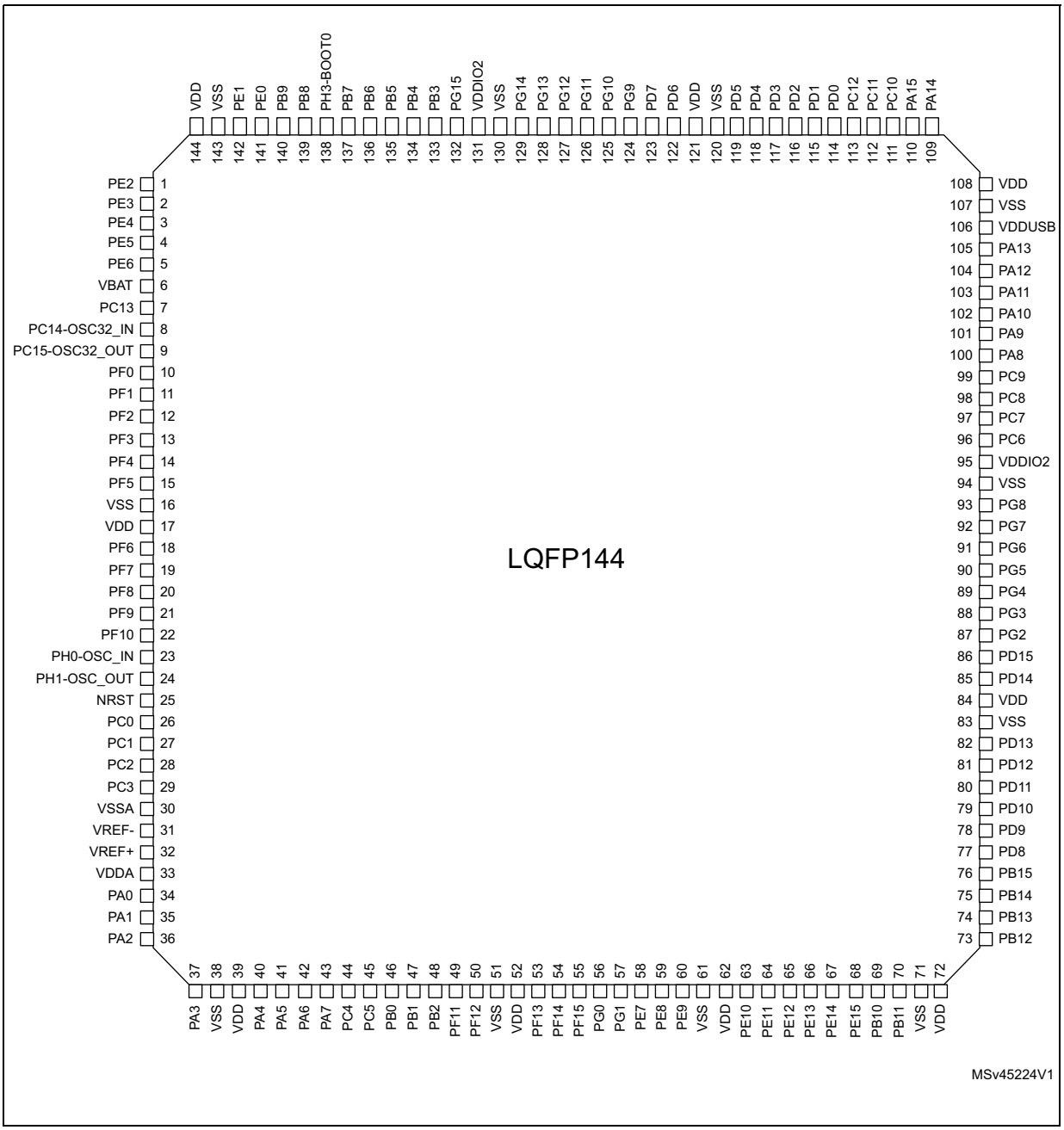
The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

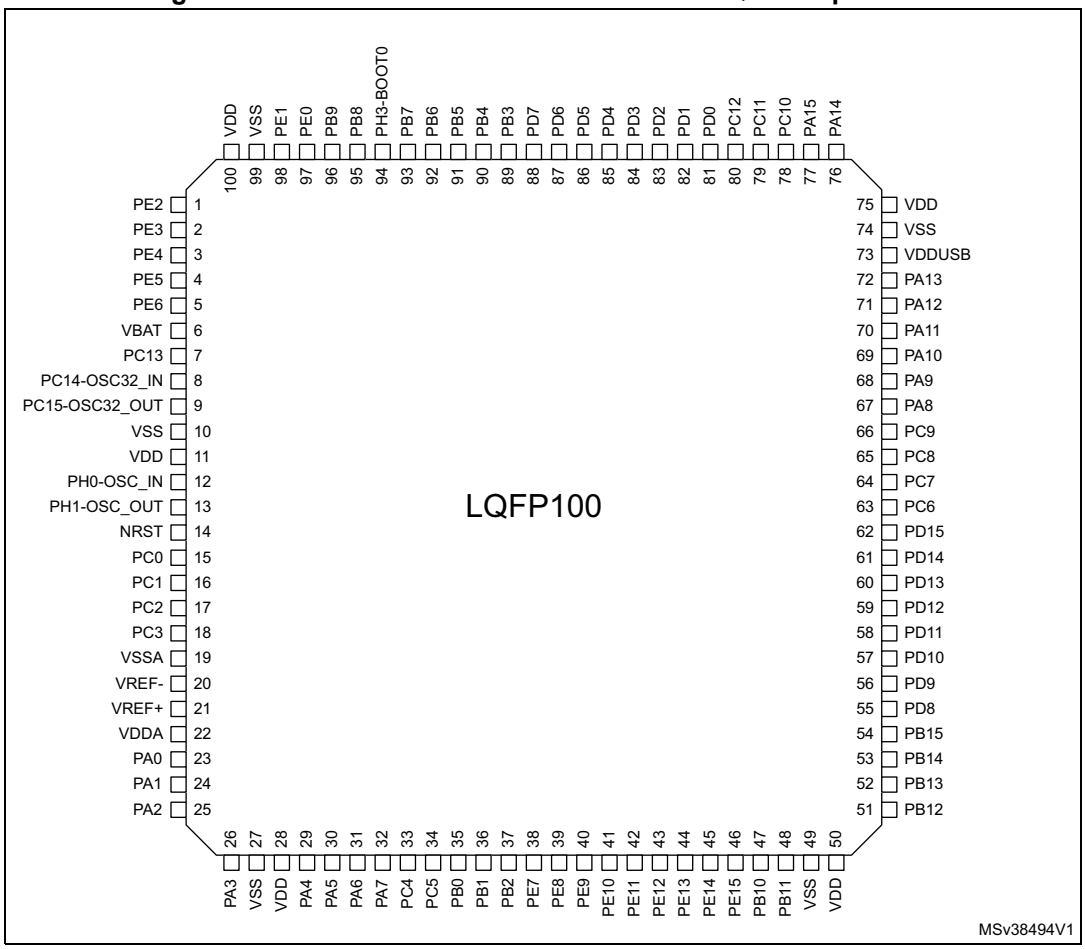
Many features are shared with the general-purpose TIMx timers (described in *Section 3.32.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

**Figure 10. STM32L4S5xx and STM32L4S7xx LQFP144 pinout(1)**




1. The above figure shows the package top view.

**Figure 16. STM32L4S5xx and STM32L4S7xx LQFP100 pinout(1)**




1. The above figure shows the package top view.

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 42 | M9 | 64 | L5 | N8 | 39 | 60 | H7 | L5 | N8 | PE11 | I/O | FT | - | TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT | - |
| 43 | L9 | 65 | M5 | M8 | 40 | 61 | M9 | M5 | M8 | PE12 | I/O | FT | - | TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, OCTOSPIM_1_IO0, LCD_G5, FMC_D9, EVENTOUT | - |
| 44 | M10 | 66 | J5 | L8 | 41 | 62 | J8 | J5 | L8 | PE13 | I/O | FT | - | TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT | - |
| 45 | M11 | 67 | H5 | K8 | 42 | 63 | M10 | H5 | K7 | PE14 | I/O | FT | - | TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPIM_P1_IO2, LCD_G7, FMC_D11, EVENTOUT | - |
| 46 | M12 | 68 | K4 | J8 | 43 | 64 | K8 | K4 | J7 | PE15 | I/O | FT | - | TIM1_BKIN, SPI1_MOSI, OCTOSPIM_P1_IO3, LCD_R2, FMC_D12, EVENTOUT | - |
| 47 | L10 | 69 | L4 | N9 | 44 | 65 | L9 | L4 | N9 | PB10 | I/O | FT_fl | - | TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPIM_P1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT | - |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| - | - | - | - | - | 59 | 80 | - | - | - | VDD12DSI | S | - | - | - | - |
| - | - | - | - | - | - | - | H11 | J2 | J11 | DSI_D1P | I/O | - | (3) | - | - |
| - | - | - | - | - | - | - | H12 | J1 | J12 | DSI_D1N | I/O | - | (3) | - | - |
| - | - | - | - | - | - | - | J10 | K3 | K13 | VSSDSI | S | - | - | - | - |
| - | - | - | K3 | - | - | - | - | - | - | VSS | S | - | - | - | - |
| - | - | - | L3 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | L1 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | L2 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | K1 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | K2 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | J2 | - | - | - | - | - | - | NC | - | - | - | - | - |
| - | - | - | J1 | - | - | - | - | - | - | NC | - | - | - | - | - |
| 55 | K9 | 77 | H2 | L11 | 60 | 81 | H10 | H2 | K10 | PD8 | I/O | FT | - | USART3_TX, DCMI_HSYNC, LCD_R3, FMC_D13, EVENTOUT | - |
| 56 | K8 | 78 | H1 | L10 | 61 | 82 | H9 | H1 | K9 | PD9 | I/O | FT | - | USART3_RX, DCMI_PIXCLK, LCD_R4, FMC_D14, SAI2_MCLK_A, EVENTOUT | - |
| 57 | J12 | 79 | G5 | J13 | 62 | 83 | H8 | G5 | J10 | PD10 | I/O | FT | - | USART3_CK, TSC_G6_IO1, LCD_R5, FMC_D15, SAI2_SCK_A, EVENTOUT | - |
| - | - | - | - | H13 | - | - | - | - | - | VDD | S | - | - | - | - |
| 58 | J11 | 80 | G4 | K12 | - | 84 | G11 | G4 | J9 | PD11 | I/O | FT | - | I2C4_SMBA, USART3_CTS_NSS, TSC_G6_IO2, LCD_R6, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT | - |

**Table 15. STM32L4Sxxx pin definitions (continued)**

| Pin Number | | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32L4S5xx STM32L4S7xx | | | | | STM32L4S9xx | | | | | | | | | | |
| LQFP100 | BGA132 | LQFP144 | WLCSP144 | UFBGA169 | LQFP100 | LQFP144 | UFBGA144 | WLCSP144 | UFBGA169 | | | | | | |
| 90 | A7 | 134 | C8 | A5 | 92 | 134 | A5 | C8 | A5 | PB4 (NJTRST) | I/O | FT_fa | (4) | NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS_NSS, UART5_RTS_DE, TSC_G2_IO1, DCMI_D12, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT | COMP2_INP |
| 91 | C5 | 135 | E8 | B5 | 93 | 135 | B5 | E8 | B5 | PB5 | I/O | FT_la | - | LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT | - |
| 92 | B5 | 136 | C9 | C5 | 94 | 136 | D5 | C9 | C5 | PB6 | I/O | FT_fa | - | LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, DFSDM1_DATIN5, USART1_TX, TSC_G2_IO3, DCMI_D5, SAI1_FS_B, TIM16_CH1N, EVENTOUT | COMP2_INP |

**Table 18. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx memory map and peripheral register boundary addresses(1) (continued)**

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| APB1 | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0C00- 0x4000 0FFF | 1 KB | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | 1 KB | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

1. The gray color is used for reserved boundary addresses.

**Table 29. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | | 25°C | 55°C | 85°C | 105°C | 125°C | 25°C | 55°C | 85°C | 105°C | 125°C | |
| $I_{DD}$ (Run) | Supply current in Run mode | $f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable | Range 2 | 26 MHz | 4.10 | 4.50 | 5.60 | 7.20 | 10.00 | 4.7 | 5.6 | 7.6 | 11.0 | 17.0 | mA |
| | | | | 16 MHz | 2.75 | 3.10 | 4.25 | 5.85 | 8.70 | 3.2 | 4.1 | 6.1 | 9.4 | 16.0 | |
| | | | | 8 MHz | 1.25 | 1.90 | 2.95 | 4.55 | 7.35 | 1.7 | 2.7 | 4.7 | 8.0 | 14.0 | |
| | | | | 4 MHz | 0.91 | 1.25 | 2.35 | 3.90 | 6.75 | 1.2 | 2.0 | 4.0 | 7.3 | 14.0 | |
| | | | | 2 MHz | 0.59 | 0.94 | 2.00 | 3.60 | 6.40 | 0.8 | 1.6 | 3.6 | 6.9 | 13.0 | |
| | | | | 1 MHz | 0.42 | 0.77 | 1.85 | 3.40 | 6.25 | 0.6 | 1.4 | 3.4 | 6.7 | 13.0 | |
| | | | | 100 KHz | 0.27 | 0.63 | 1.70 | 3.25 | 6.10 | 0.4 | 1.2 | 3.2 | 6.5 | 13.0 | |
| | | | Range 1 Boost Mode | 120 MHz | 17.00 | 18.00 | 19.50 | 21.50 | 25.50 | 19.0 | 21.0 | 24.0 | 28.0 | 36.0 | |
| | | | Range 1 Normal Mode | 80 MHz | 13.00 | 13.50 | 15.00 | 17.00 | 20.50 | 15.0 | 16.0 | 19.0 | 23.0 | 30.0 | |
| | | | | 72 MHz | 11.50 | 12.00 | 14.00 | 16.00 | 19.50 | 13.0 | 15.0 | 18.0 | 22.0 | 29.0 | |
| | | | | 64 MHz | 10.50 | 11.00 | 12.50 | 14.50 | 18.00 | 12.0 | 13.0 | 16.0 | 20.0 | 27.0 | |
| | | | | 48 MHz | 9.00 | 9.50 | 11.00 | 13.00 | 16.50 | 11.0 | 12.0 | 15.0 | 19.0 | 26.0 | |
| | | | | 32 MHz | 6.45 | 6.95 | 8.40 | 10.50 | 14.00 | 7.3 | 8.5 | 12.0 | 16.0 | 23.0 | |
| | | | | 24 MHz | 4.90 | 5.40 | 6.85 | 8.80 | 12.50 | 5.6 | 6.7 | 9.3 | 14.0 | 21.0 | |
| | | | | 16 MHz | 3.55 | 4.00 | 5.40 | 7.40 | 11.00 | 4.1 | 5.2 | 7.7 | 12.0 | 19.0 | |
| $I_{DD}$ (LPRun) | Supply current in Low-power run mode | $f_{HCLK} = f_{MSI}$ all peripherals disable | | 2 MHz | 590 | 1000 | 2300 | 4050 | 7200 | 800.0 | 1800 | 4200 | 7800 | 15000 | µA |
| | | | | 1 MHz | 390 | 805 | 2100 | 3850 | 7000 | 580.0 | 1600 | 4000 | 7600 | 14000 | |
| | | | | 400 KHz | 245 | 655 | 1950 | 3750 | 6900 | 420.0 | 1400 | 3800 | 7500 | 14000 | |
| | | | | 100 KHz | 195 | 610 | 1900 | 3700 | 6850 | 370.0 | 1400 | 3700 | 7500 | 14000 | |

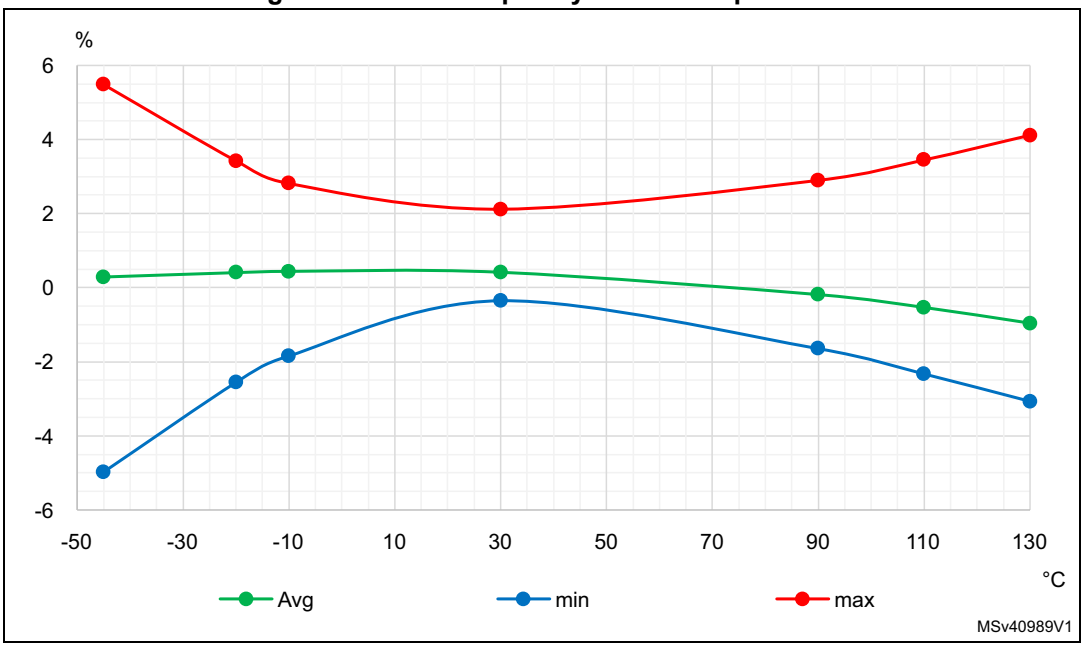
1. Guaranteed by characterization results, unless otherwise specified.

**Table 35. Current consumption in Low-power sleep mode, Flash in power-down**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | | 25°C | 55°C | 85°C | 105°C | 125°C | 25°C | 55°C | 85°C | 105°C | 125°C | |
| $I_{DD}$ (LPSleep) | Supply current in Low-power sleep mode | $f_{HCLK} = f_{MSI}$ all peripherals disable | | 2 MHz | 255 | 645 | 1950 | 3700 | 6850 | 430 | 1400 | 3700 | 7400 | 14000 | µA |
| | | | | 1 MHz | 195 | 620 | 1900 | 3700 | 6850 | 370 | 1300 | 3700 | 7400 | 14000 | |
| | | | | 400 KHz | 180 | 600 | 1900 | 3700 | 6800 | 350 | 1300 | 3700 | 7400 | 14000 | |
| | | | | 100 KHz | 175 | 595 | 1900 | 3650 | 6800 | 340 | 1300 | 3700 | 7400 | 14000 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Figure 30. HSI48 frequency versus temperature**




## Low-speed internal (LSI) RC oscillator

**Table 54. LSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | LSI Frequency | $V_{DD}$ = 3.0 V, $T_A$ = 30 °C | 31.04 | - | 32.96 | kHz |
| | | $V_{DD}$ = 1.62 to 3.6 V, $T_A$ = -40 to 125 °C | 29.5 | - | 34 | |
| $t_{SU}(LSI)^{(2)}$ | LSI oscillator start-up time | - | - | 80 | 130 | µs |
| $t_{STAB}(LSI)^{(2)}$ | LSI oscillator stabilization time | 5% of final frequency | - | 125 | 180 | µs |
| $I_{DD}(LSI)^{(2)}$ | LSI oscillator power consumption | - | - | 110 | 180 | nA |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Table 75. ADC accuracy - limited test conditions 1(1)(2)(3)**

| Sym-bol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ET | Total unadjusted error | ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA}$ = VREF+ = 3 V, TA = 25 °C | Single ended | Fast channel (max speed) | - | 4 | 5 | LSB |
| | | | | Slow channel (max speed) | - | 4 | 5 | |
| | | | Differential | Fast channel (max speed) | - | 3.5 | 4.5 | |
| | | | | Slow channel (max speed) | - | 3.5 | 4.5 | |
| EO | Offset error | | Single ended | Fast channel (max speed) | - | 1 | 2.5 | |
| | | | | Slow channel (max speed) | - | 1 | 2.5 | |
| | | | Differential | Fast channel (max speed) | - | 1.5 | 2.5 | |
| | | | | Slow channel (max speed) | - | 1.5 | 2.5 | |
| EG | Gain error | | Single ended | Fast channel (max speed) | - | 2.5 | 4.5 | |
| | | | | Slow channel (max speed) | - | 2.5 | 4.5 | |
| | | | Differential | Fast channel (max speed) | - | 2.5 | 3.5 | |
| | | | | Slow channel (max speed) | - | 2.5 | 3.5 | |
| ED | Differential linearity error | | Single ended | Fast channel (max speed) | - | 1 | 1.5 | |
| | | | | Slow channel (max speed) | - | 1 | 1.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 1.2 | |
| | | | | Slow channel (max speed) | - | 1 | 1.2 | |
| EL | Integral linearity error | | Single ended | Fast channel (max speed) | - | 1.5 | 2.5 | |
| | | | | Slow channel (max speed) | - | 1.5 | 2.5 | |
| | | | Differential | Fast channel (max speed) | - | 1 | 2 | |
| | | | | Slow channel (max speed) | - | 1 | 2 | |
| ENOB | Effective number of bits | | Single ended | Fast channel (max speed) | 10.4 | 10.5 | - | bits |
| | | | | Slow channel (max speed) | 10.4 | 10.5 | - | |
| | | | Differential | Fast channel (max speed) | 10.8 | 10.9 | - | |
| | | | | Slow channel (max speed) | 10.8 | 10.9 | - | |
| SINAD | Signal-to-noise and distortion ratio | | Single ended | Fast channel (max speed) | 64.4 | 65 | - | dB |
| | | | | Slow channel (max speed) | 64.4 | 65 | - | |
| | | | Differential | Fast channel (max speed) | 66.8 | 67.4 | - | |
| | | | | Slow channel (max speed) | 66.8 | 67.4 | - | |
| SNR | Signal-to-noise ratio | | Single ended | Fast channel (max speed) | 65 | 66 | - | |
| | | | | Slow channel (max speed) | 65 | 66 | - | |
| | | | Differential | Fast channel (max speed) | 67 | 68 | - | |
| | | | | Slow channel (max speed) | 67 | 68 | - | |

**Table 92. SPI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 9 | - | 16 | ns |
| $t_{v(SO)}$ | Data output valid time | Slave mode<br>2.7 V < $V_{DD}$ < 3.6 V<br>Voltage Range V1 | - | 13 | 15 | ns |
| | | Slave mode<br>1.71 V < $V_{DD}$ < 3.6 V<br>Voltage Range V1 | - | 10 | 23 | |
| | | Slave mode<br>1.71 V < $V_{DD}$ < 3.6 V<br>Voltage Range V2 | - | 13 | 25 | |
| | | Slave mode<br>1.08 V < $V_{DD}$ < 1.32 V(3) | - | 29 | 39 | |
| $t_{v(MO)}$ | | Master mode | - | 2 | 4 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode 1.71 V < $V_{DD}$ < 3.6 V | 7 | - | - | |
| | | Slave mode 1.08 < $V_{DD}$ < 1.32 V(3) | 26 | - | - | |
| $t_{h(MO)}$ | | Master mode | 1 | - | - | |

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.
3. SPI mapped on Port G.

**Figure 39. SPI timing diagram - slave mode and CPHA = 0**

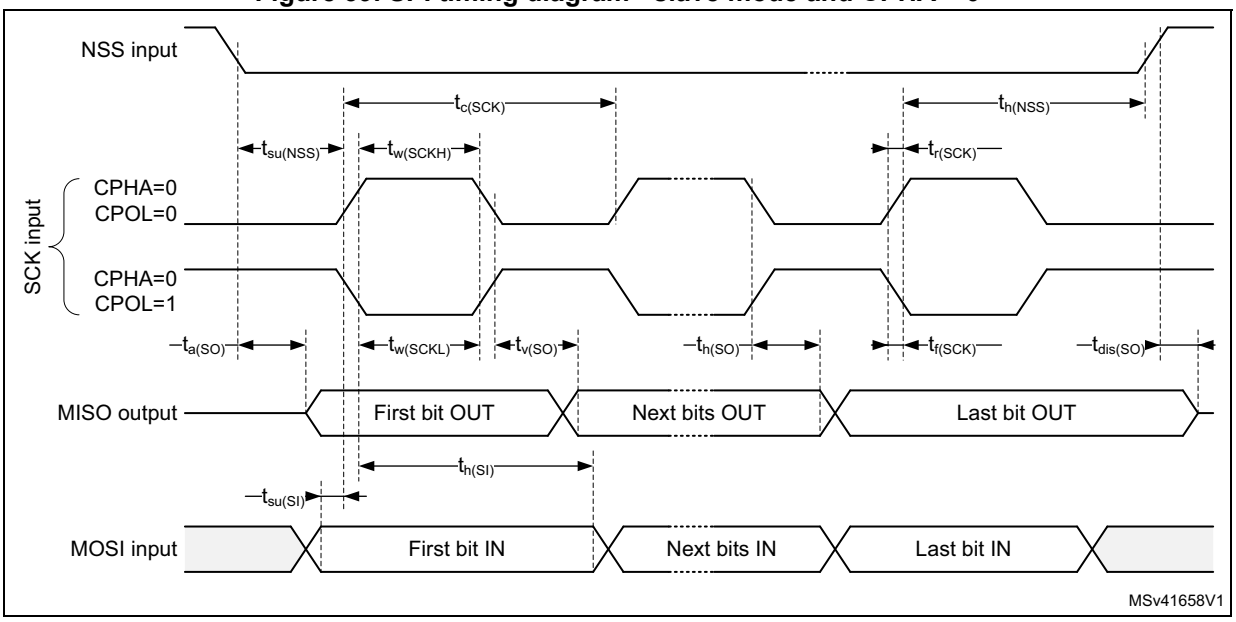


**Figure 53. NAND controller waveforms for read access**

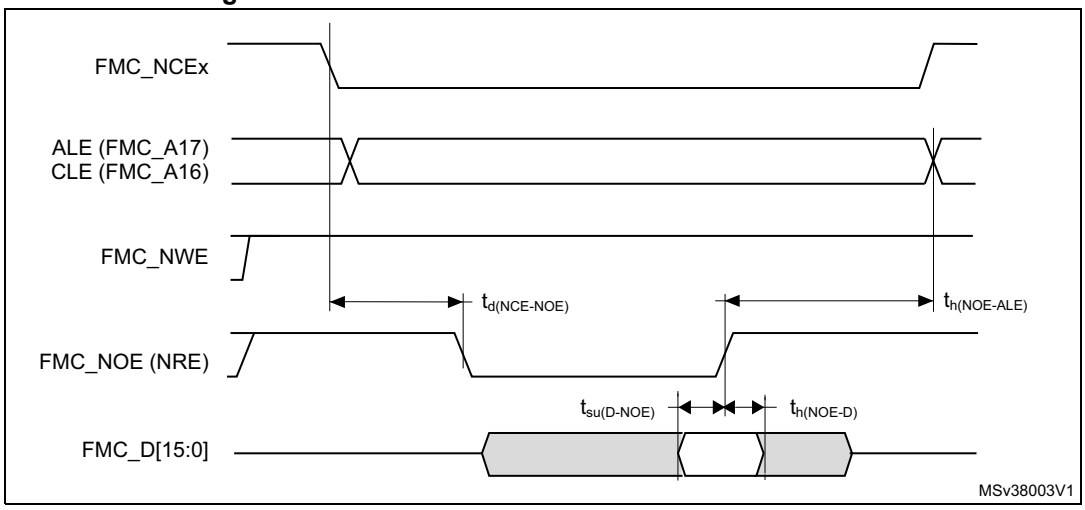



**Figure 54. NAND controller waveforms for write access**

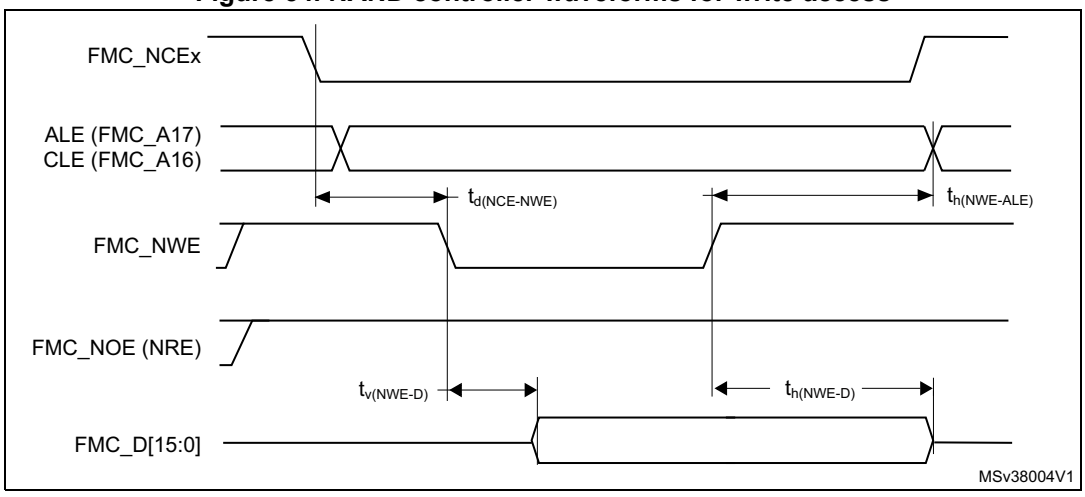
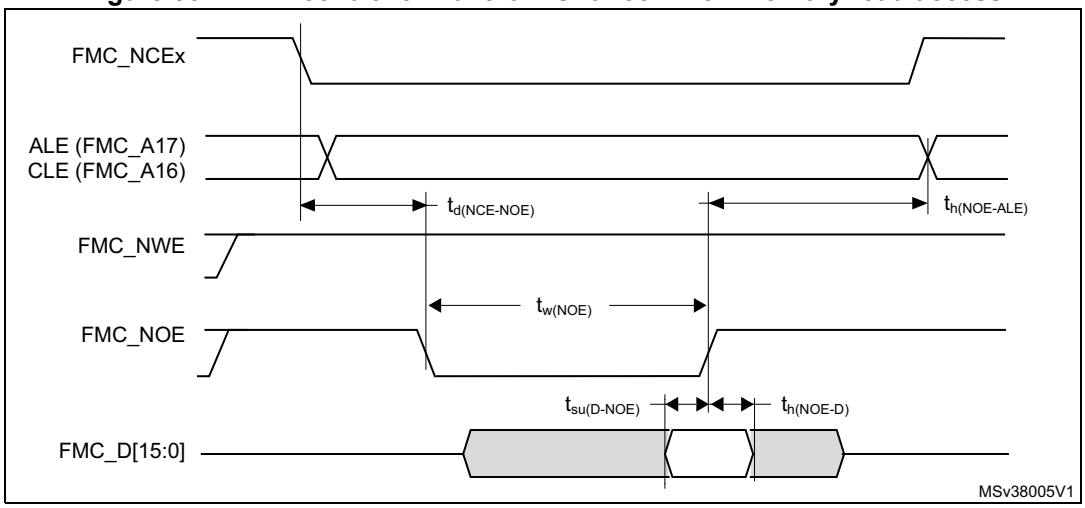
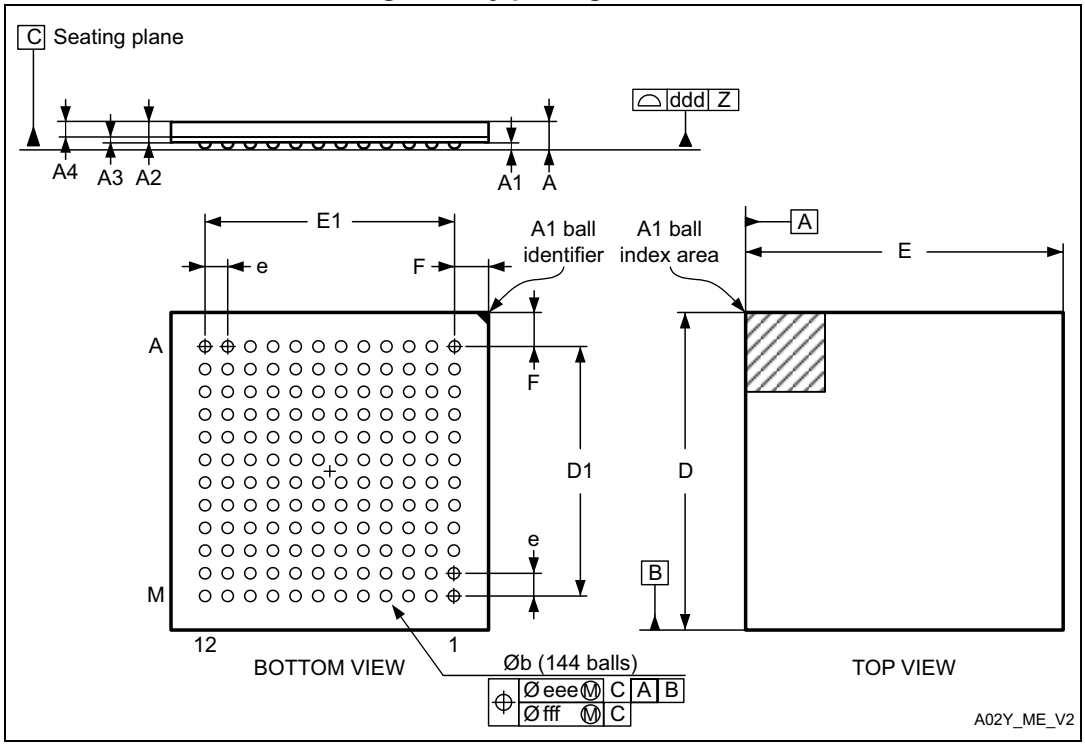



**Figure 55. NAND controller waveforms for common memory read access**



## 7.2 UFBGA144 package information

**Figure 70. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline**



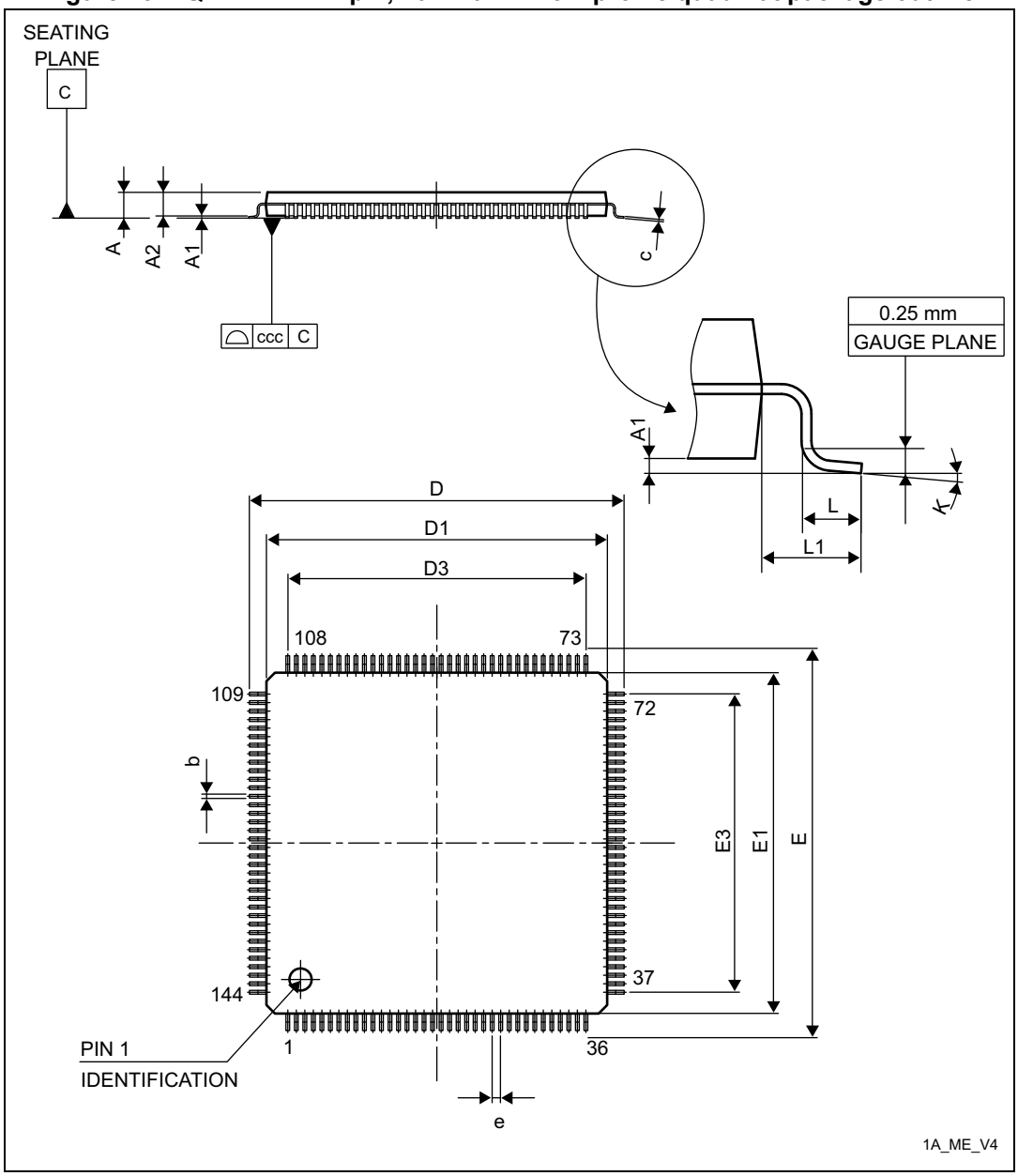

1. Drawing is not to scale.

**Table 120. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | - | 0.130 | - | - | 0.0051 | - |
| A4 | - | 0.320 | - | - | 0.0126 | - |
| b | 0.360 | 0.400 | 0.440 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| E | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| e | 0.750 | 0.800 | 0.850 | - | 0.0197 | - |
| F | 0.550 | 0.600 | 0.650 | 0.0177 | 0.0197 | 0.0217 |

## 7.3 LQFP144 package information

**Figure 73. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline**




1. Drawing is not to scale.