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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n107-518

6 BLOCK DIAGRAM

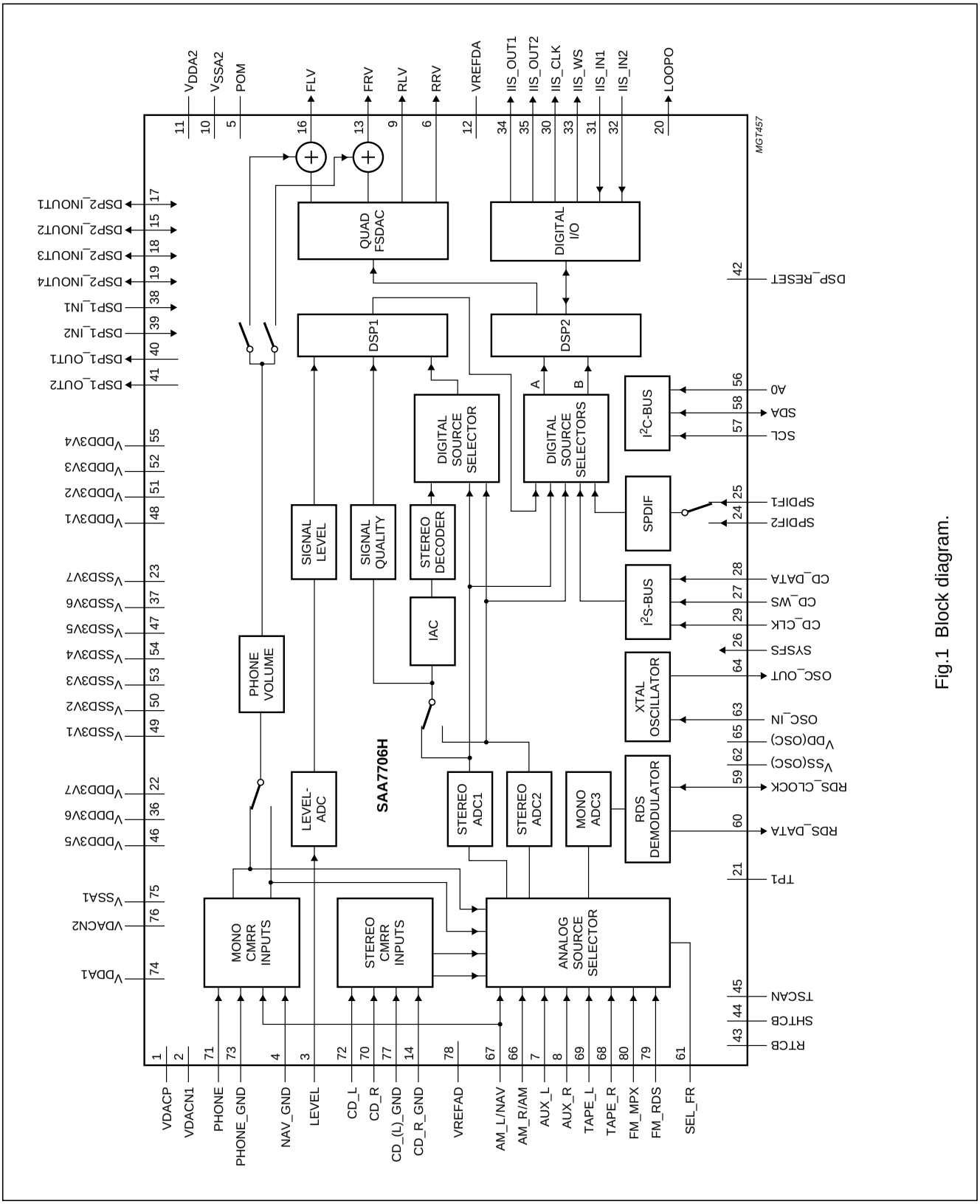


Fig.1 Block diagram.

SYMBOL	PIN	PIN TYPE	DESCRIPTION
PHONE_GND	73	apio gsmcap	common mode reference input pin of the PHONE signal
V_{DDA1}	74	vddco	positive supply analog (ADC1, ADC2, ADC3 and level-ADC only)
V_{SSA1}	75	vssco	ground supply analog (ADC3 and level-ADC only)
VDACN2	76	apio	ground reference voltage (ADC2)
CD_(L)_GND	77	apio gsmcap	common mode reference input pin for analog CD or TAPE or in the event of separated ground reference pins used for CD_L or TAPE_L
VREFAD	78	apio	common mode reference voltage ADC1, ADC2, ADC3 and level-ADC
FM_RDS	79	apio gsmcap	FM RDS signal; analog input pin
FM_MPX	80	apio gsmcap	FM multiplex signal; analog input pin

Table 1 Brief explanation of used pin types

PIN TYPE	EXPLANATION
apio	3-state I/O analog; I/O pad cell; actually pin type vddco
apio gsmcap	3-state I/O analog; I/O pad cell; actually pin type vddco with high GSM immunity
bpts5thdt5v	43 MHz bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
bpts10tht5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; 5 V tolerant
bpts10thdt5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
iic400kt5v	I^2C-bus pad; 400 kHz I^2C-bus specification; TTL; 5 V tolerant
ipthtt5v	input pad buffer; TTL; hysteresis; 5 V tolerant
ipthdt5v	input pad buffer; TTL; hysteresis; pull-down; 5 V tolerant
iptut5v	input pad buffer; TTL; pull-up; 5 V tolerant
op4mc	output pad buffer; 4 mA output drive; CMOS; slew rate control; 50 MHz
ots10ct5v	output pad buffer; 3-state, 10 ns slew rate control; CMOS; 5 V tolerant
ops10c	output pad buffer; 4 mA output drive; CMOS; slew rate control; 21 MHz
vdde	V_{DD} supply peripheral only
vsse	V_{SS} supply peripheral only
vddco	V_{DD} supply to core only
vssco	V_{SS} supply to core only (vssco does not connect the substrate)
vddi	V_{DD} supply to core and peripheral
vssis	V_{SS} supply to core and peripheral; with substrate connection

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

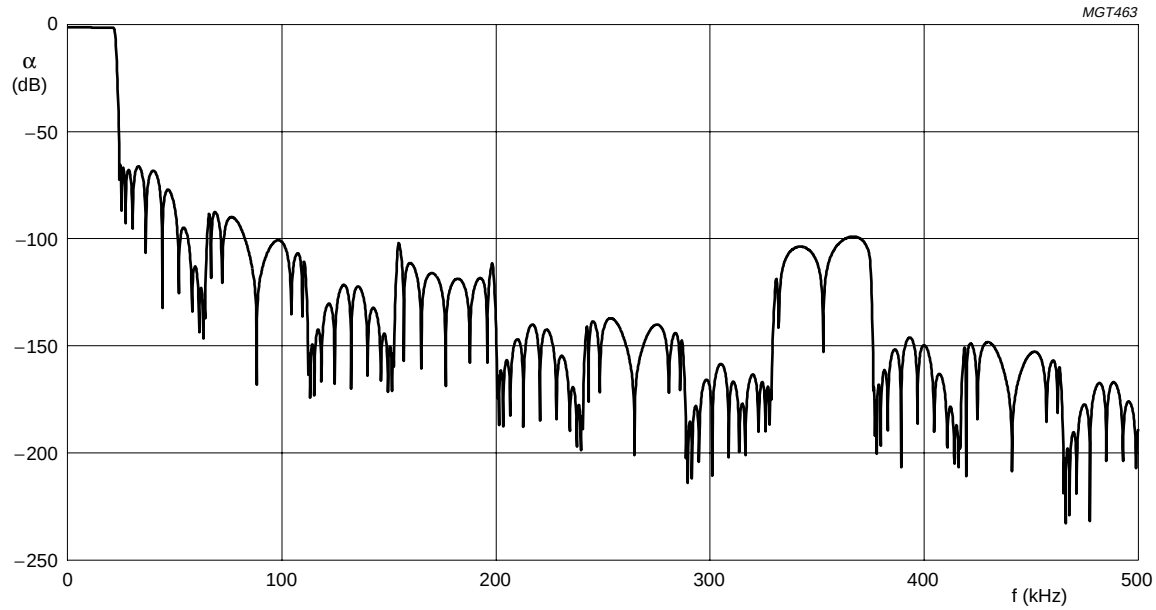


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

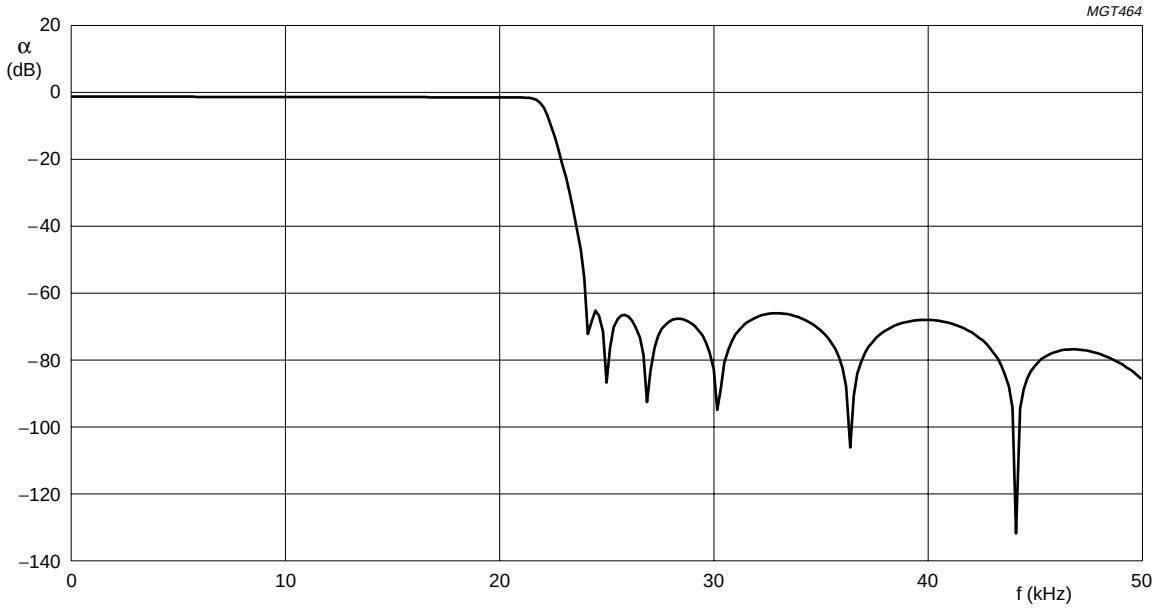


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.3 Signal path for level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a level input is implemented (pin LEVEL). In the event of radio reception the clocking of the filters and the level-ADC is based on a 38 kHz sampling frequency. A DC input signal is converted by a bitstream sigma-delta ADC followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to pin LEVEL.

The input signal for level must be in the range 0 to 3.3 V ($V_{VDACP} - V_{VDACN}$). The 9-bit level-ADC converts this input voltage in steps with a resolution better than at least 14 mV over the 3.3 V range.

The tolerance on the gain is less than 2%. The MSB is always logic 0 to represent a positive level. Input level span can be increased by an external resistor tap. The high input impedance of the level-ADC makes this possible.

The decimation filter reduces in the event of an 38 kHz based clocking regime the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz with a resulting f_s = 76 kHz. The response curve is given in Fig.9.

The level information is sub-sampled by the DSP1 to obtain a field strength and a multipath indication. These values are stored in the coefficient or data RAM. Via the I^2C-bus they can be read and used in other microcontroller programs.

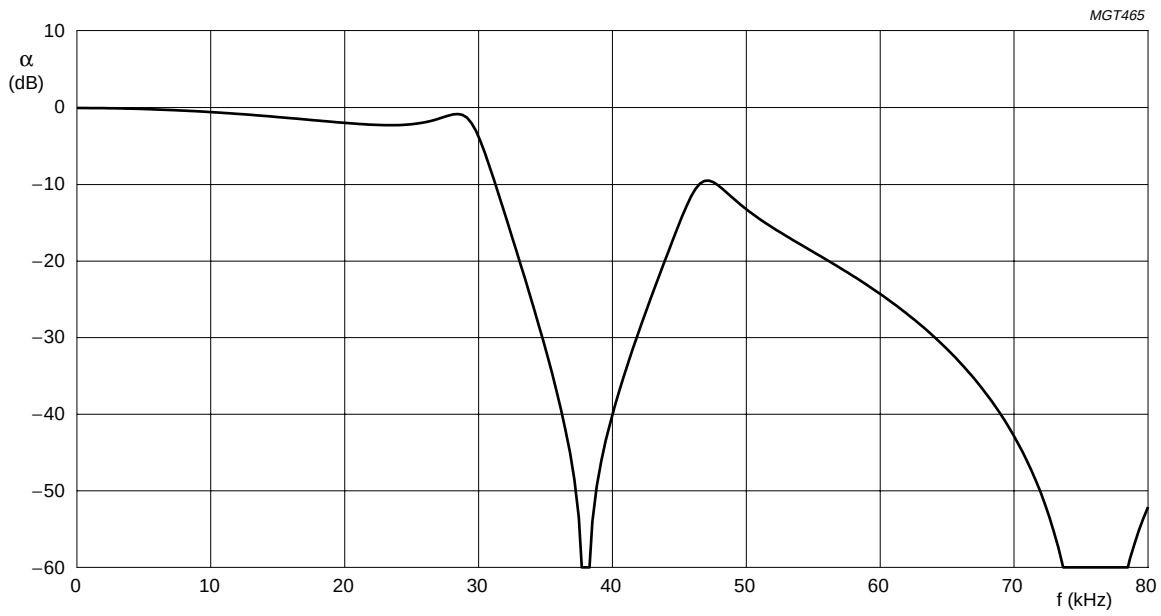
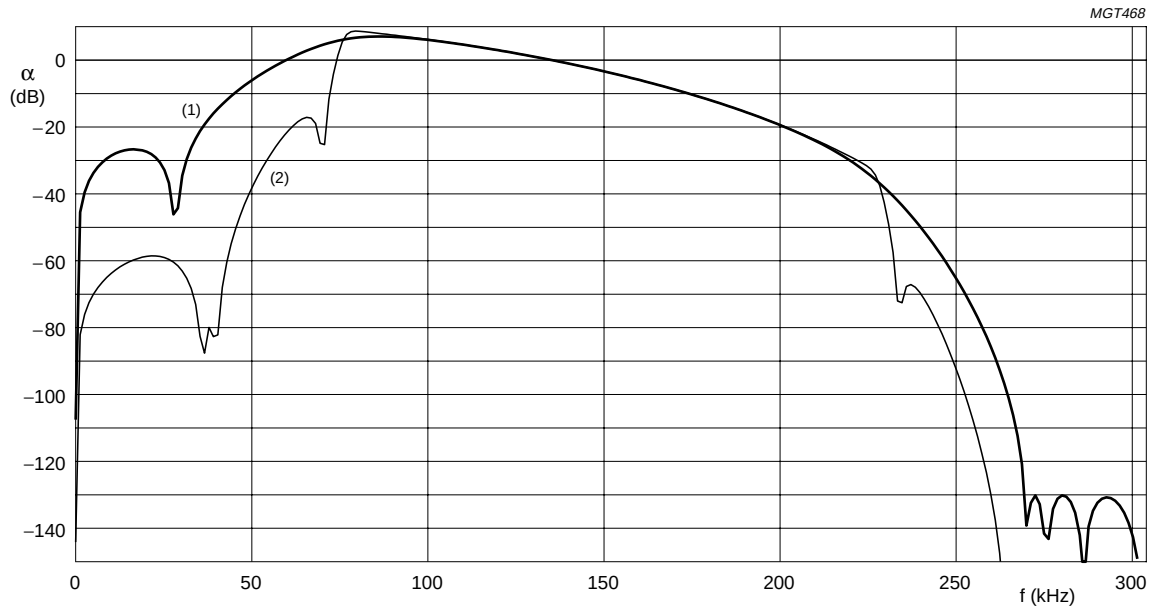


Fig.9 Frequency response level-ADC and decimal filter.

8.4.1 NOISE LEVEL

The high-pass 1 (HP1 or narrow band noise level filter) output of the second MPX decimation filter in a band from 60 kHz to 120 kHz is detected with an envelope detector and decimated to a frequency of 38 kHz. The response time of the detector is 100 µs. Another option is the high-pass 2 (HP2 or wide band noise level filter). This output of the first MPX decimation filter is in a band from 60 to 240 kHz. It has the same properties and is also decimated to the same 38 kHz. Which of the signals is used (HP1 or HP2) is determined by the I^2C-bus bit sel_nsdec.

The resulting noise information is rectified and has a word length of 10 bits. This means that the lowest and/or the highest possible level is not used. The noise level can be detected and filtered in the DSP1-core and be used to optimize the FM weak signal processing. The transfer curves of both filters before decimation are shown in Fig.12.



(1) Noise with wide band digital filter.
(2) Noise with small band digital filter.

Fig.12 Frequency response of noise level before decimation.

8.4.2 MONO OR STEREO SWITCHING

The DCS block uses a sample rate converter to derive from the XTAL clock, via a PLL, a 512 multiple of 19 kHz (9.728 MHz). In the event of mono reception the DCS circuit generates a preset frequency of n × 19 kHz ±2 Hz. In the event of stereo reception the frequency is exactly n × 19 kHz (DCS locked to N × pilot tone). The detection of the pilot and the stereo indication is done in the DSP program.

8.4.3 THE AUTOMATIC LOCK SYSTEM

The VCO of the DCS block will be at 19 kHz ±2 Hz exact based in the event of no-pilot FM_MPX reception or in the event of only RDS reception. In the event of stereo reception the phase error is zero for a pilot tone with a frequency of exactly 19 kHz.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I^2C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I^2C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I^2C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

8.7.3 Function of pin POM

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has past a particular level. This results in an almost dB-linear behaviour. This must prevent 'plop' effects during power on or off.

8.7.4 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate power supply of 3.3 V. A capacitor connected to this power supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

8.7.5 Pin VREFDA for internal reference

With two internal resistors half the supply voltage V_{DDA2} is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC.

In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin V_{SSA2}.

8.7.6 Supply of the filter stream DAC

The entire analog circuitry of the DACs and the operational amplifiers are supplied by 2 supply pins: V_{DDA2} and V_{SSA2}. V_{DDA2} must have sufficient decoupling to prevent total harmonic distortion degradation and to ensure a good power supply rejection ratio. The digital part of the DAC is fully supplied from the chip core supply.

8.8 Clock circuit and oscillator

The chip has an on-chip crystal clock oscillator. The block diagram of this Pierce oscillator is shown in Fig.13. The active element needed to compensate for the loss resistance of the crystal is the block G_m. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to the clock signal.

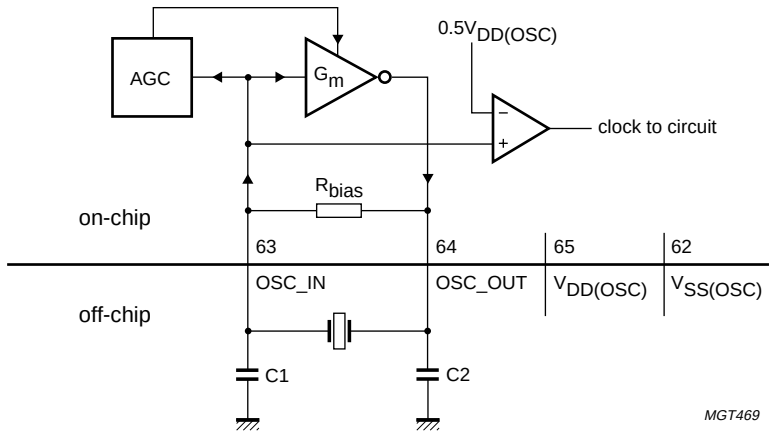


Fig.13 Block diagram oscillator circuit.

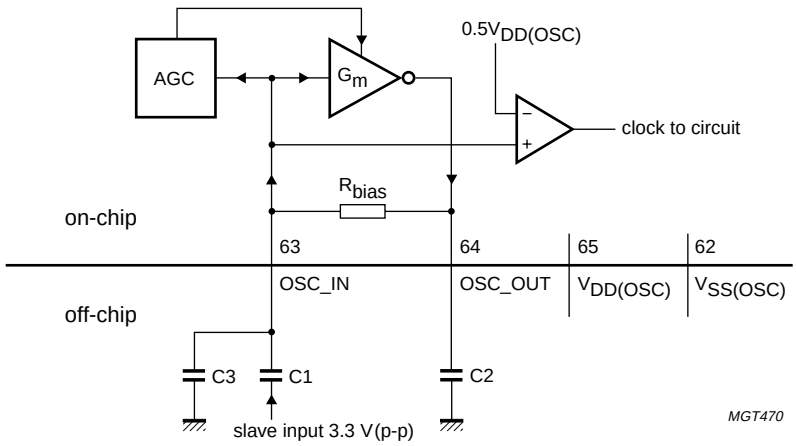


Fig.14 Block diagram of the oscillator in slave mode.

8.8.1 Supply of the crystal oscillator

The power supply connections of the oscillator are separated from the other supply lines. This is done to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin $V_{SS(OSC)}$ is used as ground supply and pin $V_{DD(OSC)}$ as positive supply. A series resistor plus capacitance is required for proper operating on pin $V_{DD(OSC)}$, see Figs 25 and 26. See also important remark in Section 8.10.

8.9 The phase-locked loop circuit to generate the DSPs and other clocks

There are several reasons why a PLL circuit is used to generate the clock for the DSPs:

- The PLL makes it possible to switch in the rare cases that tuning on a multiple of the DSP clock frequency occurs to a slightly higher frequency for the clock of the DSP. In this way an undisturbed reception with respect to the DSP clock frequency is possible.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 100 MHz, are always third overtone crystals and must also be manufactured on customer demand. This makes these crystals expensive. The PLL1 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256×44.1 kHz = 11.2896 MHz crystal is chosen. This type of crystal is widely used.
- Although a multiple of the frequency of the used crystal of 11.2896 MHz falls within the FM reception band, this will not disturb the reception because the relatively low frequency crystal is driven in a controlled way and the sine wave of the crystal has in the FM reception band only very minor harmonics.

8.10 Supply of the digital part (V_{DDD3V1} to V_{DDD3V4})

The supply voltage on pins V_{DDD3V1} to V_{DDD3V4} must be for at least 10 ms earlier active than the supply voltage applied to pin $V_{DD(OSC)}$.

8.11 CL_GEN, audio clock recovery block

When an external I^2S-bus or SPDIF source is connected, the FSDAC circuitry needs an $256f_s$ related clock. This clock is recovered from either the incoming WS of the digital serial input or the WS derived from the SPDIF1/SPDIF2 input. There is also a possibility to provide the chip with an external clock, in that case it must be a $256f_s$ clock with a fixed phase relation to the source.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I^2S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I^2S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I^2C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I^2C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

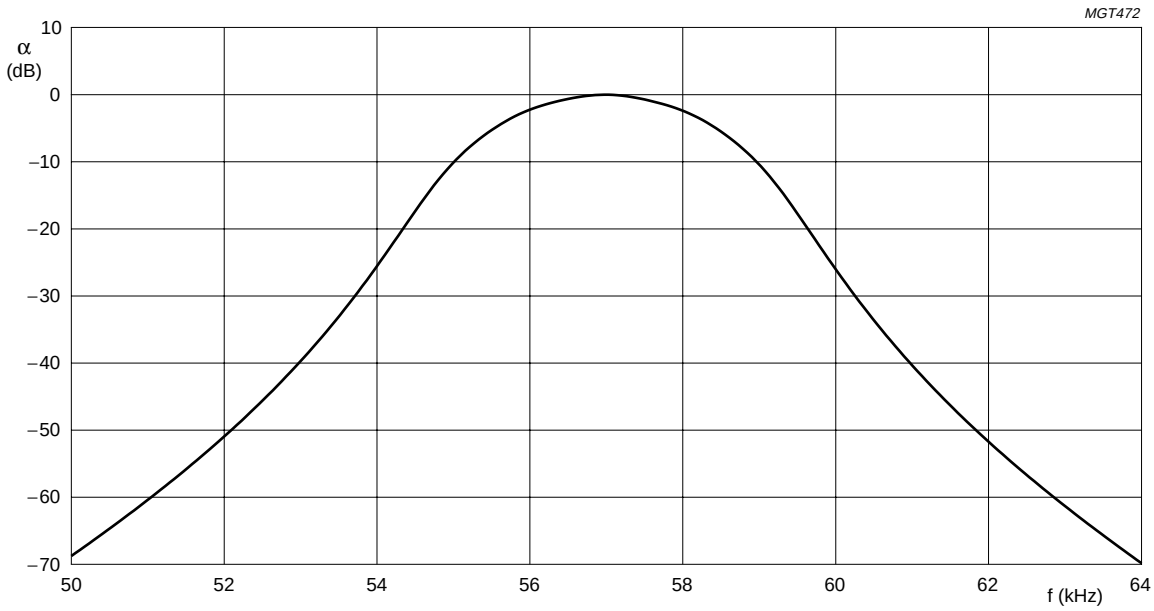


Fig.17 Detailed frequency response curve RDS channel.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDS_CLOCK and RDS_DATA. In the event of FM-stereo reception the clock of the total chip is locked to the stereo pilot (19 kHz multiple). In the event of FM-mono the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases like AM reception or tape, the DCS circuit has to be set in a preset position by means of an I^2C-bus bit. Under these conditions the RDS system is always clocked by the DCS clock in a 38 kHz (4×9.5 kHz) based sequence.

8.15.2 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 μs after the clock transition. The timing of the data change is 100 μs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller. The RDS timing is shown in Fig.18. During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

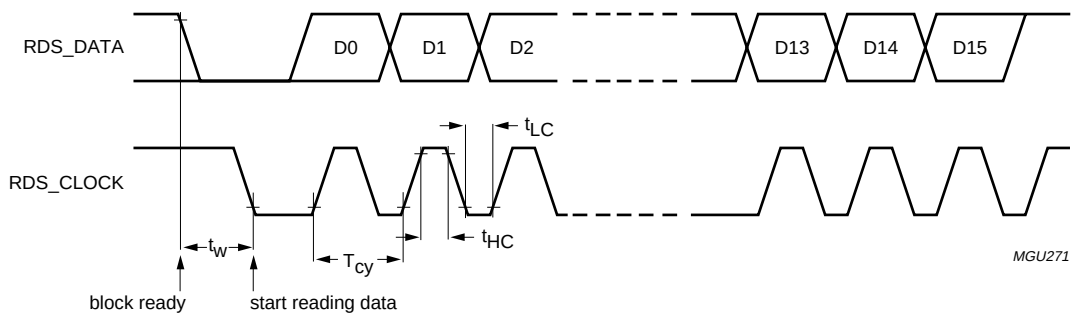


Fig.19 Interface signals RDS decoder and microcontroller (buffer mode).

8.16 DSP reset

Pin DSP_RESET is active LOW and requires an external pull-up resistor. Between this pin and the V_{SSD} ground a capacitor should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in reset as long as the power supply is not stabilized. A more or less fixed relationship between the DSP_RESET (pin) and the POM (pin) time constant is mandatory.

The voltage on pin POM determines the current flowing in the DACs. At 0 V on pin POM the DAC currents are zero and so are the DAC output voltages.

At the V_{DDA2} voltage the DAC currents are at their nominal (maximal) value. Long before the DAC outputs get to their nominal output voltages, the DSP must be in working mode to reset the output register: therefore the DSP time constant must be shorter than the POM time constant. For recommended capacitors see Figs 25 and 26.

The reset has the following function:

- All I^2C-bus bits are set to their default value
- The DSP status registers (DSP1 and DSP2) are reset
- The program counter of both DSPs are set to address 0000H
- The two output flags of DSP1 (DSP1_OUT1 and DSP1_OUT2) are reset to logic 0. All the configurable flags of DSP2 are reset to logic 0, however the four flags available at the output of the chip are default configured as input flags (DSP2_INOUT1, DSP2_INOUT2, DSP2_INOUT3 and DSP2_INOUT4).

When the level on pin DSP_RESET is at HIGH, the DSP program (DSP1 and DSP2) starts to run.

8.17 Test mode connections (pins TSCAN, RTCB and SHTCB)

Pins TSCAN, RTCB and SHTCB are used to put the chip in test mode and to test the internal connections. Each pin has an internal pull-down resistor to ground. In the application these pins can be left open or connected to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{tot}	total power dissipation	DSP1 at 50 MHz, DSP2 at 62.9 MHz	–	540	750	mW
Digital I/O; T_{amb} = −40 to +85 °C; V_{DD} = 3 to 3.6 V						
V_{IH}	HIGH-level input voltage for all digital inputs and I/Os		2.0	–	–	V
V_{IL}	LOW-level input voltage for all digital inputs and I/Os		–	–	0.8	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	–	V
V_{OH}	HIGH-level output voltage	standard output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		5 ns slew rate output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		10 ns slew rate output; I_O = –2 mA	V_{DD} – 0.4	–	–	V
		20 ns slew rate output; I_O = –1 mA	V_{DD} – 0.4	–	–	V
V_{OL}	LOW-level output voltage	standard output; I_O = 4 mA	–	–	0.4	V
		5 ns slew rate output; I_O = 4mA	–	–	0.4	V
		10 ns slew rate output; I_O = 2 mA	–	–	0.4	V
		20 ns slew rate output; I_O = 1 mA	–	–	0.4	V
		I^2C-bus output; I_O = 4 mA	–	–	0.4	V
I_{LO}	output leakage current 3-state outputs	V_O = 0 V or V_{DD}	–	–	±5	µA
R_{pd}	internal pull-down resistor to V_{SS}		24	50	140	kΩ
R_{pu}	internal pull-up resistor to V_{DD}		30	50	100	kΩ
C_i	input capacitance		–	–	3.5	pF
$t_{i(r)}$,$t_{i(f)}$	input rise and fall times	V_{DD} = 3.6 V	–	6	200	ns
$t_{o(t)}$	output transition time	standard output; C_L = 30 pF	–	3.5	–	ns
		5 ns slew rate output; C_L = 30 pF	–	5	–	ns
		10 ns slew rate output; C_L = 30 pF	–	10	–	ns
		20 ns slew rate output; C_L = 30 pF	–	20	–	ns
		I^2C-bus output; C_b = 400 pF	60	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

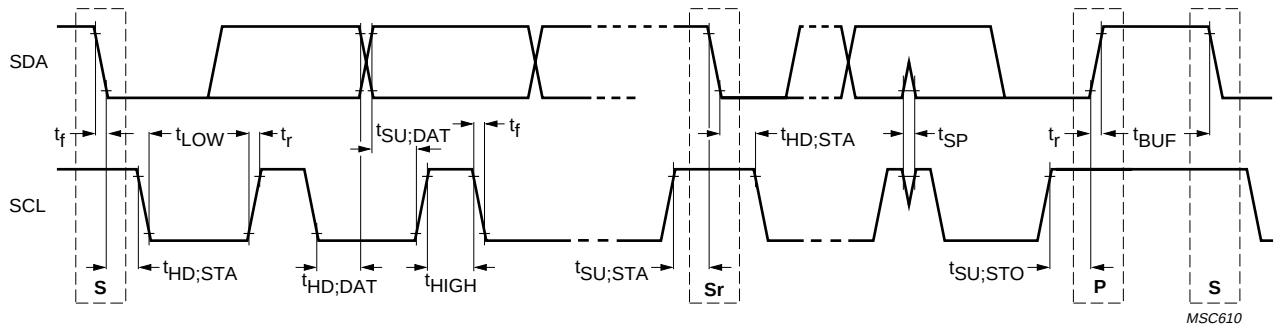


Fig.24 Definition of timing on the I²C-bus.

15 SOFTWARE DESCRIPTION

The use and description of the software features of the SAA7706H will be described in the separate application manual.

16 APPLICATION DIAGRAM

The application diagram shown in Figs 25 and 26 must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I²S-bus inputs of the CD-input are not used. For the real application set-up the information of the application report is necessary.

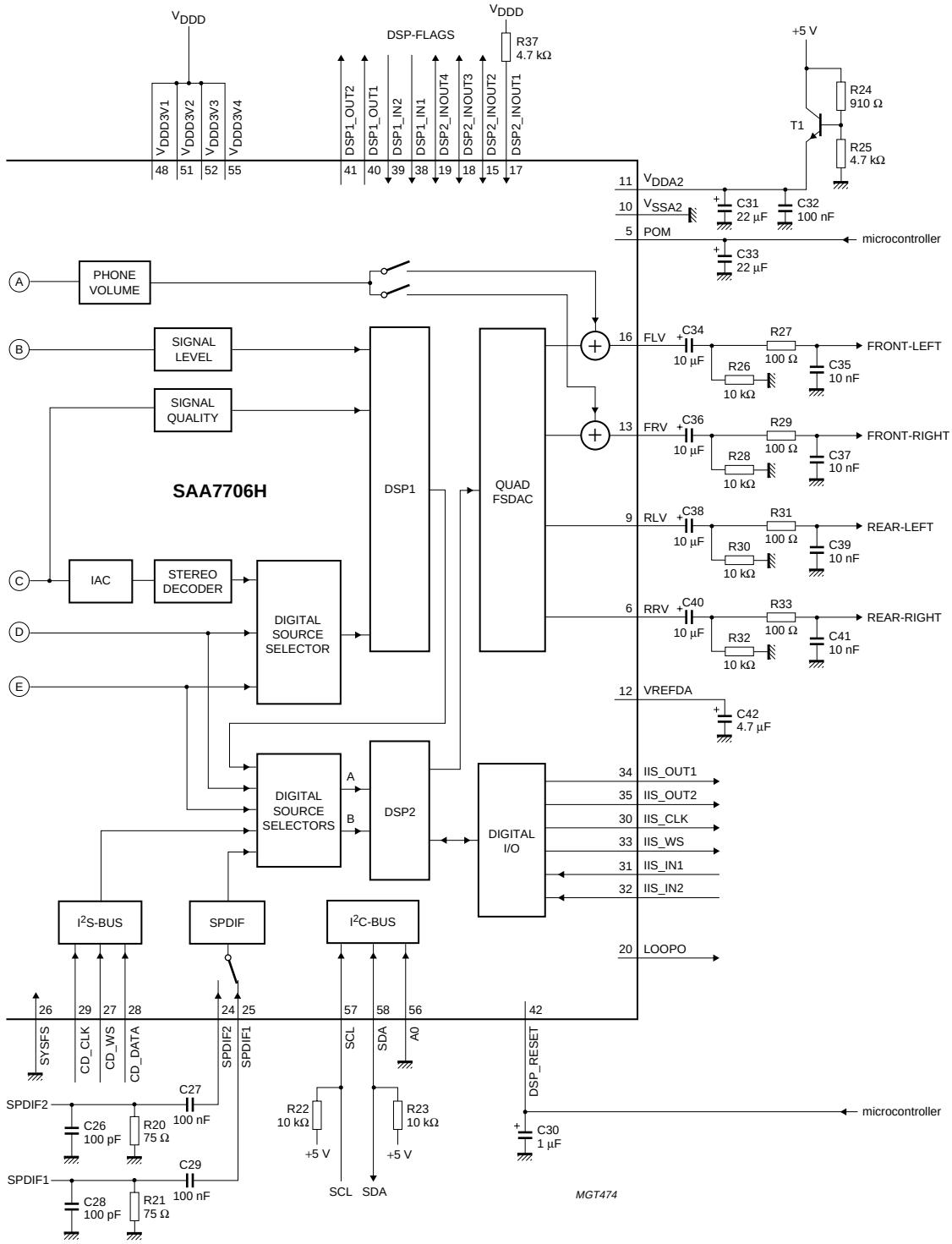
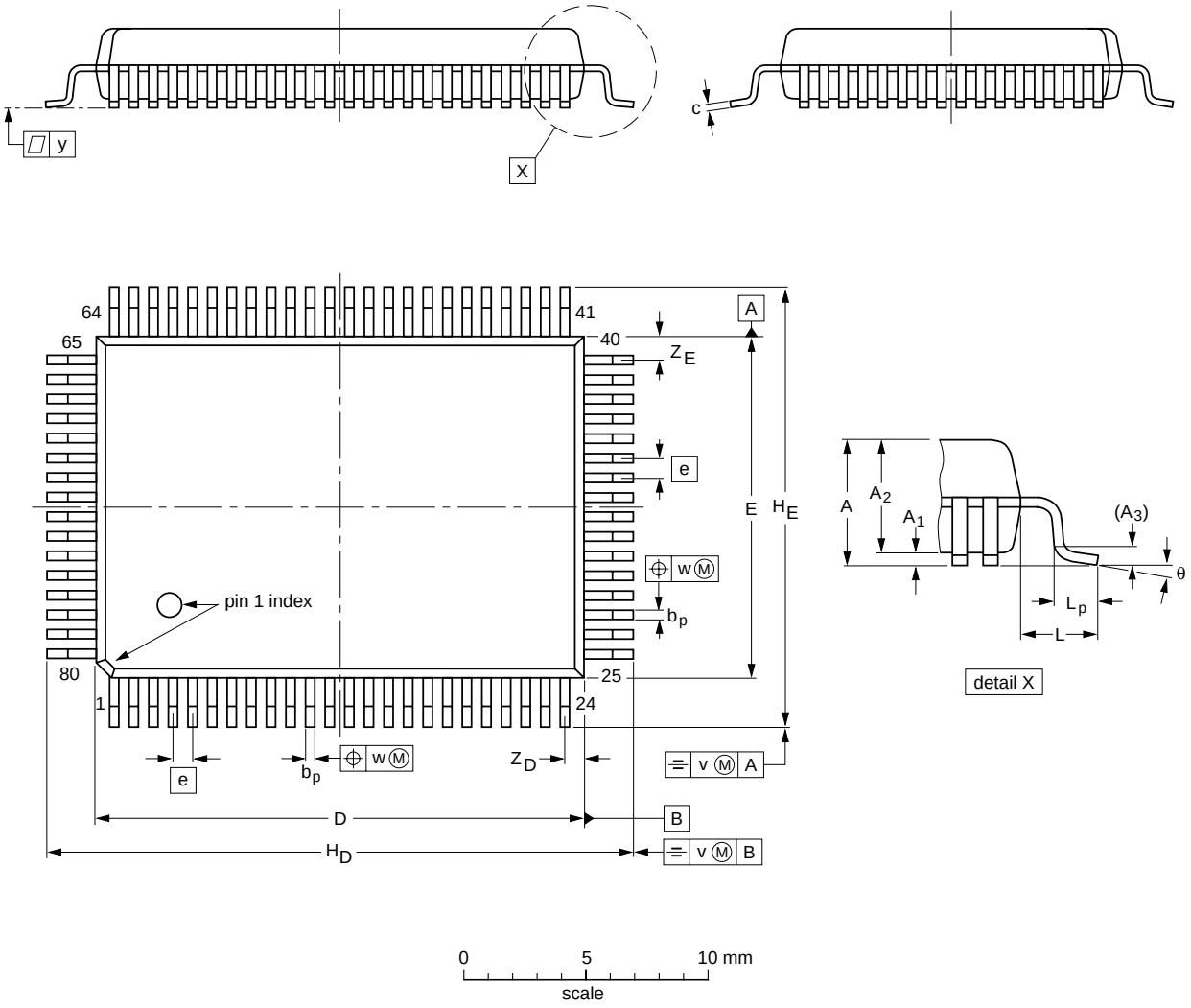


Fig.26 Application diagram (continued from Fig.25).

17 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				~~97-08-01~~ 99-12-27

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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