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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n107s-518

- Noise generator allows for frequency response measurements
- Boot-up ROM for fast start-up
- Signal level, noise and multipath detection for AM or FM signal quality information
- AM co-channel and adjacent channel detection (not in all rom_codes available).

2 APPLICATIONS

- High-end car radio systems.

3 GENERAL DESCRIPTION

The SAA7706H performs all the signal functions in front of the power amplifiers and behind the car radio tuner AM and FM outputs and the CD, tape and phone inputs. These functions are:

- Interference absorption
- Stereo decoding for FM and AM (stereo)
- RDS-demodulation
- FM and AM weak signal processing (soft mute, sliding stereo and high cut)
- Dolby-B tape noise reduction
- CD de-emphasis function
- Audio controls for volume, balance, fader, tone and dynamics compression.

Some functions have been implemented in hardware (FM stereo decoder, RDS-demodulator and FM Interference Absorption Circuit (IAC) and are not freely programmable.

Digital audio signals from external sources with the Philips I^2S-bus and the LSB-justified 16, 18, 20 and 24 bits format or SPDIF format are accepted.

The big advantage of this SAA7706H device is the ‘dual media support’; this enables independent front seat and rear seat audio sources and control.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
P_{tot}	total power dissipation	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	540	750	mW
FM_MPX input						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%; VOLFM = 00H	0.33	0.368	–	V
THD	total harmonic distortion	input signal 0.368 V (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	–70	–65	dB
			–	0.03	0.056	%
S/N	signal-to-noise ratio input stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
CD, TAPE, AUX and AM inputs						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%	0.6	0.66	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz	–	–85	–75	dB
S/N	signal-to-noise ratio	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS)	85	90	–	dB
FSDAC						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio (measured with system one)	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio (measured with system one)	code = 0; A-weighted	–	105	–	dB
Crystal oscillator						
f_{xtal}	crystal frequency		–	11.2896	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7706H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

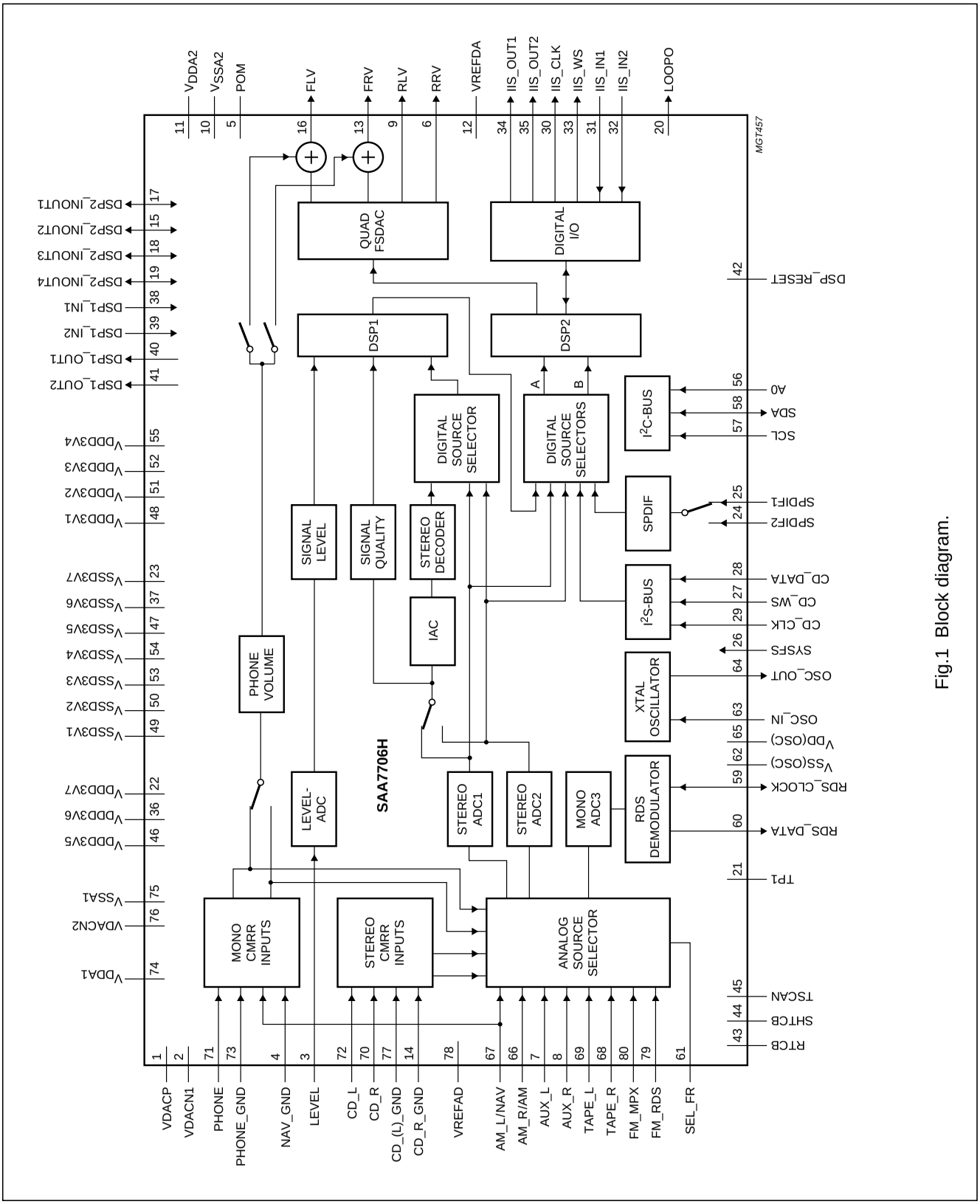


Fig.1 Block diagram.

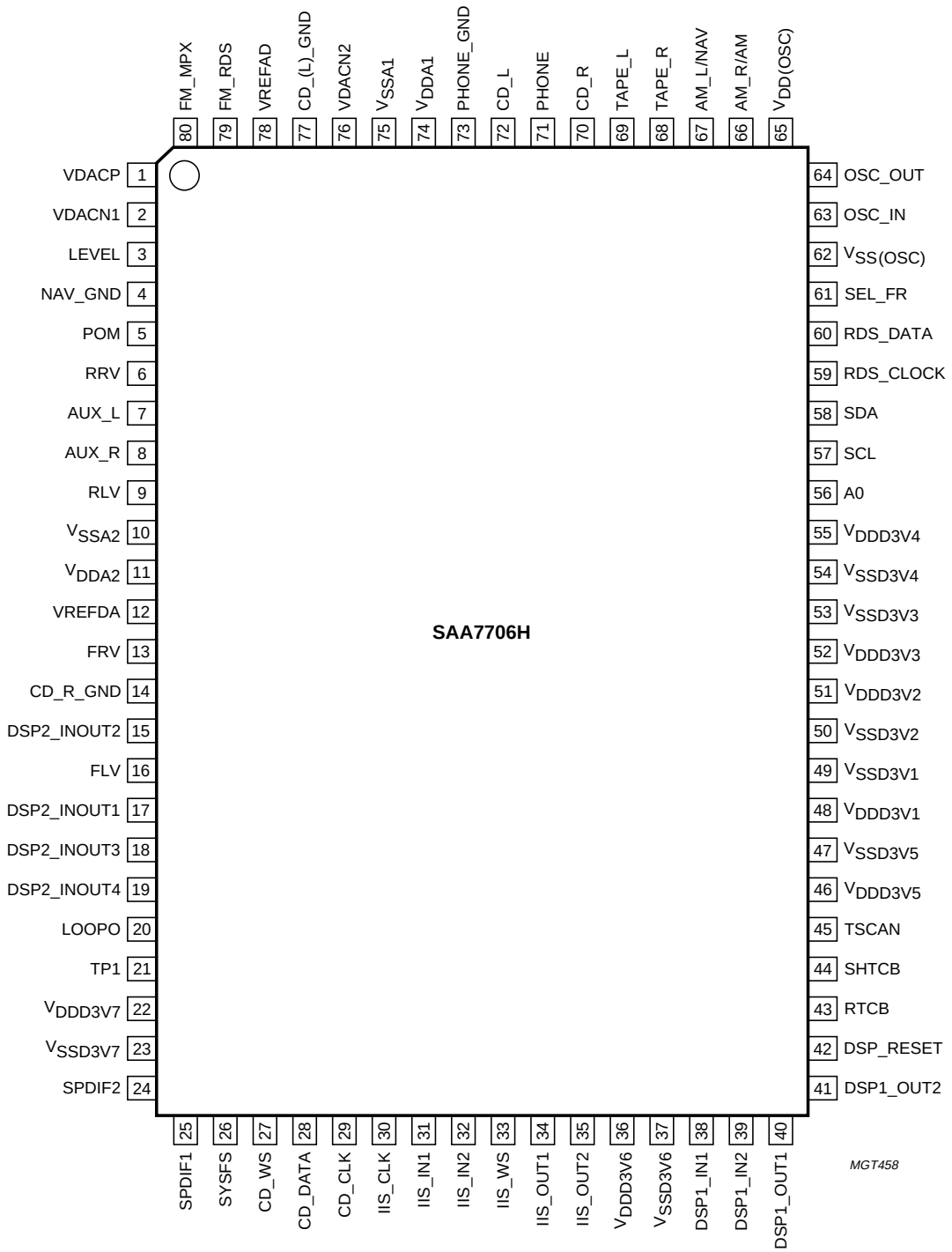


Fig.2 Pinning diagram.

8 FUNCTIONAL DESCRIPTION

8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via I^2C-bus.

8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

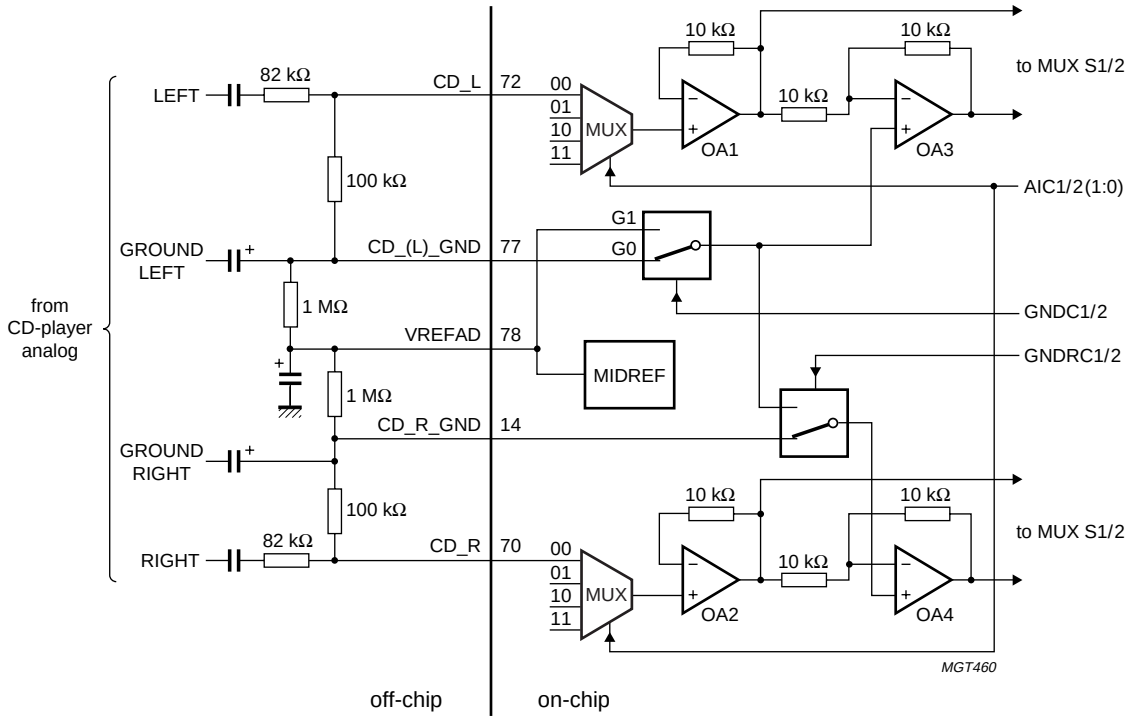


Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

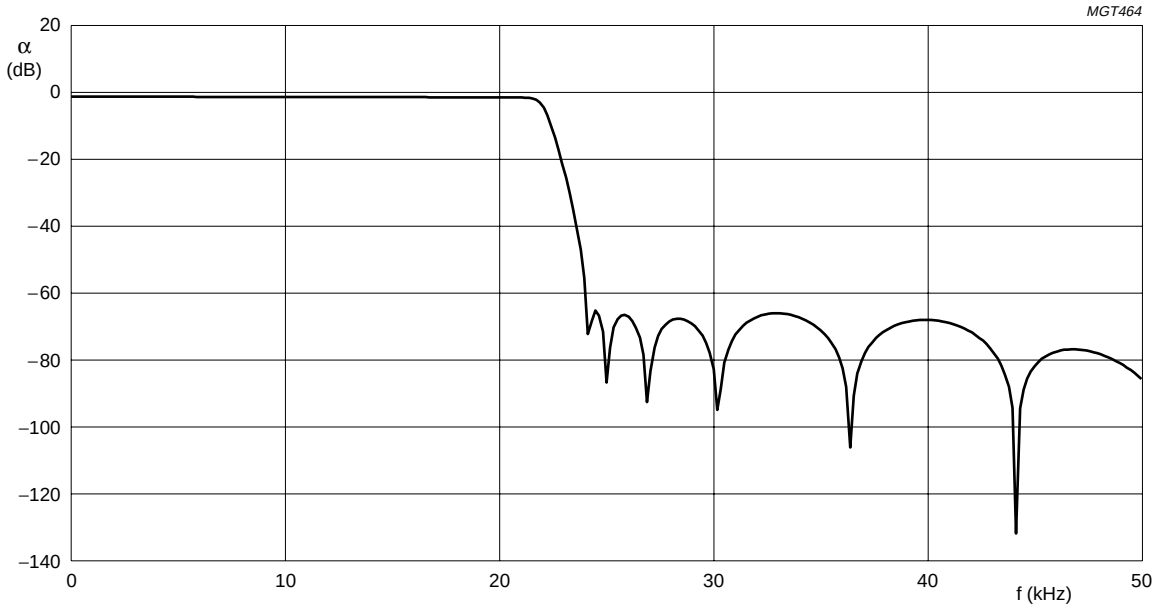


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.3 Signal path for level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a level input is implemented (pin LEVEL). In the event of radio reception the clocking of the filters and the level-ADC is based on a 38 kHz sampling frequency. A DC input signal is converted by a bitstream sigma-delta ADC followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to pin LEVEL.

The input signal for level must be in the range 0 to 3.3 V ($V_{VDACP} - V_{VDACN}$). The 9-bit level-ADC converts this input voltage in steps with a resolution better than at least 14 mV over the 3.3 V range.

The tolerance on the gain is less than 2%. The MSB is always logic 0 to represent a positive level. Input level span can be increased by an external resistor tap. The high input impedance of the level-ADC makes this possible.

The decimation filter reduces in the event of an 38 kHz based clocking regime the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz with a resulting f_s = 76 kHz. The response curve is given in Fig.9.

The level information is sub-sampled by the DSP1 to obtain a field strength and a multipath indication. These values are stored in the coefficient or data RAM. Via the I^2C-bus they can be read and used in other microcontroller programs.

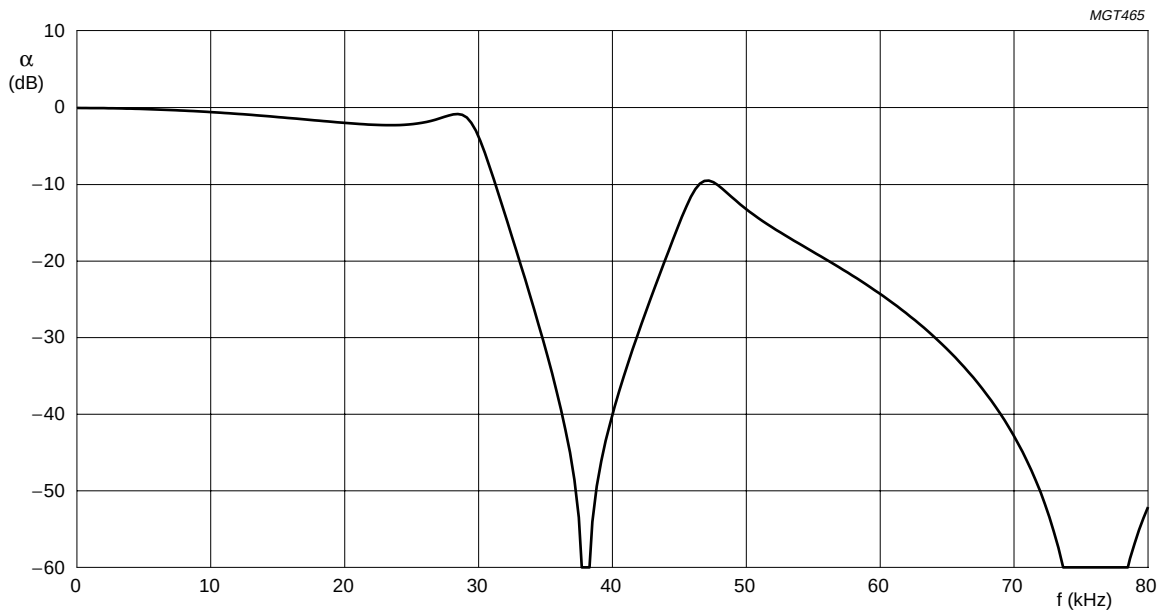
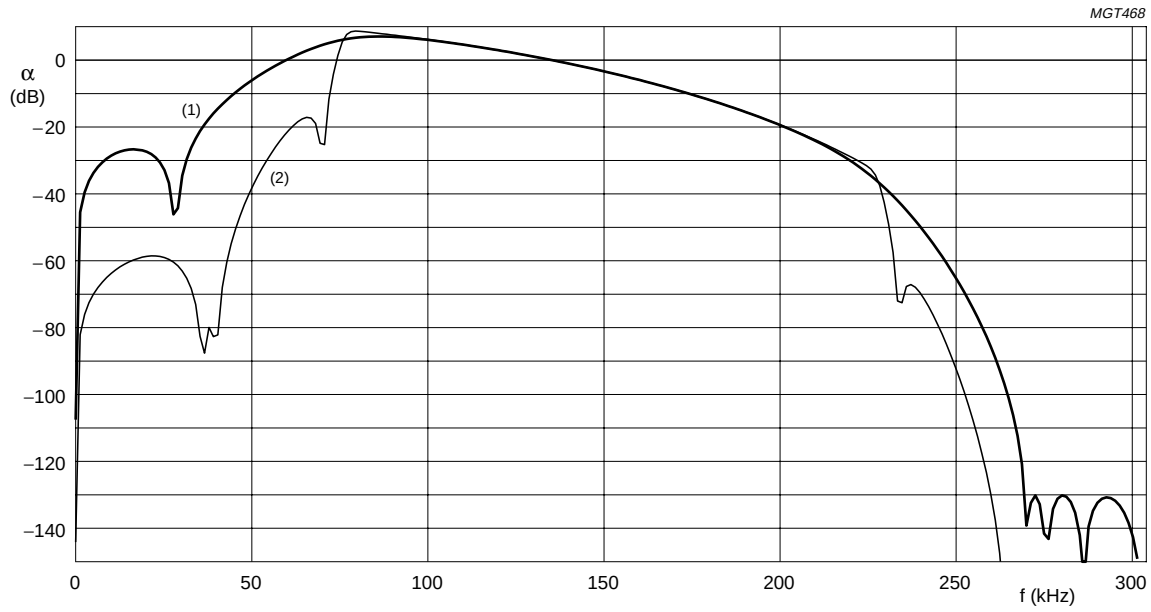


Fig.9 Frequency response level-ADC and decimal filter.

8.4.1 NOISE LEVEL

The high-pass 1 (HP1 or narrow band noise level filter) output of the second MPX decimation filter in a band from 60 kHz to 120 kHz is detected with an envelope detector and decimated to a frequency of 38 kHz. The response time of the detector is 100 µs. Another option is the high-pass 2 (HP2 or wide band noise level filter). This output of the first MPX decimation filter is in a band from 60 to 240 kHz. It has the same properties and is also decimated to the same 38 kHz. Which of the signals is used (HP1 or HP2) is determined by the I^2C-bus bit sel_nsdec.

The resulting noise information is rectified and has a word length of 10 bits. This means that the lowest and/or the highest possible level is not used. The noise level can be detected and filtered in the DSP1-core and be used to optimize the FM weak signal processing. The transfer curves of both filters before decimation are shown in Fig.12.



(1) Noise with wide band digital filter.
(2) Noise with small band digital filter.

Fig.12 Frequency response of noise level before decimation.

8.4.2 MONO OR STEREO SWITCHING

The DCS block uses a sample rate converter to derive from the XTAL clock, via a PLL, a 512 multiple of 19 kHz (9.728 MHz). In the event of mono reception the DCS circuit generates a preset frequency of n × 19 kHz ±2 Hz. In the event of stereo reception the frequency is exactly n × 19 kHz (DCS locked to N × pilot tone). The detection of the pilot and the stereo indication is done in the DSP program.

8.4.3 THE AUTOMATIC LOCK SYSTEM

The VCO of the DCS block will be at 19 kHz ±2 Hz exact based in the event of no-pilot FM_MPX reception or in the event of only RDS reception. In the event of stereo reception the phase error is zero for a pilot tone with a frequency of exactly 19 kHz.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I^2C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I^2C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I^2C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

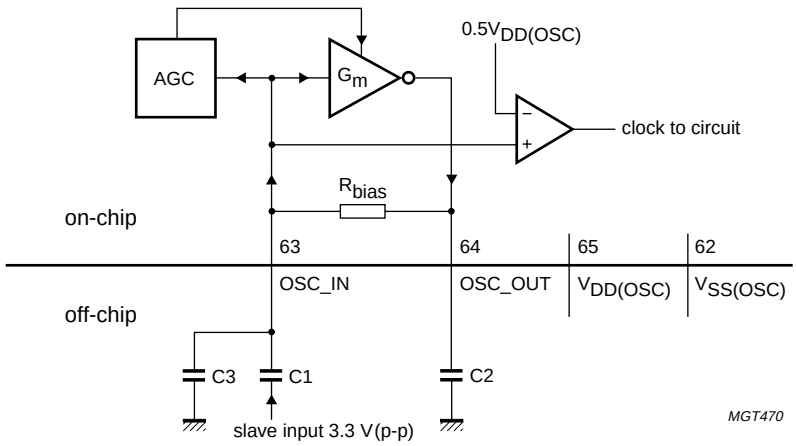


Fig.14 Block diagram of the oscillator in slave mode.

8.8.1 Supply of the crystal oscillator

The power supply connections of the oscillator are separated from the other supply lines. This is done to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin $V_{SS(OSC)}$ is used as ground supply and pin $V_{DD(OSC)}$ as positive supply. A series resistor plus capacitance is required for proper operating on pin $V_{DD(OSC)}$, see Figs 25 and 26. See also important remark in Section 8.10.

8.9 The phase-locked loop circuit to generate the DSPs and other clocks

There are several reasons why a PLL circuit is used to generate the clock for the DSPs:

- The PLL makes it possible to switch in the rare cases that tuning on a multiple of the DSP clock frequency occurs to a slightly higher frequency for the clock of the DSP. In this way an undisturbed reception with respect to the DSP clock frequency is possible.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 100 MHz, are always third overtone crystals and must also be manufactured on customer demand. This makes these crystals expensive. The PLL1 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256×44.1 kHz = 11.2896 MHz crystal is chosen. This type of crystal is widely used.
- Although a multiple of the frequency of the used crystal of 11.2896 MHz falls within the FM reception band, this will not disturb the reception because the relatively low frequency crystal is driven in a controlled way and the sine wave of the crystal has in the FM reception band only very minor harmonics.

8.10 Supply of the digital part (V_{DDD3V1} to V_{DDD3V4})

The supply voltage on pins V_{DDD3V1} to V_{DDD3V4} must be for at least 10 ms earlier active than the supply voltage applied to pin $V_{DD(OSC)}$.

8.11 CL_GEN, audio clock recovery block

When an external I^2S-bus or SPDIF source is connected, the FSDAC circuitry needs an $256f_s$ related clock. This clock is recovered from either the incoming WS of the digital serial input or the WS derived from the SPDIF1/SPDIF2 input. There is also a possibility to provide the chip with an external clock, in that case it must be a $256f_s$ clock with a fixed phase relation to the source.

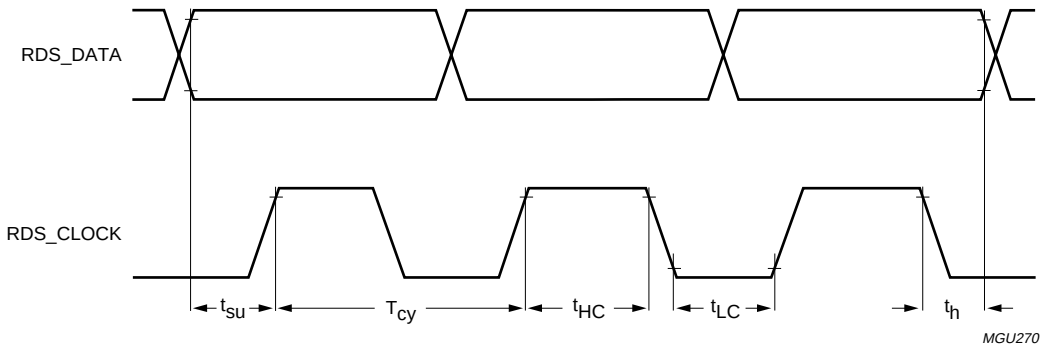


Fig.18 RDS timing in the direct output mode.

8.15.3 Buffering of RDS data

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microcontroller for every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

8.15.4 Buffer interface

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled down and the buffer is overwritten. The microcontroller has to monitor the data line in at most every 13.5 ms. This mode can be selected via an I^2C-bus.

In Fig.19 the interface signals from the RDS decoder and the microcontroller in buffer mode are shown. When the buffer is filled with 16 bits the data line is pulled down. The data line will remain LOW until reading of the buffer is started by pulling down the clock line. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the line HIGH. The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH. When a new 16-bit buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.

10 LIMITING VALUES

In accordance with the Absolute Maximum Ratings System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+3.6	V
V_n	input voltage on any pin		–0.5	+5.5	V
I_{IK}	DC input clamping diode current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamping diode current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
$I_{O(sink/source)}$	DC output source or sink current	$–0.5 \text{ V} < V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD},I_{SS}	supply current per supply pin		–	±50	mA
T_{amb}	ambient operating temperature		–40	+85	°C
T_{stg}	storage temperature range		–65	+125	°C
V_{ESD}	ESD voltage				
	human body model	100 pF; 1500 Ω	2000	–	V
	machine model	200 pF; 0.5 μH; 10 Ω	200	–	V
$I_{lu(prot)}$	latch-up protection current	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	890	mW

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	45	K/W

12 CHARACTERISTICS

V_{DD} = 3 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; T_{amb} = –40 to +85 °C						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3.0	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
$I_{DDD(core)}$	supply current of the digital core part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	105	140	mA
$I_{DDD(peri)}$	supply current of the digital periphery part	without external load to ground	–	5	10	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
$I_{DDA(ADC)}$	supply current of the ADCs	zero input and output signal	–	15	26	mA
$I_{DDA(DAC)}$	supply current of the DACs	zero input and output signal	–	19	30	mA
$I_{DDA(osc)}$	supply current XTAL oscillator	functional mode	–	2	4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{res}	audio frequency response					
	CD, TAPE, AM and AUX input signals	f_s = 44.1 kHz; at –3 dB	20	–	–	kHz
	FM_MPX input signal	at –3 dB via DSP at DAC output	17	–	–	kHz
ΔG_{L-R}	overall left/right gain unbalance (TAPE, CD, AUX and AM input signals)		–	–	0.5	dB
α_{ct}	crosstalk between inputs	f_i = 1 kHz	65	–	–	dB
		f_i = 15 kHz	50	–	–	dB
$PSRR_{MPX/RDS}$	power supply ripple rejection MPX and RDS ADCs	output via I^2S-bus; ADC input short-circuited; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{VREFAD} = 22 µF; C_{VDACP} = 10 µF	35	45	–	dB
$PSRR_{LAD}$	power supply ripple rejection level-ADC	output via DAC; ADC input short-circuited; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{VREFAD} = 22 µF	29	39	–	dB
$CMRR_{CD}$	common-mode rejection ratio for CD input mode	$R_{CD\_(L)\_GND}$ = 1 MΩ; resistance of CD player ground cable < 1 kΩ; f_i = 1 kHz	60	–	–	dB
AC characteristics PHONE and NAV inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
THD	total harmonic distortion of PHONE and NAV input signals at maximum input voltage	V_i = 0.75 V (RMS); f_i = 1 kHz; VOLMIX = 30H; measured at FLV and FRV outputs	40	–	–	dB
CMRR	common mode rejection ratio of PHONE and NAV input signals	V_i = 0.75 V(RMS); f_i = 1 kHz; VOLMIX = 30H	25	50	–	dB
R_i	input impedance of PHONE, NAV/AM_L and AM_R input signals		90	120	150	kΩ
$V_{i(max)(rms)}$	maximum input level of PHONE and NAV input signals (RMS value)	f_i = 1 kHz; VOLMIX = 30H	0.75	1	–	V
AC characteristics FM_RDS input; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
$V_{i(con)(max)(rms)}$	maximum conversion level of FM_RDS input (RMS value)	THD < 1%; VOLRDS = 00H	0.33	0.368	–	V
$R_{i(FM\_RDS)}$	input resistance FM_RDS input		40	60	72	kΩ
THD_{FM_RDS}	total harmonic distortion RDS ADC	f_c = 57 kHz	–60	–67	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²S-bus timing (see Fig.23)						
t_r	rise time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
t_f	fall time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
T_{cy}	bit clock cycle time		325	–	–	ns
$t_{BCK(H)}$	bit clock time HIGH	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{BCK(L)}$	bit clock time LOW	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{su(D)}$	data set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(D)}$	data hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{d(D)}$	data delay time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
$t_{su(WS)}$	word select set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(WS)}$	word select hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns

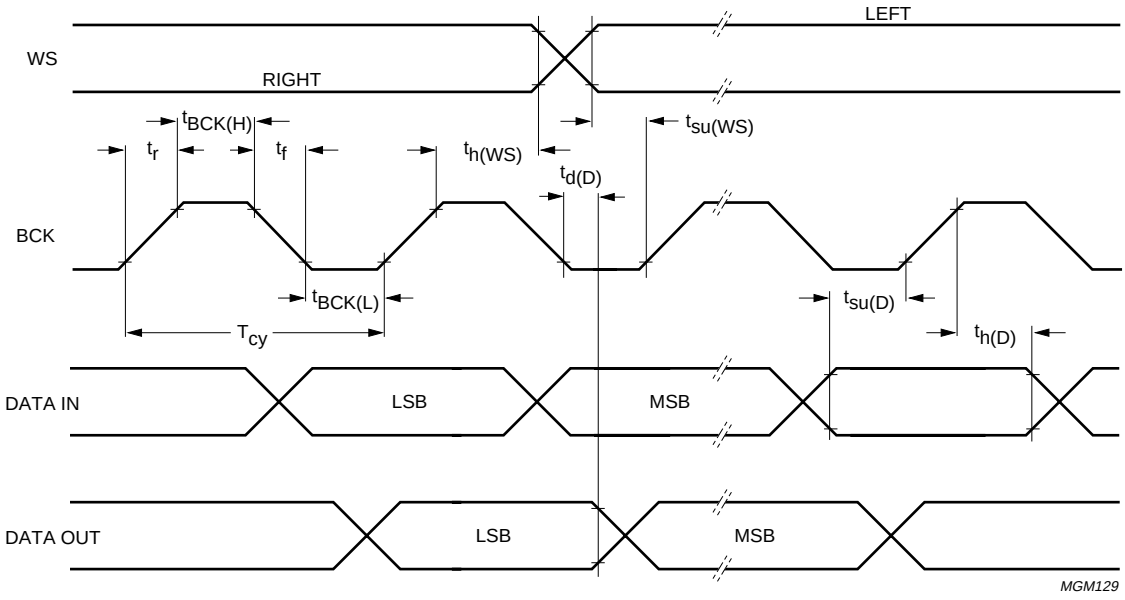


Fig.23 Input timing digital audio data inputs.

14 I²C-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time		0	–	0	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	rise time of both SDA and SCL signals	C_b in pF	–	1000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	C_b in pF	–	300	$20 + 0.1C_b$	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs
C_b	capacitive load for each bus line		–	400	–	400	pF
t_{SP}	pulse width of spikes to be suppressed by input filter		–	–	0	50	ns

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

20 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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22 PURCHASE OF PHILIPS I²C COMPONENTS

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