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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n107s-557

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6 BLOCK DIAGRAM

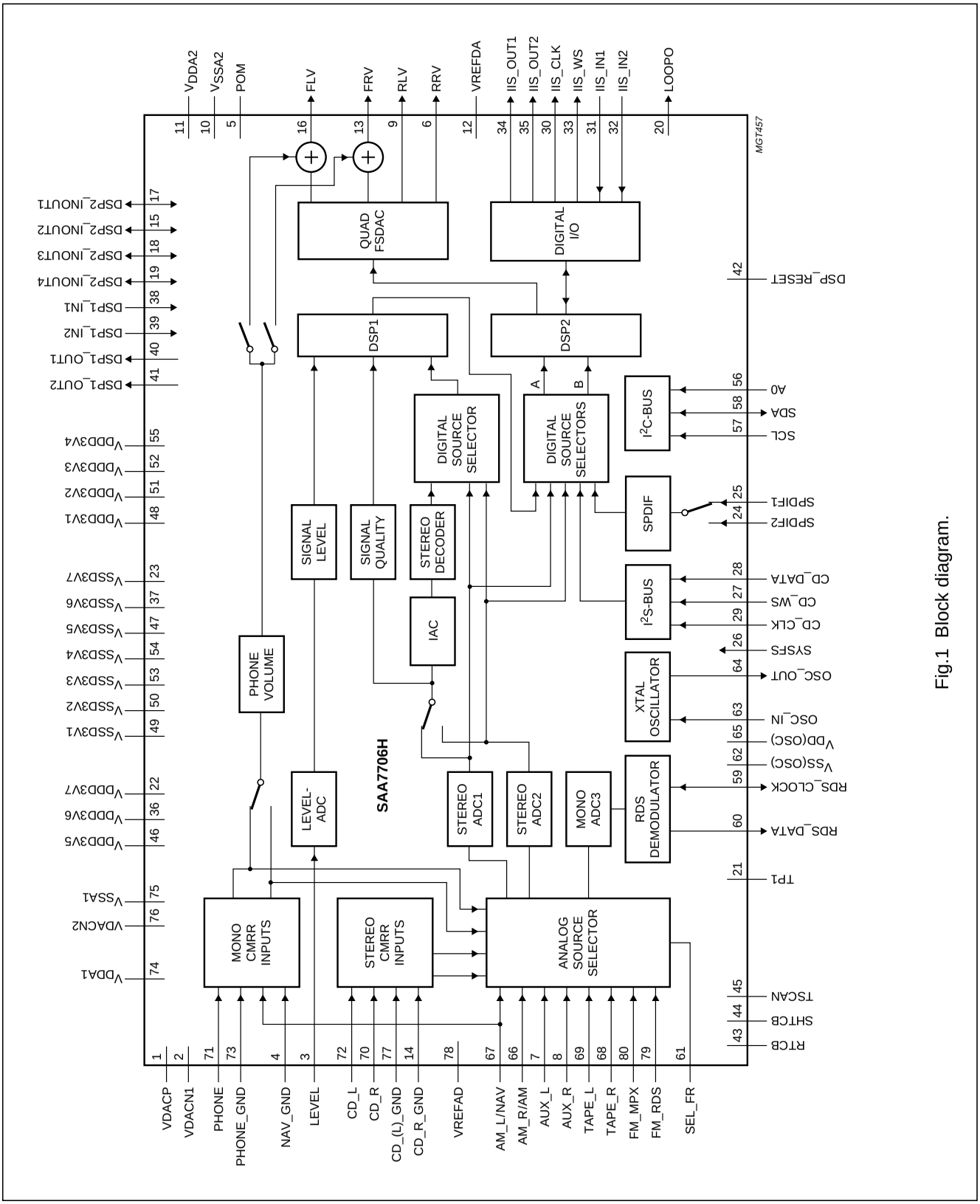


Fig.1 Block diagram.

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

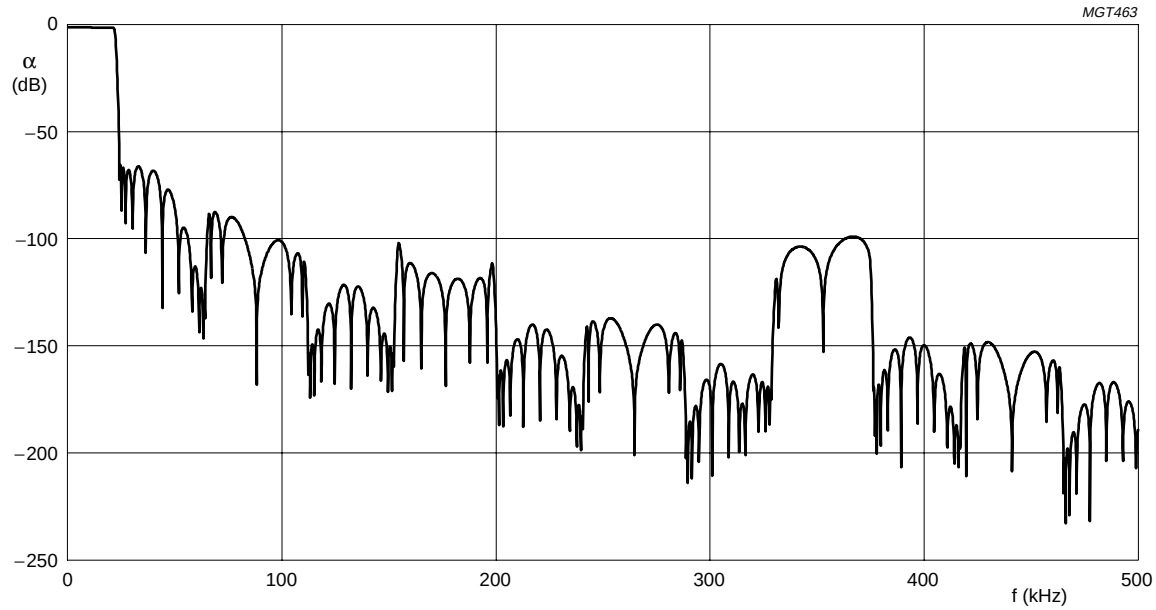


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

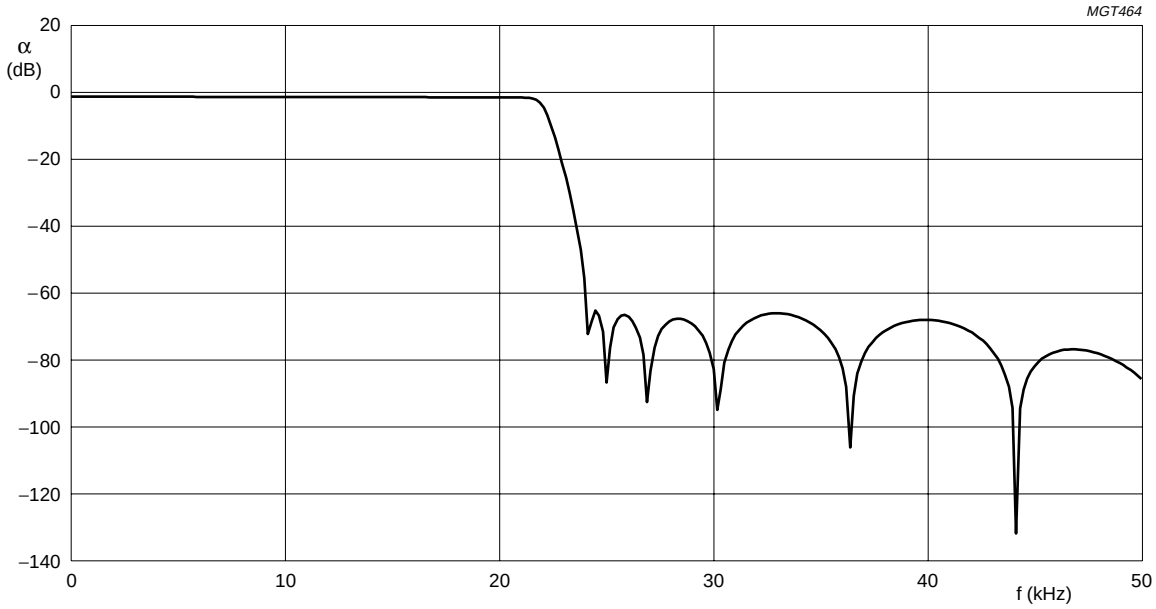


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

The outputs of the stereo decoder to the DSP1, which are all running on a sample frequency of 38 kHz are:

- Pilot presence indication: pilot-I. This 1-bit signal is LOW for a pilot frequency deviation <4 kHz and HIGH for a pilot frequency deviation >4 kHz and locked on a pilot tone.
- 'Left' and 'right' FM reception stereo signal: this is the 18-bit output of the stereo decoder after the matrix decoding.
- Noise level (see also Section 8.4.1): which is retrieved from the high-pass output of the MPX filter. The noise level is detected and filtered in the DSP1 and is used to optimize the FM weak signal processing.

Normally the FM_MPX input and the FM_RDS input have the same source. If the FM input contains a stereo radio channel, the pilot information is switched to the Digitally Controlled Sampling (DCS) clock generation and the DCS clock is locked to the 256 $\times$ 38 kHz of the pilot. In this case this locked frequency is also used for the RDS path ensuring the best possible performance.

Except from the above mentioned theoretical response also the non-flat frequency response of the ADC has to be compensated in the DSP1 program.

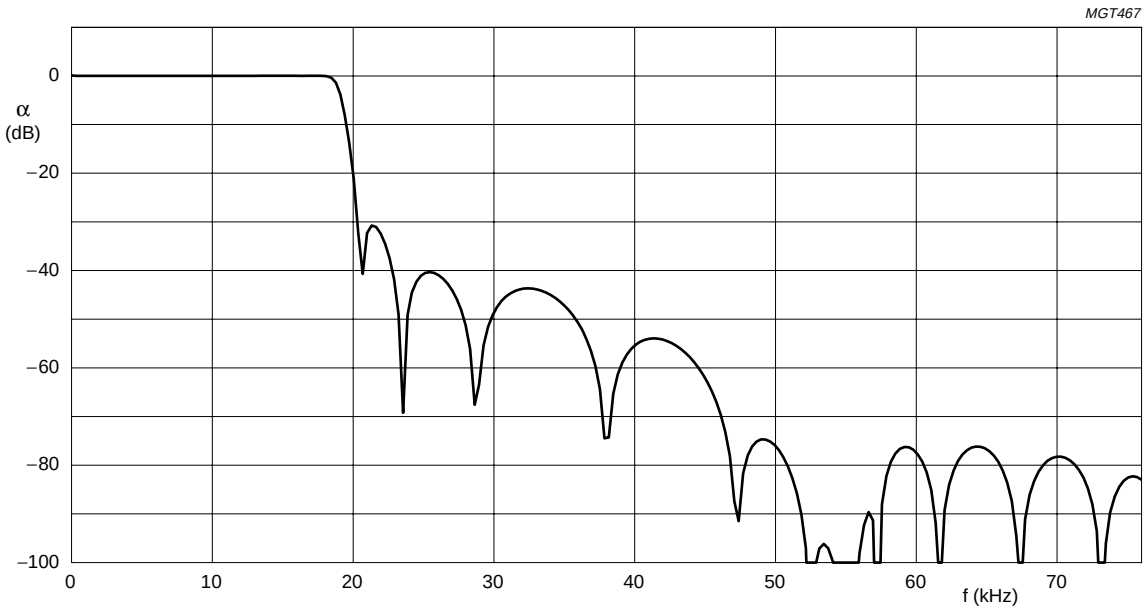


Fig.11 Transfer of MPX signal at the output of the stereo decoder.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I^2C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I^2C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I^2C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

8.7.3 Function of pin POM

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has past a particular level. This results in an almost dB-linear behaviour. This must prevent 'plop' effects during power on or off.

8.7.4 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate power supply of 3.3 V. A capacitor connected to this power supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

8.7.5 Pin VREFDA for internal reference

With two internal resistors half the supply voltage V_{DDA2} is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC.

In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin V_{SSA2}.

8.7.6 Supply of the filter stream DAC

The entire analog circuitry of the DACs and the operational amplifiers are supplied by 2 supply pins: V_{DDA2} and V_{SSA2}. V_{DDA2} must have sufficient decoupling to prevent total harmonic distortion degradation and to ensure a good power supply rejection ratio. The digital part of the DAC is fully supplied from the chip core supply.

8.8 Clock circuit and oscillator

The chip has an on-chip crystal clock oscillator. The block diagram of this Pierce oscillator is shown in Fig.13. The active element needed to compensate for the loss resistance of the crystal is the block G_m. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to the clock signal.

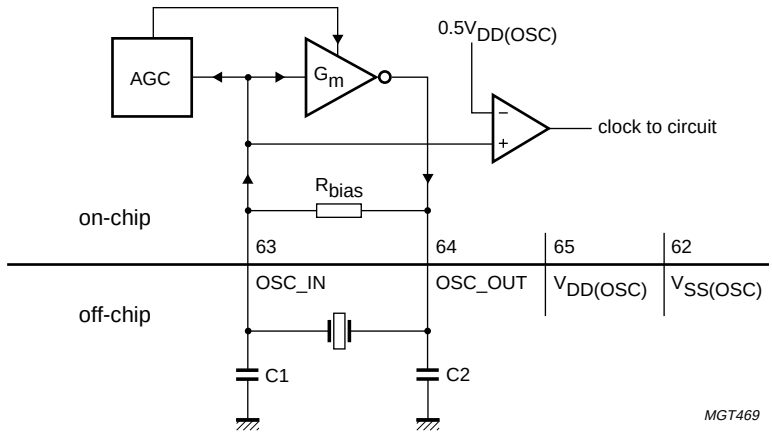


Fig.13 Block diagram oscillator circuit.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I^2S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I^2S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I^2C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I^2C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

9.6 I²C-bus memory map specification

The I²C-bus memory map contains all defined I²C-bus bits. The map is split up in two different sections, the hardware memory registers and the RAM definitions. In Table 5 the preliminary memory map is depicted. The hardware registers are memory map on the XRAM of DSP2. Table 5 shows the detailed memory map of those locations. All locations are acknowledged by the SAA7706H even if the user tries to write to a reserved space. The data in these sections will be lost. Reading from this locations will result in undefined data words.

Table 4 I²C-bus memory map

ADDRESS	FUNCTION	SIZE
2000H to 21FFH	YRAM (DSP2)	512 × 12 bits
1FF0H to 1FFFH	hardware registers	16 × 24 bits
1000H to 127FH	XRAM (DSP2)	640 × 24 bits
0FFFH	DSP CONTROL	1 × 16 bits
0800H to 097FH	YRAM (DSP1)	384 × 12 bits
0000H to 017FH	XRAM (DSP1)	384 × 18 bits

Table 5 I²C-bus memory map overview of hardware registers

DESCRIPTION	REGISTER
Hardware registers	
Program counter register DSP2	1FFFH
Status register DSP2	1FFEH
I/O configuration register DSP2	1FFDH
Phone, navigation and audio register	1FFCH
FM and RDS sensitivity register	1FFBH
Clock coefficient register	1FFAH
Clock settings register	1FF9H
IAC settings register	1FF8H
Selector register	1FF7H
CL_GEN register 4	1FF6H
CL_GEN register 3	1FF5H
CL_GEN register 2	1FF4H
CL_GEN register 1	1FF3H
Evaluation register	1FF0H
DSP control	
DSPs and general control register	0FFFH

10 LIMITING VALUES

In accordance with the Absolute Maximum Ratings System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+3.6	V
V_n	input voltage on any pin		–0.5	+5.5	V
I_{IK}	DC input clamping diode current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamping diode current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
$I_{O(sink/source)}$	DC output source or sink current	$–0.5 \text{ V} < V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD},I_{SS}	supply current per supply pin		–	±50	mA
T_{amb}	ambient operating temperature		–40	+85	°C
T_{stg}	storage temperature range		–65	+125	°C
V_{ESD}	ESD voltage				
	human body model	100 pF; 1500 Ω	2000	–	V
	machine model	200 pF; 0.5 μH; 10 Ω	200	–	V
$I_{lu(prot)}$	latch-up protection current	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	890	mW

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	45	K/W

12 CHARACTERISTICS

V_{DD} = 3 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; T_{amb} = –40 to +85 °C						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3.0	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
$I_{DDD(core)}$	supply current of the digital core part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	105	140	mA
$I_{DDD(peri)}$	supply current of the digital periphery part	without external load to ground	–	5	10	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
$I_{DDA(ADC)}$	supply current of the ADCs	zero input and output signal	–	15	26	mA
$I_{DDA(DAC)}$	supply current of the DACs	zero input and output signal	–	19	30	mA
$I_{DDA(osc)}$	supply current XTAL oscillator	functional mode	–	2	4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{tot}	total power dissipation	DSP1 at 50 MHz, DSP2 at 62.9 MHz	–	540	750	mW
Digital I/O; T_{amb} = −40 to +85 °C; V_{DD} = 3 to 3.6 V						
V_{IH}	HIGH-level input voltage for all digital inputs and I/Os		2.0	–	–	V
V_{IL}	LOW-level input voltage for all digital inputs and I/Os		–	–	0.8	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	–	V
V_{OH}	HIGH-level output voltage	standard output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		5 ns slew rate output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		10 ns slew rate output; I_O = –2 mA	V_{DD} – 0.4	–	–	V
		20 ns slew rate output; I_O = –1 mA	V_{DD} – 0.4	–	–	V
V_{OL}	LOW-level output voltage	standard output; I_O = 4 mA	–	–	0.4	V
		5 ns slew rate output; I_O = 4mA	–	–	0.4	V
		10 ns slew rate output; I_O = 2 mA	–	–	0.4	V
		20 ns slew rate output; I_O = 1 mA	–	–	0.4	V
		I^2C-bus output; I_O = 4 mA	–	–	0.4	V
I_{LO}	output leakage current 3-state outputs	V_O = 0 V or V_{DD}	–	–	±5	µA
R_{pd}	internal pull-down resistor to V_{SS}		24	50	140	kΩ
R_{pu}	internal pull-up resistor to V_{DD}		30	50	100	kΩ
C_i	input capacitance		–	–	3.5	pF
$t_{i(r)}$,$t_{i(f)}$	input rise and fall times	V_{DD} = 3.6 V	–	6	200	ns
$t_{o(t)}$	output transition time	standard output; C_L = 30 pF	–	3.5	–	ns
		5 ns slew rate output; C_L = 30 pF	–	5	–	ns
		10 ns slew rate output; C_L = 30 pF	–	10	–	ns
		20 ns slew rate output; C_L = 30 pF	–	20	–	ns
		I^2C-bus output; C_b = 400 pF	60	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio					
	CD, TAPE, AM and AUX input signals	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS); f_s = 44.1 kHz	85	90	–	dB
	FM_MPX input signal mono	input signal at 1 kHz; bandwidth = 19 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	80	83	–	dB
	FM_MPX input signal stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
α_{19}	carrier and harmonic suppression at the output	pilot signal frequency = 19 kHz	–	81	–	dB
		unmodulated	–	98	–	dB
α_{38}	carrier and harmonic suppression at the output	subcarrier frequency = 38 kHz	–	83	–	dB
		unmodulated	–	91	–	dB
α_{57}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 57 kHz	–	83	–	dB
		unmodulated	–	96	–	dB
α_{76}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 76 kHz	–	84	–	dB
		unmodulated	–	94	–	dB
$IM_{\alpha 10}$	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz	77	–	–	dB
$IM_{\alpha 13}$	intermodulation	f_{mod} = 13 kHz; f_{spur} = 1 kHz	76	–	–	dB
$\alpha_{57(VF)}$	traffic radio suppression	f = 57 kHz	–	110	–	dB
$\alpha_{67(SCA)}$	Subsidiary Communication Authority (SCA) suppression	f = 67 kHz	–	110	–	dB
α_{114}	adjacent channel suppression	f = 114 kHz	–	110	–	dB
α_{190}	adjacent channel suppression	f = 190 kHz	–	110	–	dB
$V_{th(pilot)(rms)}$	pilot threshold voltage (RMS value) at pin DSP1_OUT1	stereo on; VOLFM = 07H	–	35.5	–	mV
		stereo off; VOLFM = 07H	–	35.4	–	mV
hys	hysteresis of $V_{th(pilot)(rms)}$		–	0	–	dB
α_{cs1}	channel separation FM-stereo input	f_i = 1 kHz	40	45	–	dB
		f_i = 10 kHz	25	30	–	dB
α_{cs2}	channel separation CD, TAPE, AM and AUX input signals		60	70	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²S-bus timing (see Fig.23)						
t_r	rise time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
t_f	fall time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
T_{cy}	bit clock cycle time		325	–	–	ns
$t_{BCK(H)}$	bit clock time HIGH	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{BCK(L)}$	bit clock time LOW	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{su(D)}$	data set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(D)}$	data hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{d(D)}$	data delay time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
$t_{su(WS)}$	word select set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(WS)}$	word select hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns

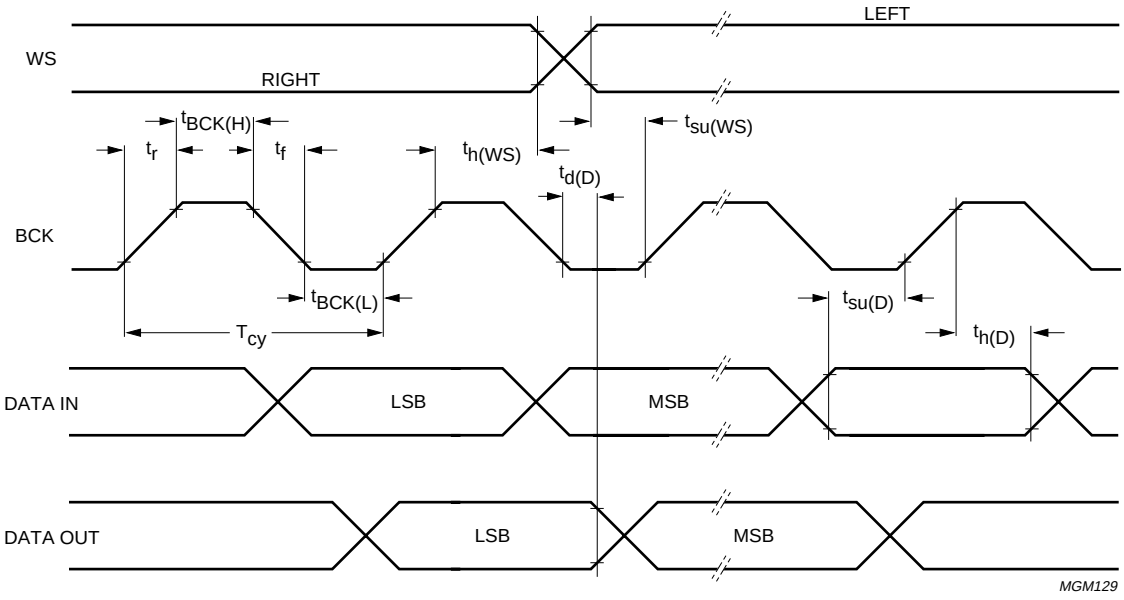


Fig.23 Input timing digital audio data inputs.

14 I²C-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time		0	–	0	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	rise time of both SDA and SCL signals	C_b in pF	–	1000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	C_b in pF	–	300	$20 + 0.1C_b$	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs
C_b	capacitive load for each bus line		–	400	–	400	pF
t_{SP}	pulse width of spikes to be suppressed by input filter		–	–	0	50	ns

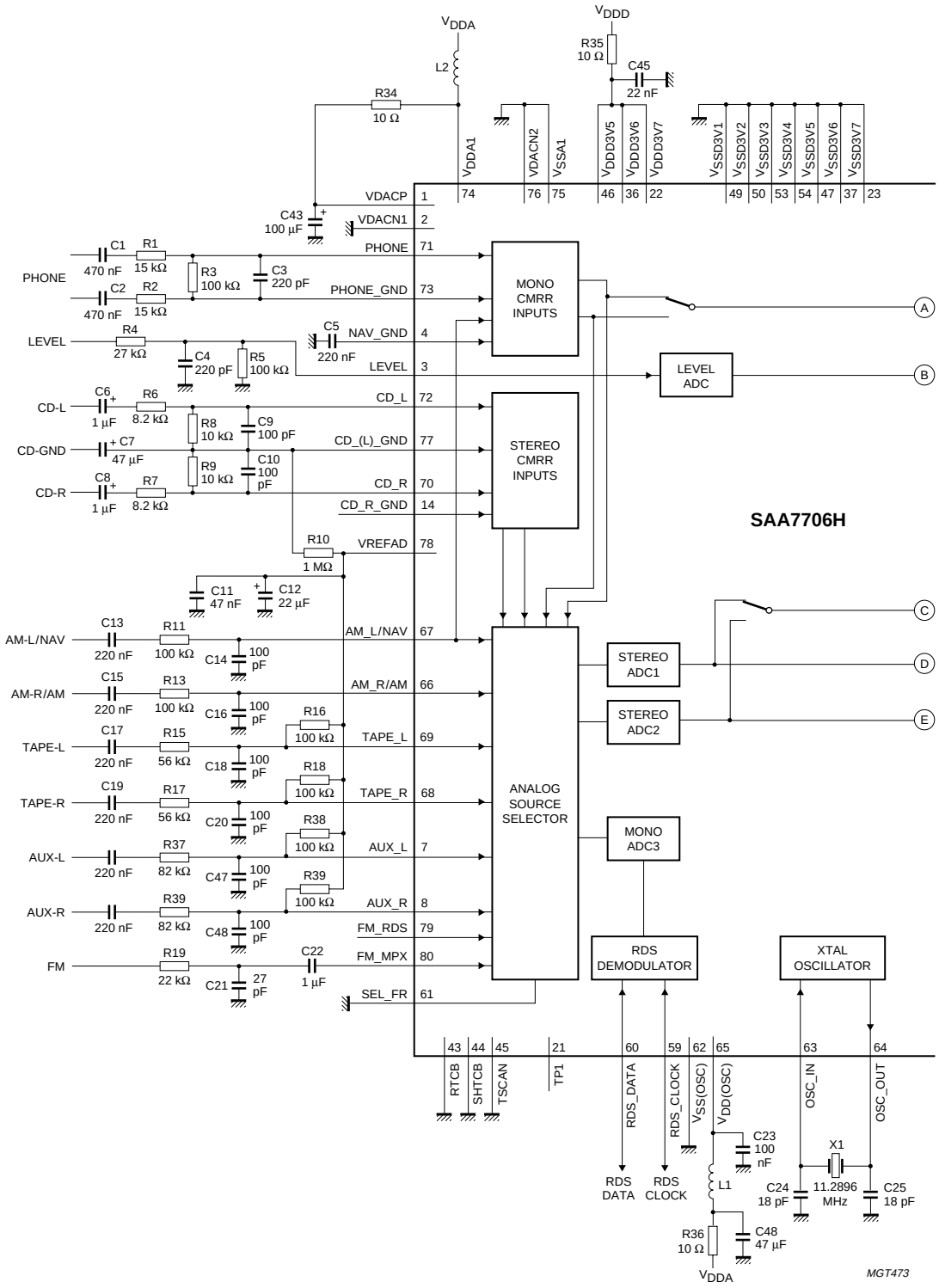
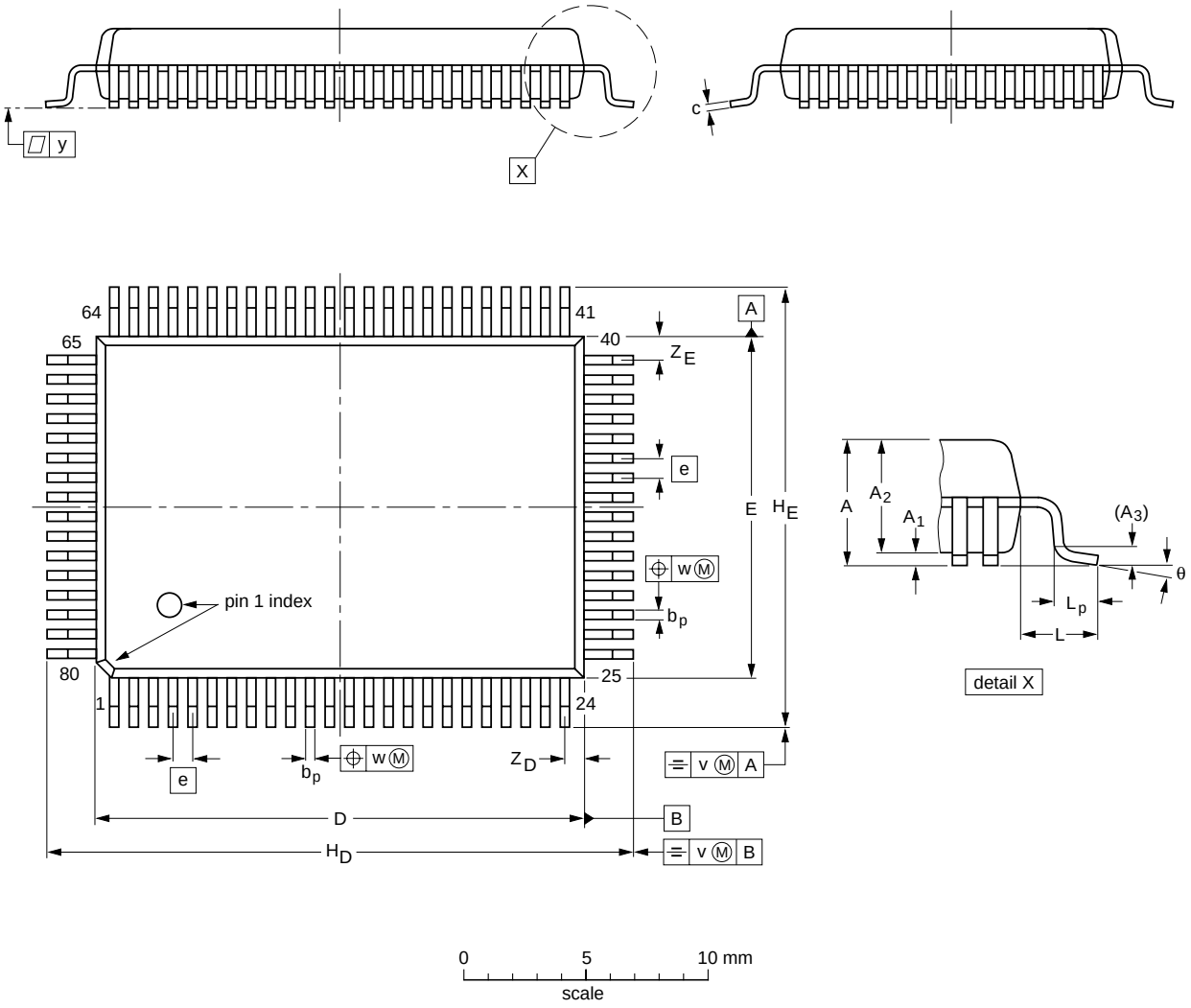


Fig.25 Application diagram (continued in Fig.26).

17 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				~~97-08-01~~ 99-12-27

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.