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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n210-518

CONTENTS

7 PINNING

SYMBOL	PIN	PIN TYPE	DESCRIPTION
VDACP	1	apio	positive reference voltage ADC1, ADC2, ADC3 and level-ADC
VDACN1	2	apio	ground reference voltage ADC1
LEVEL	3	apio gsmcap	LEVEL input pin; via this pin the level of the FM signal or level of the AM signal is fed to the DSP1; the level information is used in the DSP1 for dynamic signal processing
NAV_GND	4	apio gsmcap	common mode reference input pin of the navigation signal (pin AM_L/NAV)
POM	5	apio	power-on mute of the QFSDAC; timing is determined by an external capacitor
RRV	6	apio	rear; right audio output of the QFSDAC
AUX_L	7	apio	left channel of analog AUX input
AUX_R	8	apio	right channel of analog AUX input
RLV	9	apio	rear; left audio output of the QFSDAC
V_{SSA2}	10	vssco	ground supply analog part of the QFSDAC and SPDIF bitslicer
V_{DDA2}	11	vddco	positive supply analog part of the QFSDAC and SPDIF bitslicer
VREFDA	12	apio	voltage reference of the analog part of QFSDAC
FRV	13	apio	front; right audio output of the QFSDAC
CD_R_GND	14	apio	common-mode reference input pin for analog CD_R or TAPE_R in the event of separated ground reference pins for left and right are used
DSP2_INOUT2	15	bpts5thdt5v	flag input/output 2 of the DSP2-core (DSP2-flag) I^2C-bus configurable
FLV	16	apio	front; left audio voltage output of the QFSDAC
DSP2_INOUT1	17	bpts5thdt5v	flag input/output 1 of the DSP2-core (DSP2-flag) I^2C-bus configurable
DSP2_INOUT3	18	bpts5thdt5v	flag input/output 3 of the DSP2-core (DSP2-flag) I^2C-bus configurable
DSP2_INOUT4	19	bpts5thdt5v	flag input/output 4 of the DSP2-core (DSP2-flag) I^2C-bus configurable
LOOPO	20	bpts5tht5v	SYSCLK output ($256f_s$)
TP1	21	ipthdt5v	for test purpose only; this pin may be left open or connected to ground
V_{DDD3V7}	22	vdde	positive supply (peripheral cells only)
V_{SSD3V7}	23	vsse	ground supply (peripheral cells only)
SPDIF2	24	apio	SPDIF input 2; can be selected instead of SPDIF1 via I^2C-bus bit
SPDIF1	25	apio	SPDIF input 1; can be selected instead of SPDIF2 via I^2C-bus bit
SYSFS	26	ipthdt5v	system f_s clock input
CD_WS	27	ipthdt5v	digital CD-source word select input; I^2S-bus or LSB-justified format
CD_DATA	28	bpts10thdt5v	digital CD-source left-right data input; I^2S-bus or LSB-justified format
CD_CLK	29	ipthdt5v	digital CD-source clock input I^2S-bus or LSB-justified format
IIS_CLK	30	ots10ct5v	clock output for external I^2S-bus receiver; for example headphone or subwoofer
IIS_IN1	31	ipthdt5v	data 1 input for external I^2S-bus transmitter; e.g. audio co-processor
IIS_IN2	32	ipthdt5v	data 2 input for external I^2S-bus transmitter; e.g. audio co-processor
IIS_WS	33	ots10ct5v	word select output for external I^2S-bus receiver; for example headphone or subwoofer
IIS_OUT1	34	ots10ct5v	data 1 output for external I^2S-bus receiver or co-processor
IIS_OUT2	35	ots10ct5v	data 2 output for external I^2S-bus receiver or co-processor

SYMBOL	PIN	PIN TYPE	DESCRIPTION
V_{DDD3V6}	36	vdde	positive supply (peripheral cells only)
V_{SSD3V6}	37	vsse	ground supply (peripheral cells only)
DSP1_IN1	38	bpts10thdt5v	flag input 1 of the DSP1-core
DSP1_IN2	39	bpts10thdt5v	flag input 2 of the DSP1-core
DSP1_OUT1	40	op4mc	flag output 1 of the DSP1-core
DSP1_OUT2	41	op4mc	flag output 2 of the DSP1-core
DSP_RESET	42	iptut5v	general reset of chip (active LOW)
RTCB	43	ipthdt5v	asynchronous reset test control block; connect to ground (internal pull-down)
SHTCB	44	ipthdt5v	shift clock test control block (internal pull-down)
TSCAN	45	ipthdt5v	scan control active high (internal pull-down)
V_{DDD3V5}	46	vdde	positive supply (peripheral cells only)
V_{SSD3V5}	47	vsse	ground supply (peripheral cells only)
V_{DDD3V1}	48	vddi	positive supply (core only)
V_{SSD3V1}	49	vssis	ground supply (core only)
V_{SSD3V2}	50	vssco	ground supply (core only)
V_{DDD3V2}	51	vddco	positive supply (core only)
V_{DDD3V3}	52	vddco	positive supply (core only)
V_{SSD3V3}	53	vssco	ground supply (core only)
V_{SSD3V4}	54	vssis	ground supply (core only)
V_{DDD3V4}	55	vddi	positive supply (core only)
A0	56	ipthdt5v	slave sub-address I^2C-bus selection or serial data input test control block
SCL	57	iptht5v	serial clock input I^2C-bus
SDA	58	iic400kt5v	serial data input/output I^2C-bus
RDS_CLOCK	59	bpts10tht5v	radio data system bit clock output or RDS external clock input I^2C-bus bit controlled
RDS_DATA	60	ops10c	radio data system data output
SEL_FR	61	iptht5v	AD input selection switch to enable high ohmic FM_MPX input at fast tuner search on FM_RDS input
$V_{SS(OSC)}$	62	vssco	ground supply (crystal oscillator only)
OSC_IN	63	apio	crystal oscillator input
OSC_OUT	64	apio	crystal oscillator output
$V_{DD(OSC)}$	65	vddco	positive supply (crystal oscillator only)
AM_R/AM	66	apio gsmcap	right channel AM audio frequency or AM input in the event of mono; analog input pin
AM_L/NAV	67	apio gsmcap	left channel AM audio frequency or input of common mode navigation signal; analog input pin
TAPE_R	68	apio gsmcap	right channel of analog TAPE input
TAPE_L	69	apio gsmcap	left channel of analog TAPE input
CD_R	70	apio gsmcap	right channel of analog CD input
PHONE	71	apio gsmcap	common mode PHONE signal, analog input pin
CD_L	72	apio gsmcap	left channel of analog CD input

8 FUNCTIONAL DESCRIPTION

8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via I^2C-bus.

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

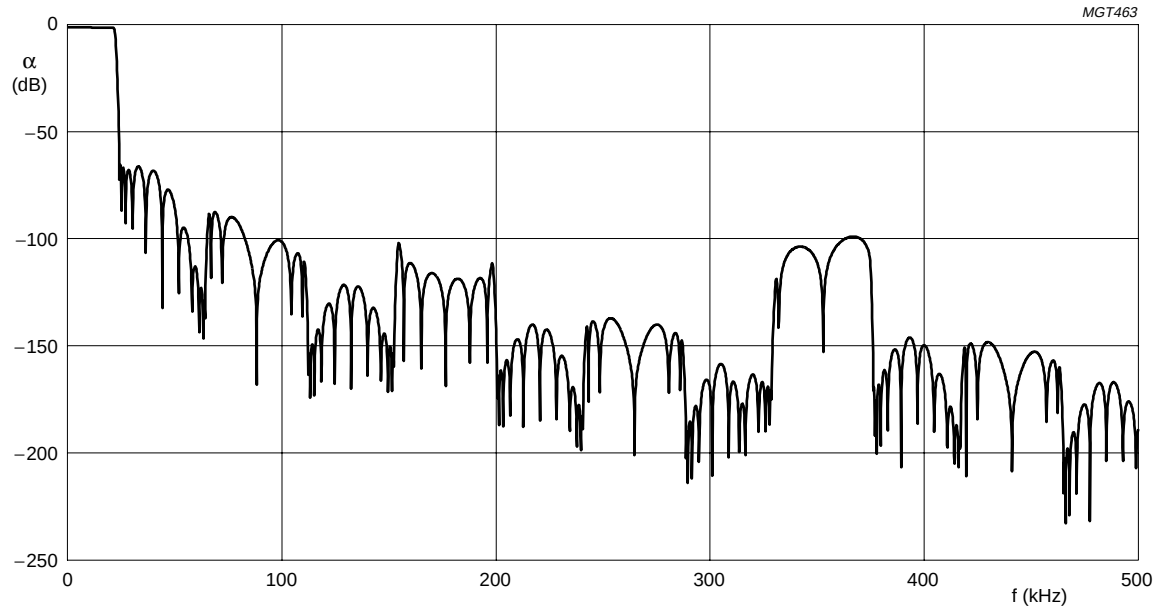


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.4 Signal path from FM_MPX input to IAC and stereo decoder

The FM_MPX signal is after selection available at one of three ADCs (ADC1, 2 and 3). The multiplex FM signal is converted to the digital domain in ADC1, 2 and 3 through a bitstream ADC. Improved performance for FM stereo can be achieved by means of adapting the noise shaper curve of the ADC to a higher bandwidth.

The first decimation takes place in two down-sample filters. These decimation filters are switched by means of the I^2C-bus bit wide_narrow in the wide or narrow band position. In the event of FM reception it must be in the narrow position.

After selection of one of the ADCs, the FM_MPX path it is followed by the IAC and the FM stereo decoder. One of the two MPX filter outputs contains the multiplex signal with a frequency range of 0 to 60 kHz. The overall low-pass frequency response of the decimation filters is shown in Fig.10.

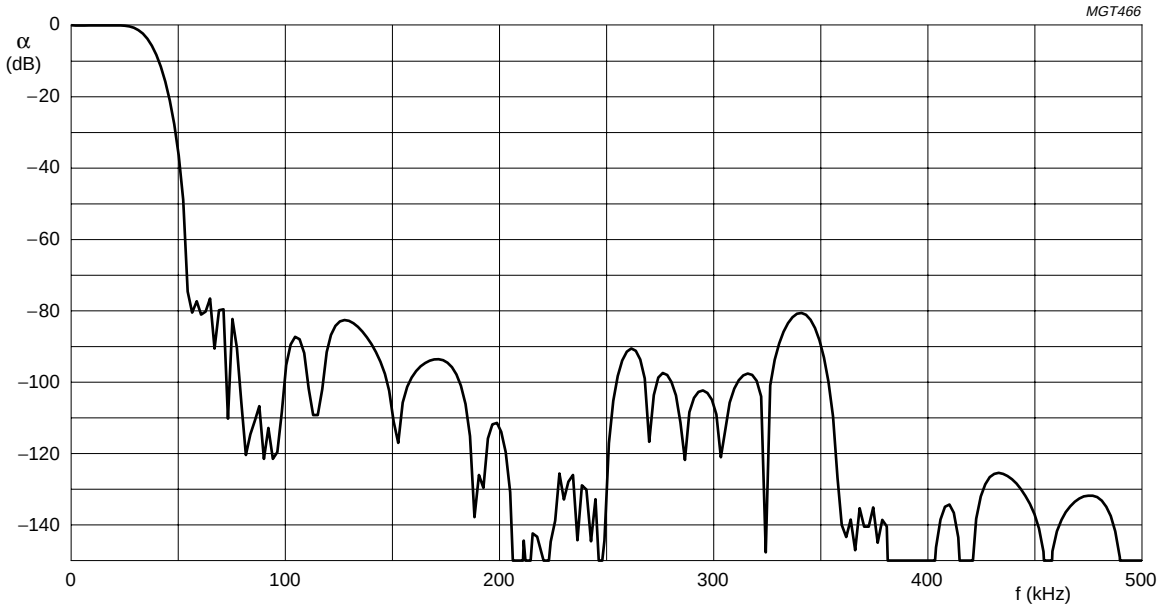
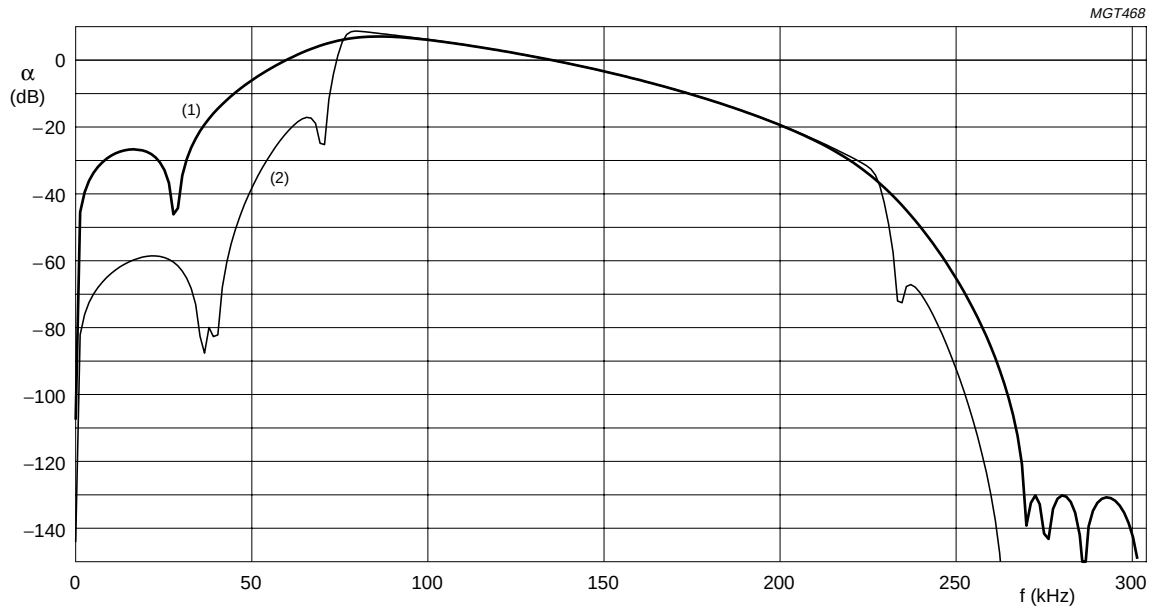


Fig.10 Overall frequency response of ADC1, ADC2 and decimation filters.

8.4.1 NOISE LEVEL

The high-pass 1 (HP1 or narrow band noise level filter) output of the second MPX decimation filter in a band from 60 kHz to 120 kHz is detected with an envelope detector and decimated to a frequency of 38 kHz. The response time of the detector is 100 µs. Another option is the high-pass 2 (HP2 or wide band noise level filter). This output of the first MPX decimation filter is in a band from 60 to 240 kHz. It has the same properties and is also decimated to the same 38 kHz. Which of the signals is used (HP1 or HP2) is determined by the I^2C-bus bit sel_nsdec.

The resulting noise information is rectified and has a word length of 10 bits. This means that the lowest and/or the highest possible level is not used. The noise level can be detected and filtered in the DSP1-core and be used to optimize the FM weak signal processing. The transfer curves of both filters before decimation are shown in Fig.12.



(1) Noise with wide band digital filter.
(2) Noise with small band digital filter.

Fig.12 Frequency response of noise level before decimation.

8.4.2 MONO OR STEREO SWITCHING

The DCS block uses a sample rate converter to derive from the XTAL clock, via a PLL, a 512 multiple of 19 kHz (9.728 MHz). In the event of mono reception the DCS circuit generates a preset frequency of n × 19 kHz ±2 Hz. In the event of stereo reception the frequency is exactly n × 19 kHz (DCS locked to N × pilot tone). The detection of the pilot and the stereo indication is done in the DSP program.

8.4.3 THE AUTOMATIC LOCK SYSTEM

The VCO of the DCS block will be at 19 kHz ±2 Hz exact based in the event of no-pilot FM_MPX reception or in the event of only RDS reception. In the event of stereo reception the phase error is zero for a pilot tone with a frequency of exactly 19 kHz.

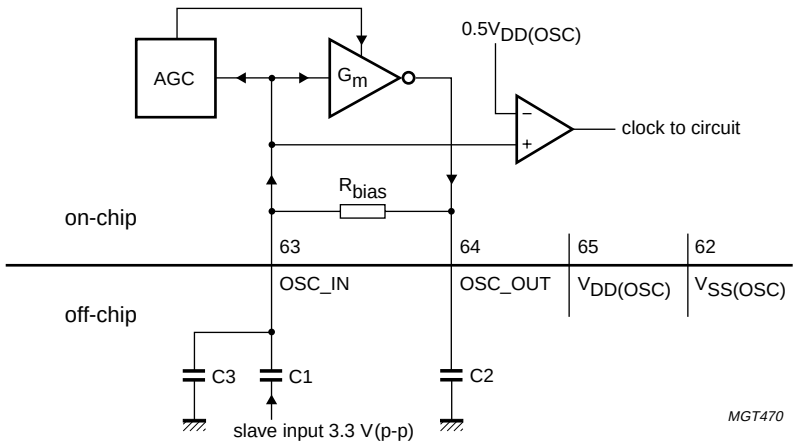


Fig.14 Block diagram of the oscillator in slave mode.

8.8.1 Supply of the crystal oscillator

The power supply connections of the oscillator are separated from the other supply lines. This is done to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin $V_{SS(OSC)}$ is used as ground supply and pin $V_{DD(OSC)}$ as positive supply. A series resistor plus capacitance is required for proper operating on pin $V_{DD(OSC)}$, see Figs 25 and 26. See also important remark in Section 8.10.

8.9 The phase-locked loop circuit to generate the DSPs and other clocks

There are several reasons why a PLL circuit is used to generate the clock for the DSPs:

- The PLL makes it possible to switch in the rare cases that tuning on a multiple of the DSP clock frequency occurs to a slightly higher frequency for the clock of the DSP. In this way an undisturbed reception with respect to the DSP clock frequency is possible.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 100 MHz, are always third overtone crystals and must also be manufactured on customer demand. This makes these crystals expensive. The PLL1 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256×44.1 kHz = 11.2896 MHz crystal is chosen. This type of crystal is widely used.
- Although a multiple of the frequency of the used crystal of 11.2896 MHz falls within the FM reception band, this will not disturb the reception because the relatively low frequency crystal is driven in a controlled way and the sine wave of the crystal has in the FM reception band only very minor harmonics.

8.10 Supply of the digital part (V_{DDD3V1} to V_{DDD3V4})

The supply voltage on pins V_{DDD3V1} to V_{DDD3V4} must be for at least 10 ms earlier active than the supply voltage applied to pin $V_{DD(OSC)}$.

8.11 CL_GEN, audio clock recovery block

When an external I^2S-bus or SPDIF source is connected, the FSDAC circuitry needs an $256f_s$ related clock. This clock is recovered from either the incoming WS of the digital serial input or the WS derived from the SPDIF1/SPDIF2 input. There is also a possibility to provide the chip with an external clock, in that case it must be a $256f_s$ clock with a fixed phase relation to the source.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14.3 DIGITAL DATA STREAM FORMATS

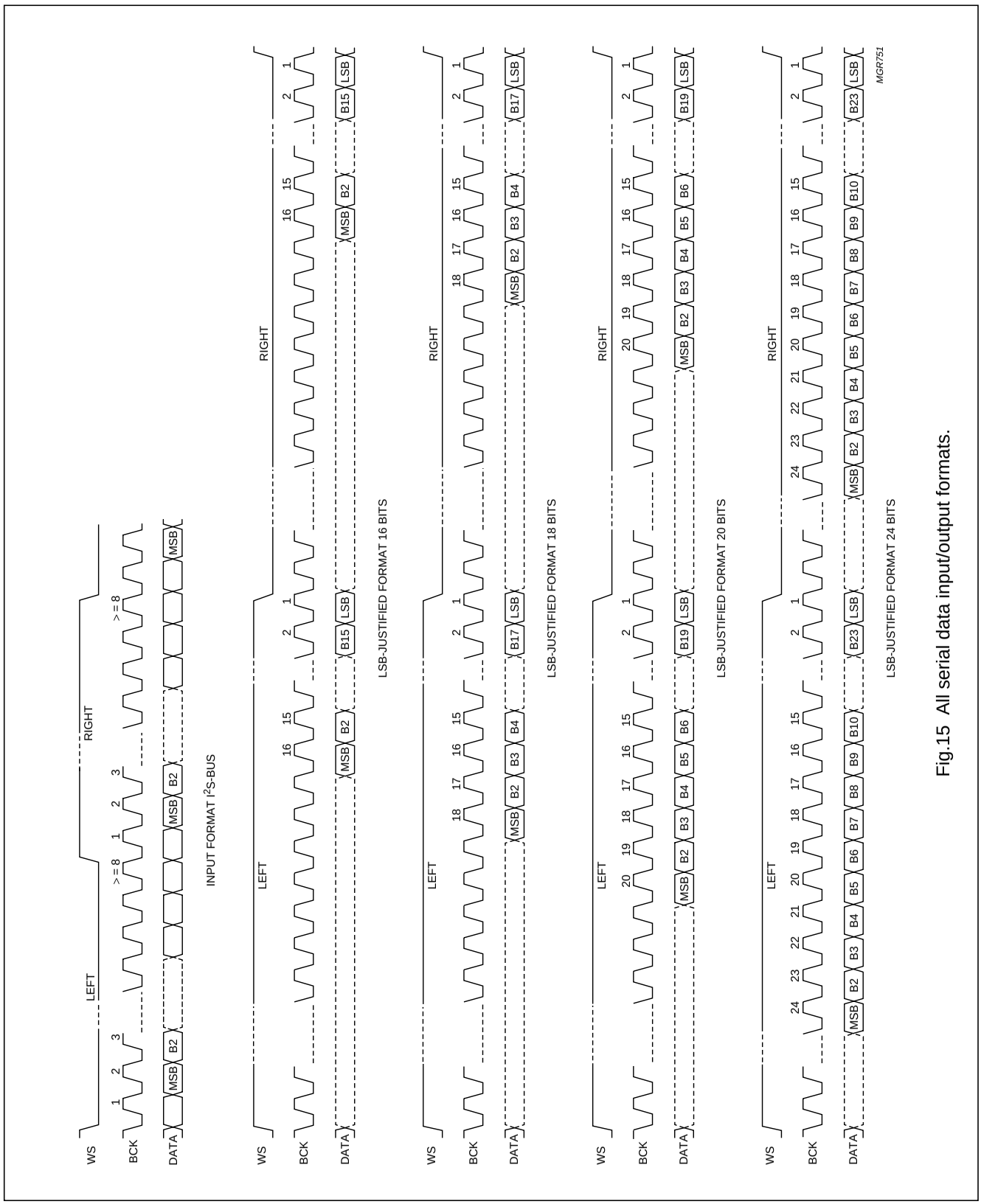


Fig.15 All serial data input/output formats.

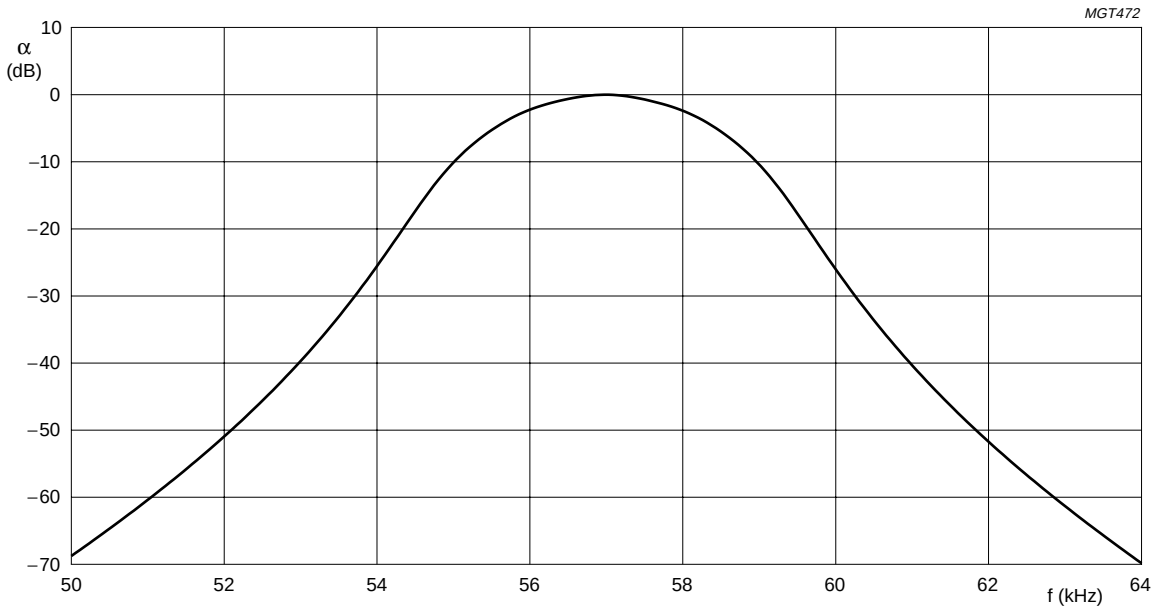


Fig.17 Detailed frequency response curve RDS channel.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDS_CLOCK and RDS_DATA. In the event of FM-stereo reception the clock of the total chip is locked to the stereo pilot (19 kHz multiple). In the event of FM-mono the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases like AM reception or tape, the DCS circuit has to be set in a preset position by means of an I^2C-bus bit. Under these conditions the RDS system is always clocked by the DCS clock in a 38 kHz (4×9.5 kHz) based sequence.

8.15.2 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 μs after the clock transition. The timing of the data change is 100 μs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller. The RDS timing is shown in Fig.18. During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

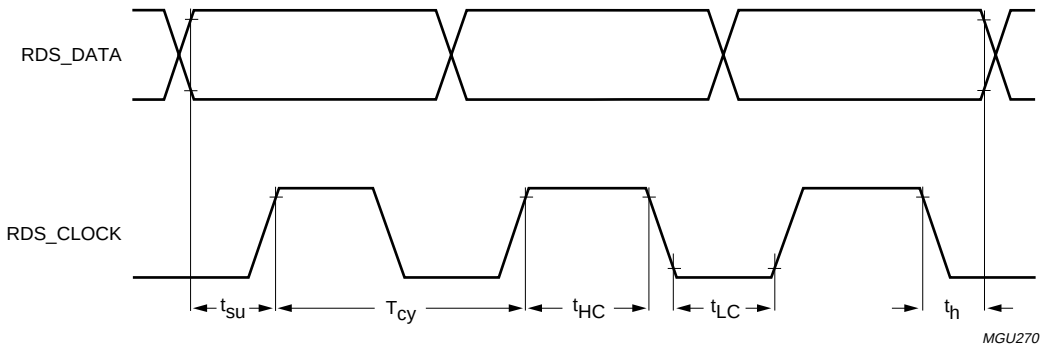


Fig.18 RDS timing in the direct output mode.

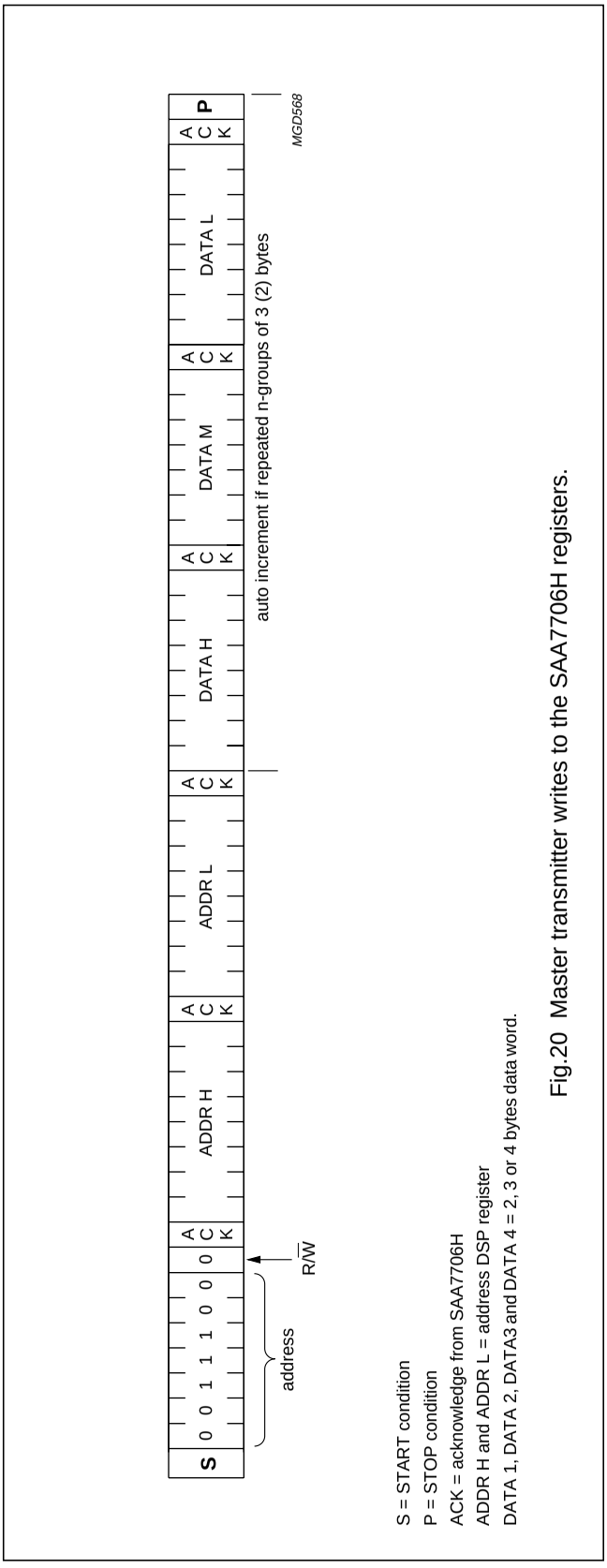
8.15.3 Buffering of RDS data

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microcontroller for every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

8.15.4 Buffer interface

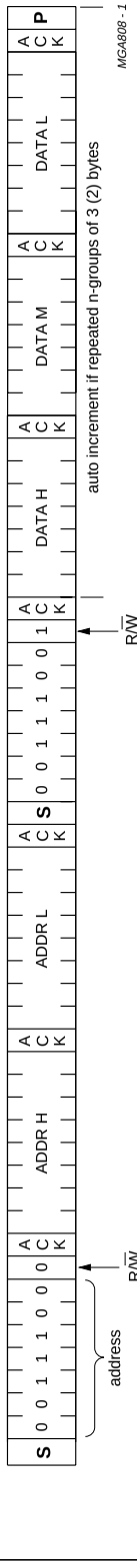
The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled down and the buffer is overwritten. The microcontroller has to monitor the data line in at most every 13.5 ms. This mode can be selected via an I^2C-bus.

In Fig.19 the interface signals from the RDS decoder and the microcontroller in buffer mode are shown. When the buffer is filled with 16 bits the data line is pulled down. The data line will remain LOW until reading of the buffer is started by pulling down the clock line. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the line HIGH. The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH. When a new 16-bit buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.



S = START condition
P = STOP condition
ACK = acknowledge from SAA7706H
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.20 Master transmitter writes to the SAA7706H registers.



S = START condition
Sr = repeated START condition
P = STOP condition
ACK = acknowledge from SAA7706H (SDA LOW)
R = repeat n-times the 2, 3 or 4 bytes data group
NA = negative acknowledge master (SDA HIGH)
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA 3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.21 Master transmitter reads from the SAA7706H registers.

9.6 I²C-bus memory map specification

The I²C-bus memory map contains all defined I²C-bus bits. The map is split up in two different sections, the hardware memory registers and the RAM definitions. In Table 5 the preliminary memory map is depicted. The hardware registers are memory map on the XRAM of DSP2. Table 5 shows the detailed memory map of those locations. All locations are acknowledged by the SAA7706H even if the user tries to write to a reserved space. The data in these sections will be lost. Reading from this locations will result in undefined data words.

Table 4 I²C-bus memory map

ADDRESS	FUNCTION	SIZE
2000H to 21FFH	YRAM (DSP2)	512 × 12 bits
1FF0H to 1FFFH	hardware registers	16 × 24 bits
1000H to 127FH	XRAM (DSP2)	640 × 24 bits
0FFFH	DSP CONTROL	1 × 16 bits
0800H to 097FH	YRAM (DSP1)	384 × 12 bits
0000H to 017FH	XRAM (DSP1)	384 × 18 bits

Table 5 I²C-bus memory map overview of hardware registers

DESCRIPTION	REGISTER
Hardware registers	
Program counter register DSP2	1FFFH
Status register DSP2	1FFEH
I/O configuration register DSP2	1FFDH
Phone, navigation and audio register	1FFCH
FM and RDS sensitivity register	1FFBH
Clock coefficient register	1FFAH
Clock settings register	1FF9H
IAC settings register	1FF8H
Selector register	1FF7H
CL_GEN register 4	1FF6H
CL_GEN register 3	1FF5H
CL_GEN register 2	1FF4H
CL_GEN register 1	1FF3H
Evaluation register	1FF0H
DSP control	
DSPs and general control register	0FFFH

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{tot}	total power dissipation	DSP1 at 50 MHz, DSP2 at 62.9 MHz	–	540	750	mW
Digital I/O; T_{amb} = −40 to +85 °C; V_{DD} = 3 to 3.6 V						
V_{IH}	HIGH-level input voltage for all digital inputs and I/Os		2.0	–	–	V
V_{IL}	LOW-level input voltage for all digital inputs and I/Os		–	–	0.8	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	–	V
V_{OH}	HIGH-level output voltage	standard output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		5 ns slew rate output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		10 ns slew rate output; I_O = –2 mA	V_{DD} – 0.4	–	–	V
		20 ns slew rate output; I_O = –1 mA	V_{DD} – 0.4	–	–	V
V_{OL}	LOW-level output voltage	standard output; I_O = 4 mA	–	–	0.4	V
		5 ns slew rate output; I_O = 4mA	–	–	0.4	V
		10 ns slew rate output; I_O = 2 mA	–	–	0.4	V
		20 ns slew rate output; I_O = 1 mA	–	–	0.4	V
		I^2C-bus output; I_O = 4 mA	–	–	0.4	V
I_{LO}	output leakage current 3-state outputs	V_O = 0 V or V_{DD}	–	–	±5	µA
R_{pd}	internal pull-down resistor to V_{SS}		24	50	140	kΩ
R_{pu}	internal pull-up resistor to V_{DD}		30	50	100	kΩ
C_i	input capacitance		–	–	3.5	pF
$t_{i(r)}$,$t_{i(f)}$	input rise and fall times	V_{DD} = 3.6 V	–	6	200	ns
$t_{o(t)}$	output transition time	standard output; C_L = 30 pF	–	3.5	–	ns
		5 ns slew rate output; C_L = 30 pF	–	5	–	ns
		10 ns slew rate output; C_L = 30 pF	–	10	–	ns
		20 ns slew rate output; C_L = 30 pF	–	20	–	ns
		I^2C-bus output; C_b = 400 pF	60	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

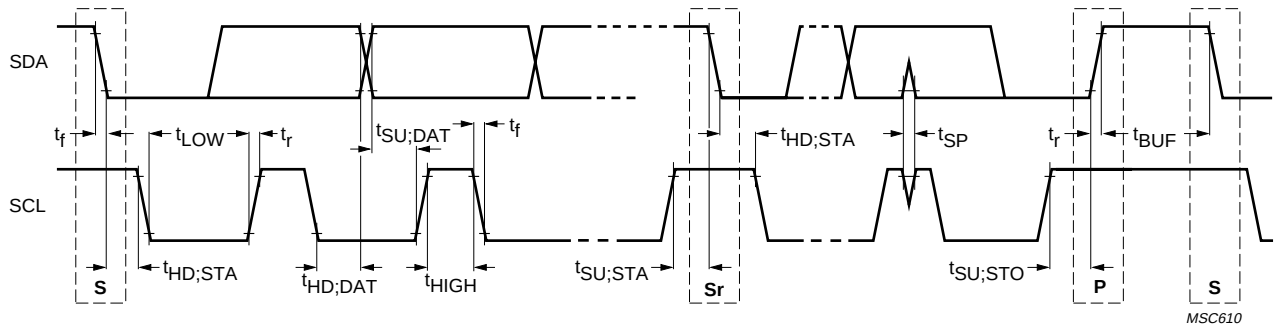


Fig.24 Definition of timing on the I²C-bus.

15 SOFTWARE DESCRIPTION

The use and description of the software features of the SAA7706H will be described in the separate application manual.

16 APPLICATION DIAGRAM

The application diagram shown in Figs 25 and 26 must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I²S-bus inputs of the CD-input are not used. For the real application set-up the information of the application report is necessary.

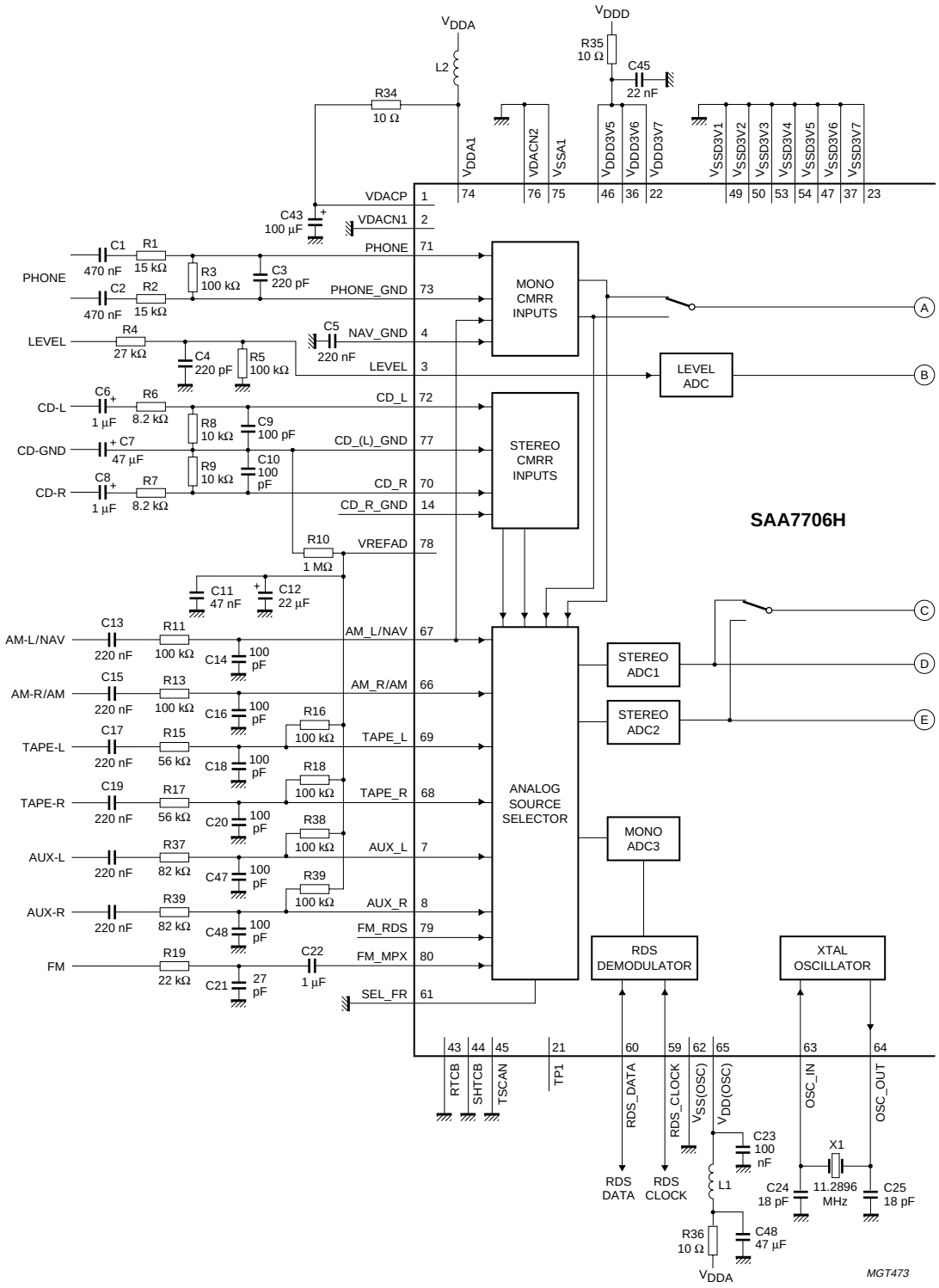
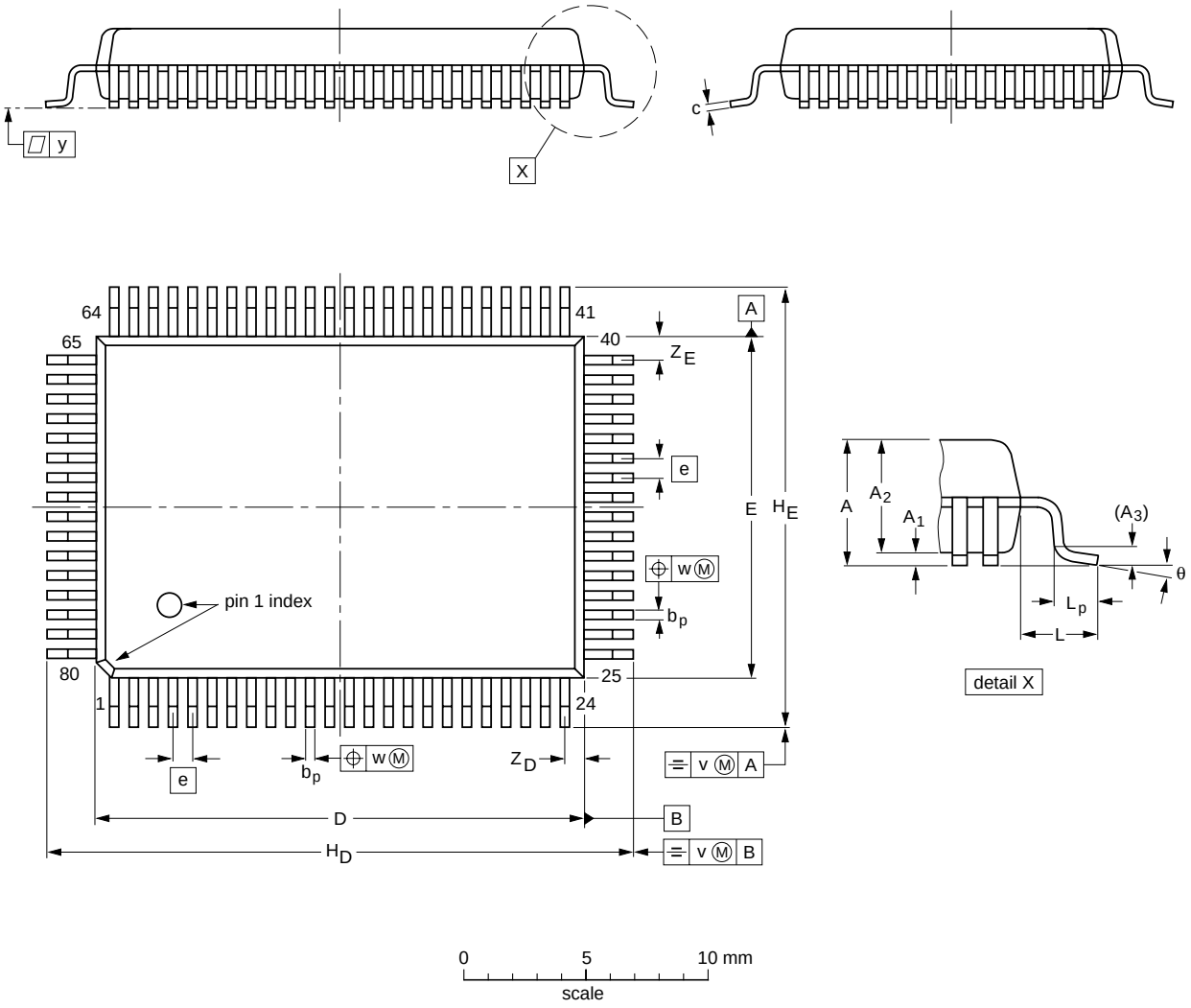


Fig.25 Application diagram (continued in Fig.26).

17 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				~~97-08-01~~ 99-12-27

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