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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n210-557

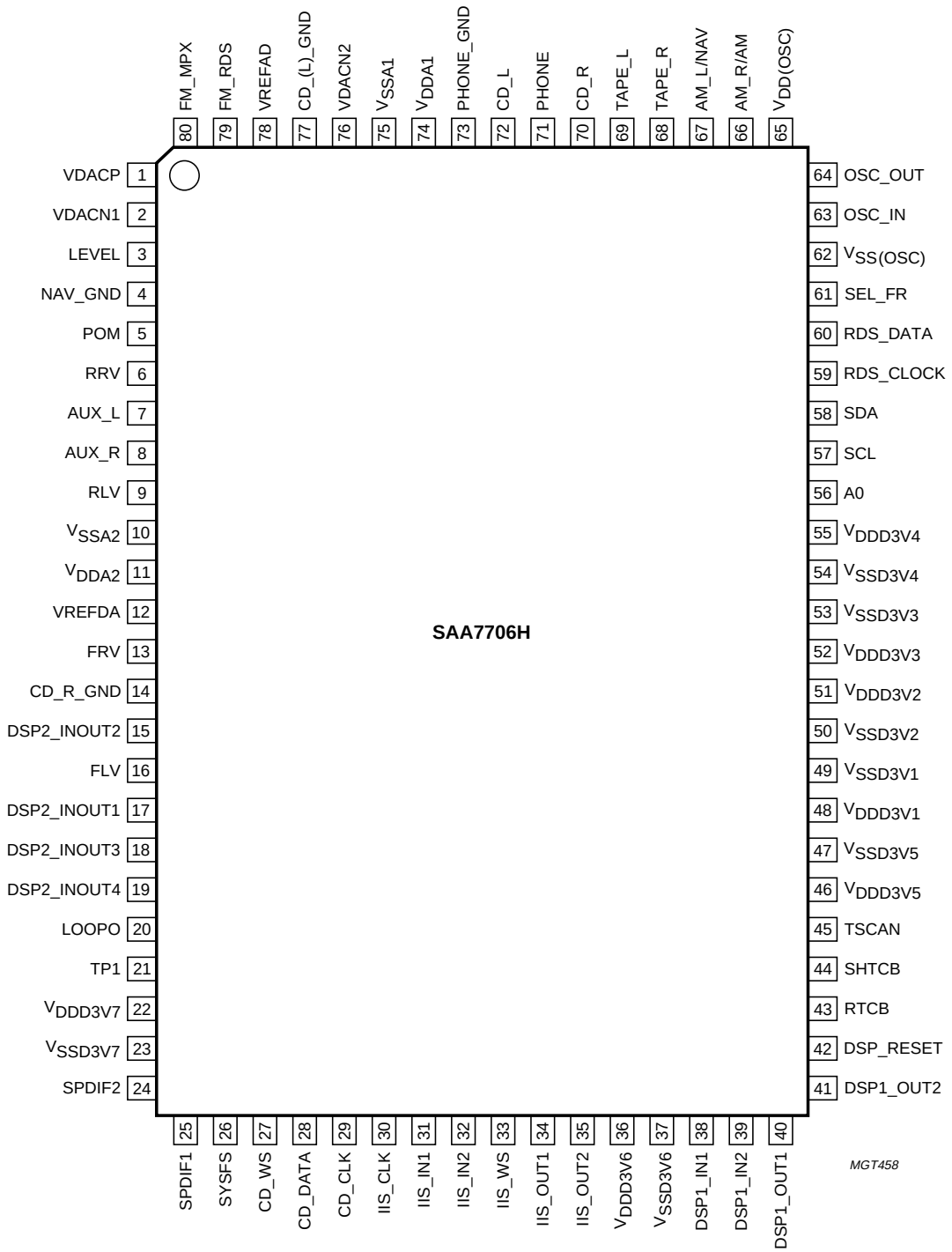


Fig.2 Pinning diagram.

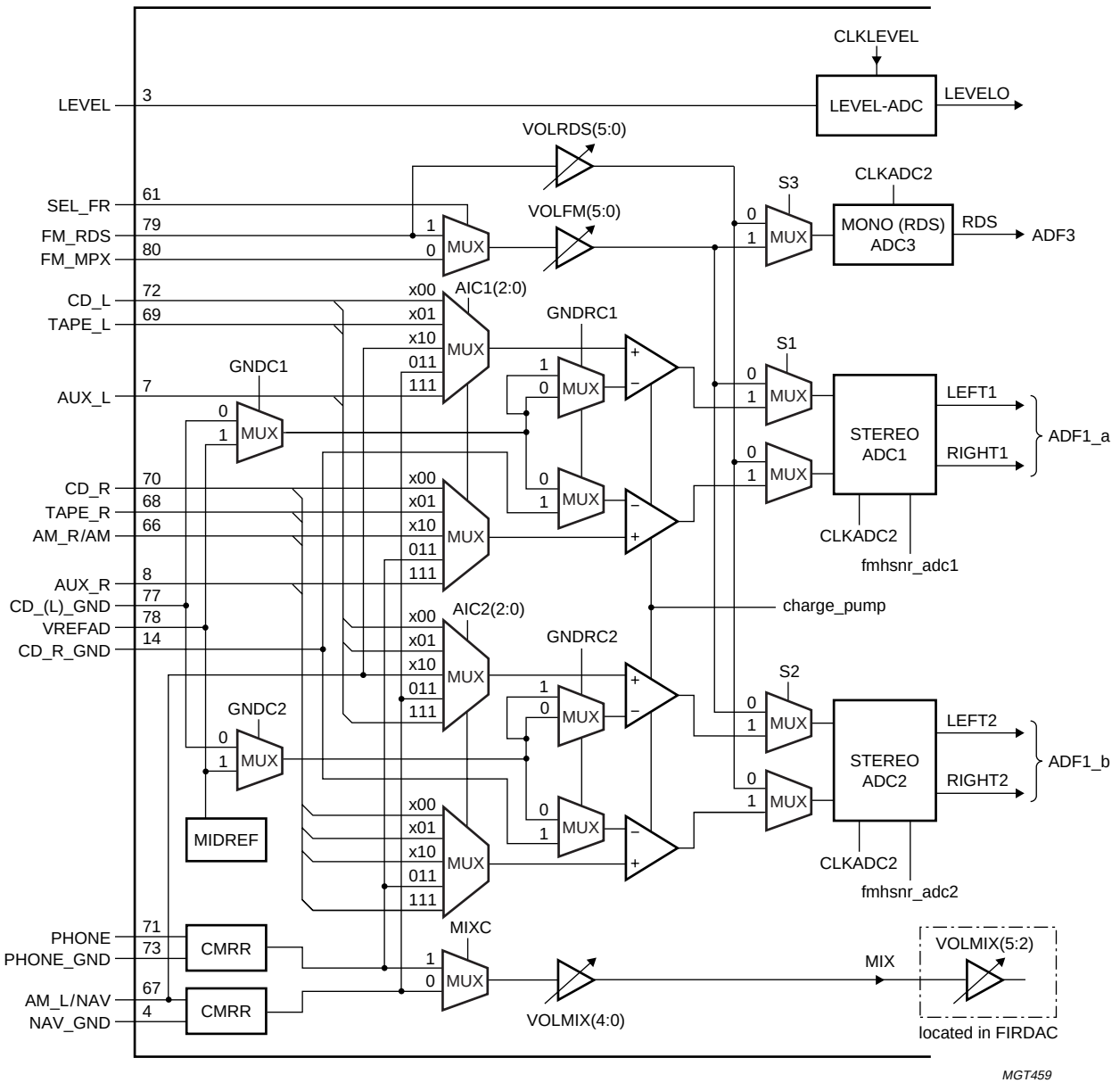


Fig.3 Analog front-end switch diagram.

8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

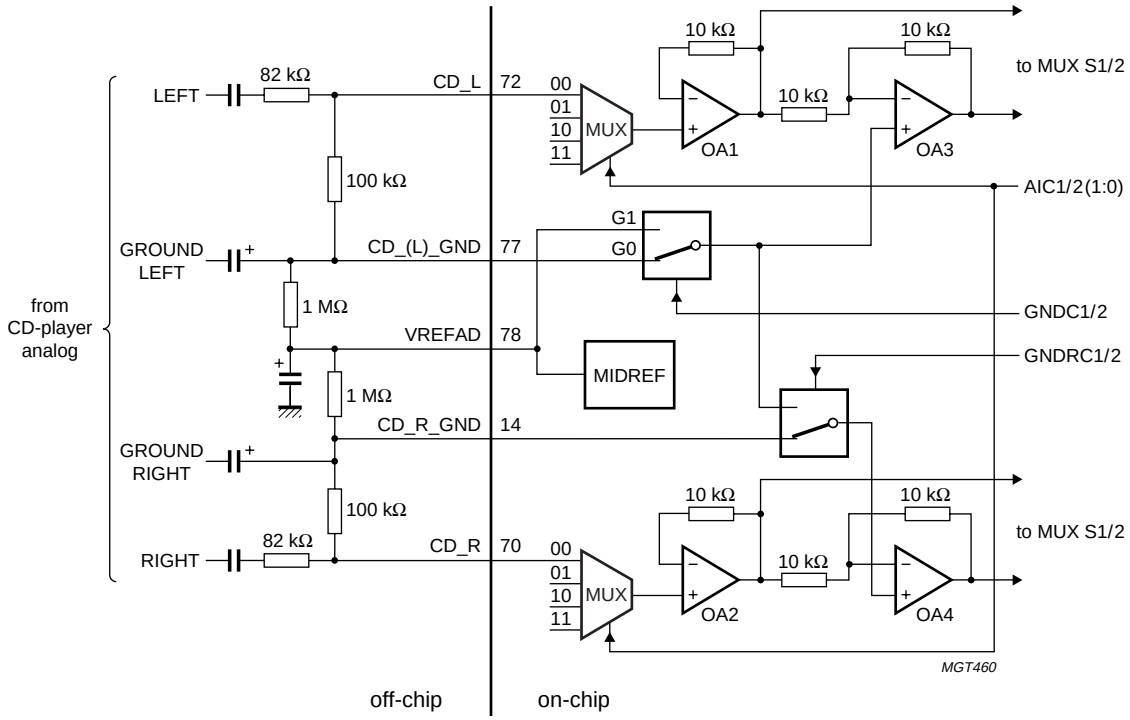


Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

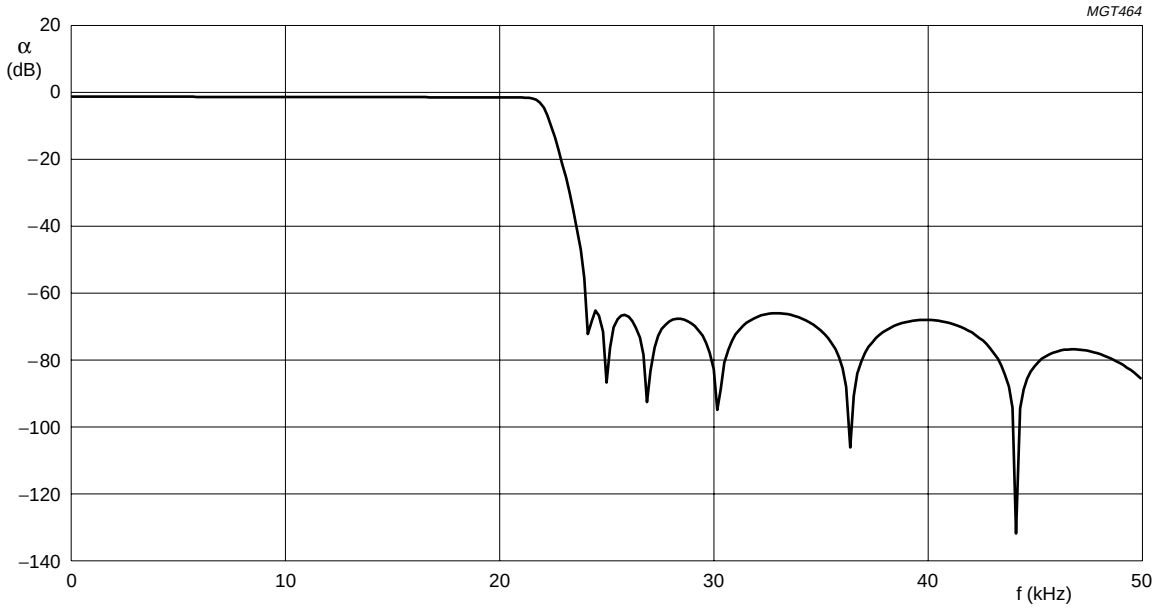


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.3 Signal path for level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a level input is implemented (pin LEVEL). In the event of radio reception the clocking of the filters and the level-ADC is based on a 38 kHz sampling frequency. A DC input signal is converted by a bitstream sigma-delta ADC followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to pin LEVEL.

The input signal for level must be in the range 0 to 3.3 V ($V_{VDACP} - V_{VDACN}$). The 9-bit level-ADC converts this input voltage in steps with a resolution better than at least 14 mV over the 3.3 V range.

The tolerance on the gain is less than 2%. The MSB is always logic 0 to represent a positive level. Input level span can be increased by an external resistor tap. The high input impedance of the level-ADC makes this possible.

The decimation filter reduces in the event of an 38 kHz based clocking regime the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz with a resulting f_s = 76 kHz. The response curve is given in Fig.9.

The level information is sub-sampled by the DSP1 to obtain a field strength and a multipath indication. These values are stored in the coefficient or data RAM. Via the I^2C-bus they can be read and used in other microcontroller programs.

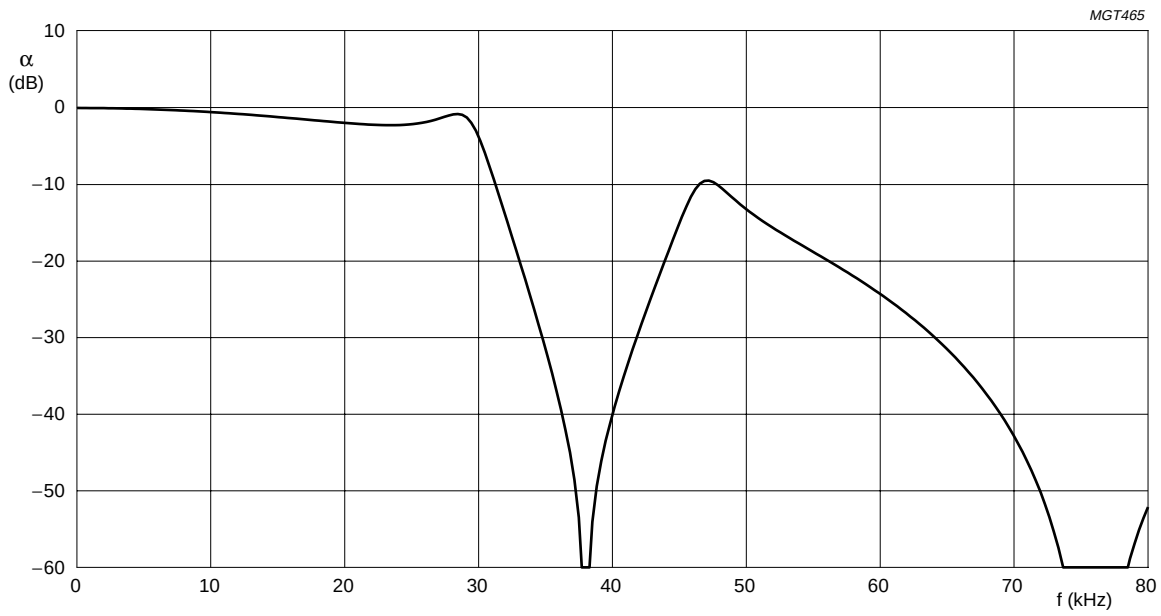


Fig.9 Frequency response level-ADC and decimal filter.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I^2S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I^2S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I^2C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I^2C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

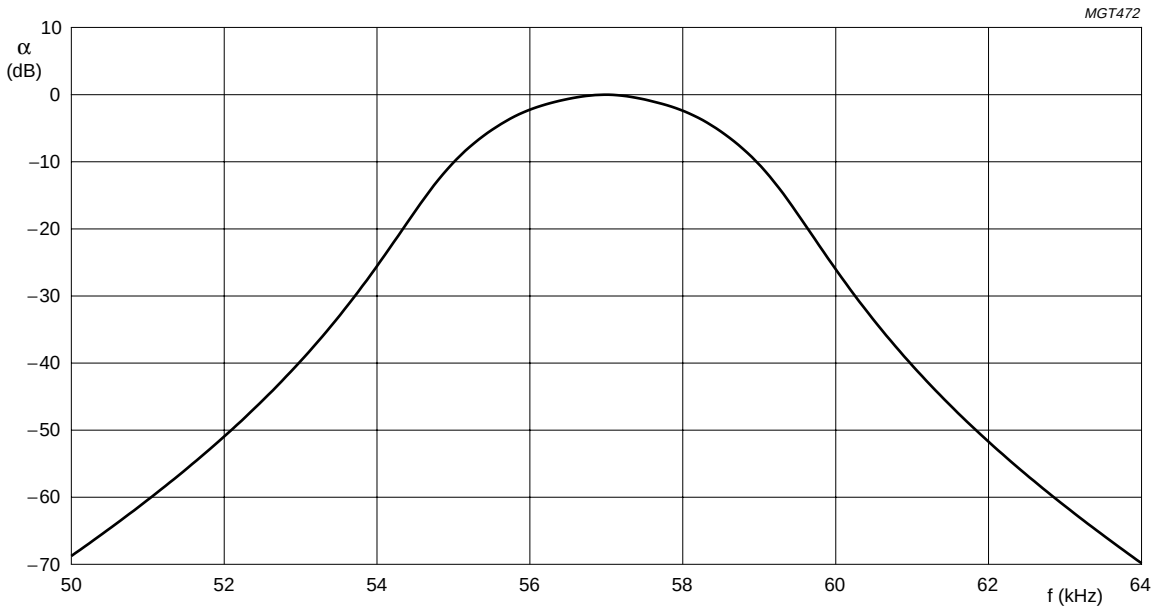
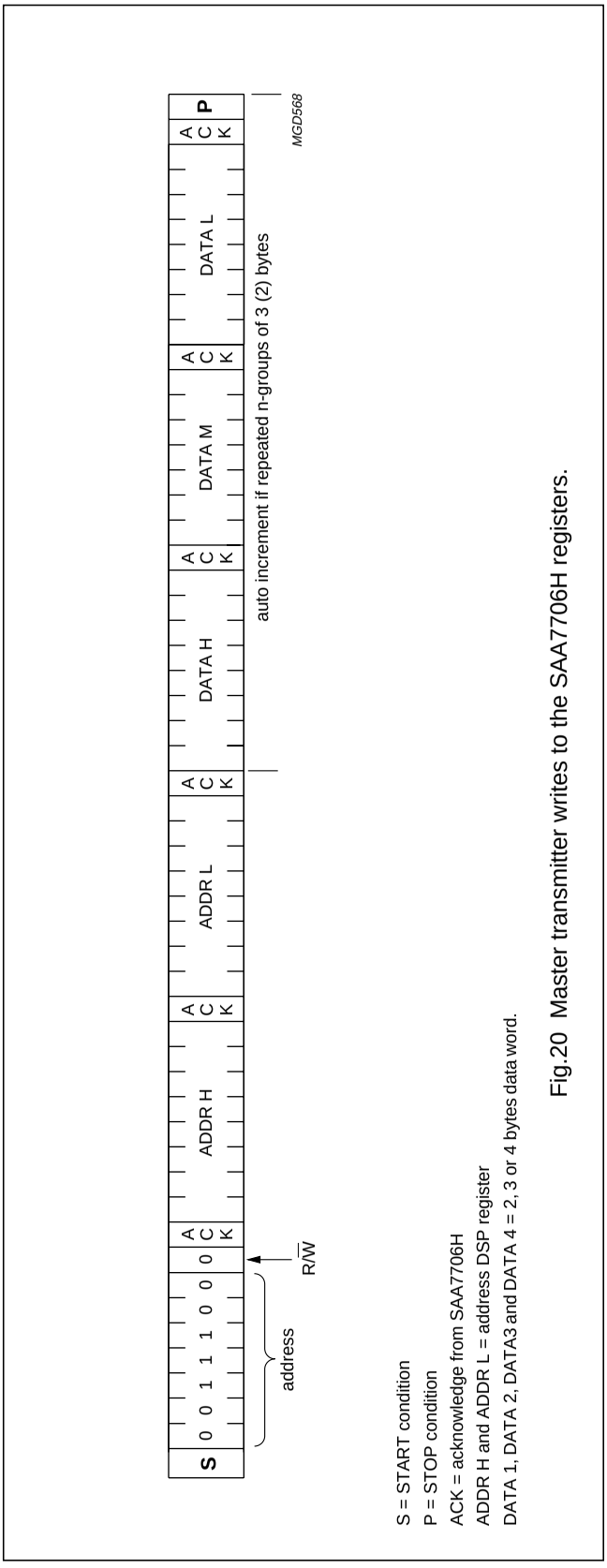


Fig.17 Detailed frequency response curve RDS channel.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDS_CLOCK and RDS_DATA. In the event of FM-stereo reception the clock of the total chip is locked to the stereo pilot (19 kHz multiple). In the event of FM-mono the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases like AM reception or tape, the DCS circuit has to be set in a preset position by means of an I^2C-bus bit. Under these conditions the RDS system is always clocked by the DCS clock in a 38 kHz (4×9.5 kHz) based sequence.

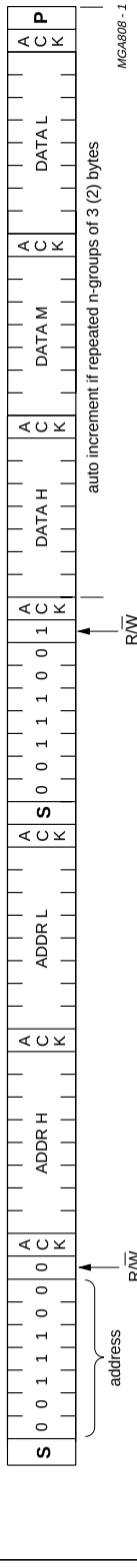
8.15.2 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 μs after the clock transition. The timing of the data change is 100 μs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller. The RDS timing is shown in Fig.18. During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.



S = START condition
P = STOP condition
ACK = acknowledge from SAA7706H
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.20 Master transmitter writes to the SAA7706H registers.



S = START condition
Sr = repeated START condition
P = STOP condition
ACK = acknowledge from SAA7706H (SDA LOW)
R = repeat n-times the 2, 3 or 4 bytes data group
NA = negative acknowledge master (SDA HIGH)
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA 3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.21 Master transmitter reads from the SAA7706H registers.

10 LIMITING VALUES

In accordance with the Absolute Maximum Ratings System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+3.6	V
V_n	input voltage on any pin		–0.5	+5.5	V
I_{IK}	DC input clamping diode current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamping diode current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
$I_{O(sink/source)}$	DC output source or sink current	$–0.5 \text{ V} < V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD},I_{SS}	supply current per supply pin		–	±50	mA
T_{amb}	ambient operating temperature		–40	+85	°C
T_{stg}	storage temperature range		–65	+125	°C
V_{ESD}	ESD voltage				
	human body model	100 pF; 1500 Ω	2000	–	V
	machine model	200 pF; 0.5 μH; 10 Ω	200	–	V
$I_{lu(prot)}$	latch-up protection current	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	890	mW

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	45	K/W

12 CHARACTERISTICS

V_{DD} = 3 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; T_{amb} = –40 to +85 °C						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3.0	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
$I_{DDD(core)}$	supply current of the digital core part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	105	140	mA
$I_{DDD(peri)}$	supply current of the digital periphery part	without external load to ground	–	5	10	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
$I_{DDA(ADC)}$	supply current of the ADCs	zero input and output signal	–	15	26	mA
$I_{DDA(DAC)}$	supply current of the DACs	zero input and output signal	–	19	30	mA
$I_{DDA(osc)}$	supply current XTAL oscillator	functional mode	–	2	4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{tot}	total power dissipation	DSP1 at 50 MHz, DSP2 at 62.9 MHz	–	540	750	mW
Digital I/O; T_{amb} = −40 to +85 °C; V_{DD} = 3 to 3.6 V						
V_{IH}	HIGH-level input voltage for all digital inputs and I/Os		2.0	–	–	V
V_{IL}	LOW-level input voltage for all digital inputs and I/Os		–	–	0.8	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	–	V
V_{OH}	HIGH-level output voltage	standard output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		5 ns slew rate output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		10 ns slew rate output; I_O = –2 mA	V_{DD} – 0.4	–	–	V
		20 ns slew rate output; I_O = –1 mA	V_{DD} – 0.4	–	–	V
V_{OL}	LOW-level output voltage	standard output; I_O = 4 mA	–	–	0.4	V
		5 ns slew rate output; I_O = 4mA	–	–	0.4	V
		10 ns slew rate output; I_O = 2 mA	–	–	0.4	V
		20 ns slew rate output; I_O = 1 mA	–	–	0.4	V
		I^2C-bus output; I_O = 4 mA	–	–	0.4	V
I_{LO}	output leakage current 3-state outputs	V_O = 0 V or V_{DD}	–	–	±5	µA
R_{pd}	internal pull-down resistor to V_{SS}		24	50	140	kΩ
R_{pu}	internal pull-up resistor to V_{DD}		30	50	100	kΩ
C_i	input capacitance		–	–	3.5	pF
$t_{i(r)}$,$t_{i(f)}$	input rise and fall times	V_{DD} = 3.6 V	–	6	200	ns
$t_{o(t)}$	output transition time	standard output; C_L = 30 pF	–	3.5	–	ns
		5 ns slew rate output; C_L = 30 pF	–	5	–	ns
		10 ns slew rate output; C_L = 30 pF	–	10	–	ns
		20 ns slew rate output; C_L = 30 pF	–	20	–	ns
		I^2C-bus output; C_b = 400 pF	60	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio					
	CD, TAPE, AM and AUX input signals	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS); f_s = 44.1 kHz	85	90	–	dB
	FM_MPX input signal mono	input signal at 1 kHz; bandwidth = 19 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	80	83	–	dB
	FM_MPX input signal stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
α_{19}	carrier and harmonic suppression at the output	pilot signal frequency = 19 kHz	–	81	–	dB
		unmodulated	–	98	–	dB
α_{38}	carrier and harmonic suppression at the output	subcarrier frequency = 38 kHz	–	83	–	dB
		unmodulated	–	91	–	dB
α_{57}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 57 kHz	–	83	–	dB
		unmodulated	–	96	–	dB
α_{76}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 76 kHz	–	84	–	dB
		unmodulated	–	94	–	dB
$IM_{\alpha 10}$	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz	77	–	–	dB
$IM_{\alpha 13}$	intermodulation	f_{mod} = 13 kHz; f_{spur} = 1 kHz	76	–	–	dB
$\alpha_{57(VF)}$	traffic radio suppression	f = 57 kHz	–	110	–	dB
$\alpha_{67(SCA)}$	Subsidiary Communication Authority (SCA) suppression	f = 67 kHz	–	110	–	dB
α_{114}	adjacent channel suppression	f = 114 kHz	–	110	–	dB
α_{190}	adjacent channel suppression	f = 190 kHz	–	110	–	dB
$V_{th(pilot)(rms)}$	pilot threshold voltage (RMS value) at pin DSP1_OUT1	stereo on; VOLFM = 07H	–	35.5	–	mV
		stereo off; VOLFM = 07H	–	35.4	–	mV
hys	hysteresis of $V_{th(pilot)(rms)}$		–	0	–	dB
α_{cs1}	channel separation FM-stereo input	f_i = 1 kHz	40	45	–	dB
		f_i = 10 kHz	25	30	–	dB
α_{cs2}	channel separation CD, TAPE, AM and AUX input signals		60	70	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	load capacitance		–	–	200	pF
AC CHARACTERISTICS						
$V_{o(RMS)}$	output voltage (RMS value)		–	1000	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio (measured with system one)	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio (measured with system one)	code = 0; A-weighted	–	105	–	dB
α_{cs}	channel separation		–	80	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 1%	–	50	–	dB
Oscillator; T_{amb} = 25 °C; $V_{DD(OSC)}$ = 3.3 V						
f_{xtal}	crystal frequency		–	11.2896	–	MHz
V_{xtal}	voltage across the crystal	crystal series resistance R_s < 100 Ω; crystal shunt capacitance C_p < 7 pF; crystal load capacitance C_L = 12 pF; $C_1 = C_2$ = 22 pF (see Fig.13)	1.6	2.6	3.6	V
$I_{DD(OSC)}$	supply current crystal oscillator	at start-up	1.7	3.4	6.4	mA
		at oscillation	–	0.32	–	mA

13 RDS AND I²S-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RDS timing (see Figs 18 and 19)						
f_{RDSCLK}	nominal RDS clock frequency		–	1187.5	–	Hz
t_{su}	clock set-up time	direct output mode	100	–	–	µs
T_{cy}	cycle time	direct output mode	–	842	–	µs
		buffer mode	2	–	–	µs
t_{HC}	clock HIGH time	direct output mode	220	–	640	µs
		buffer mode	1	–	–	µs
t_{LC}	clock LOW time	direct output mode	220	–	640	µs
		buffer mode	1	–	–	µs
t_h	data hold time		100	–	–	µs
t_w	wait time	buffer mode	1	–	–	µs

14 I²C-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time		0	–	0	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	rise time of both SDA and SCL signals	C_b in pF	–	1000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	C_b in pF	–	300	$20 + 0.1C_b$	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs
C_b	capacitive load for each bus line		–	400	–	400	pF
t_{SP}	pulse width of spikes to be suppressed by input filter		–	–	0	50	ns

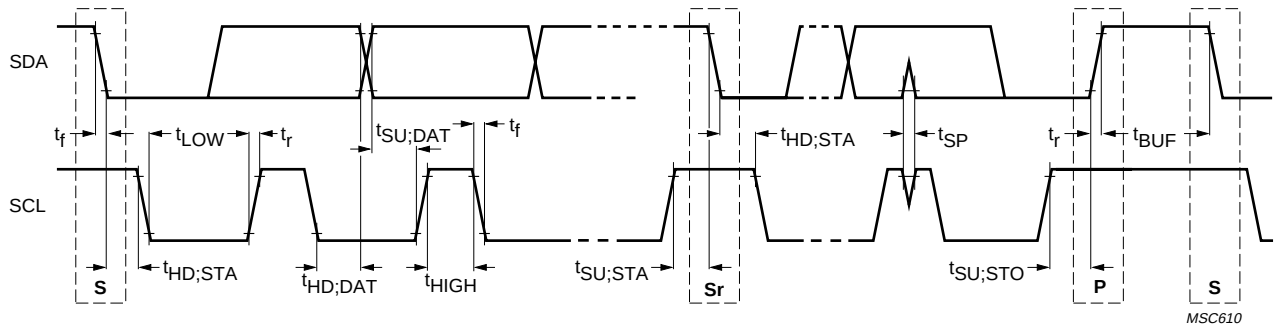


Fig.24 Definition of timing on the I^2C-bus.

15 SOFTWARE DESCRIPTION

The use and description of the software features of the SAA7706H will be described in the separate application manual.

16 APPLICATION DIAGRAM

The application diagram shown in Figs 25 and 26 must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I^2S-bus inputs of the CD-input are not used. For the real application set-up the information of the application report is necessary.

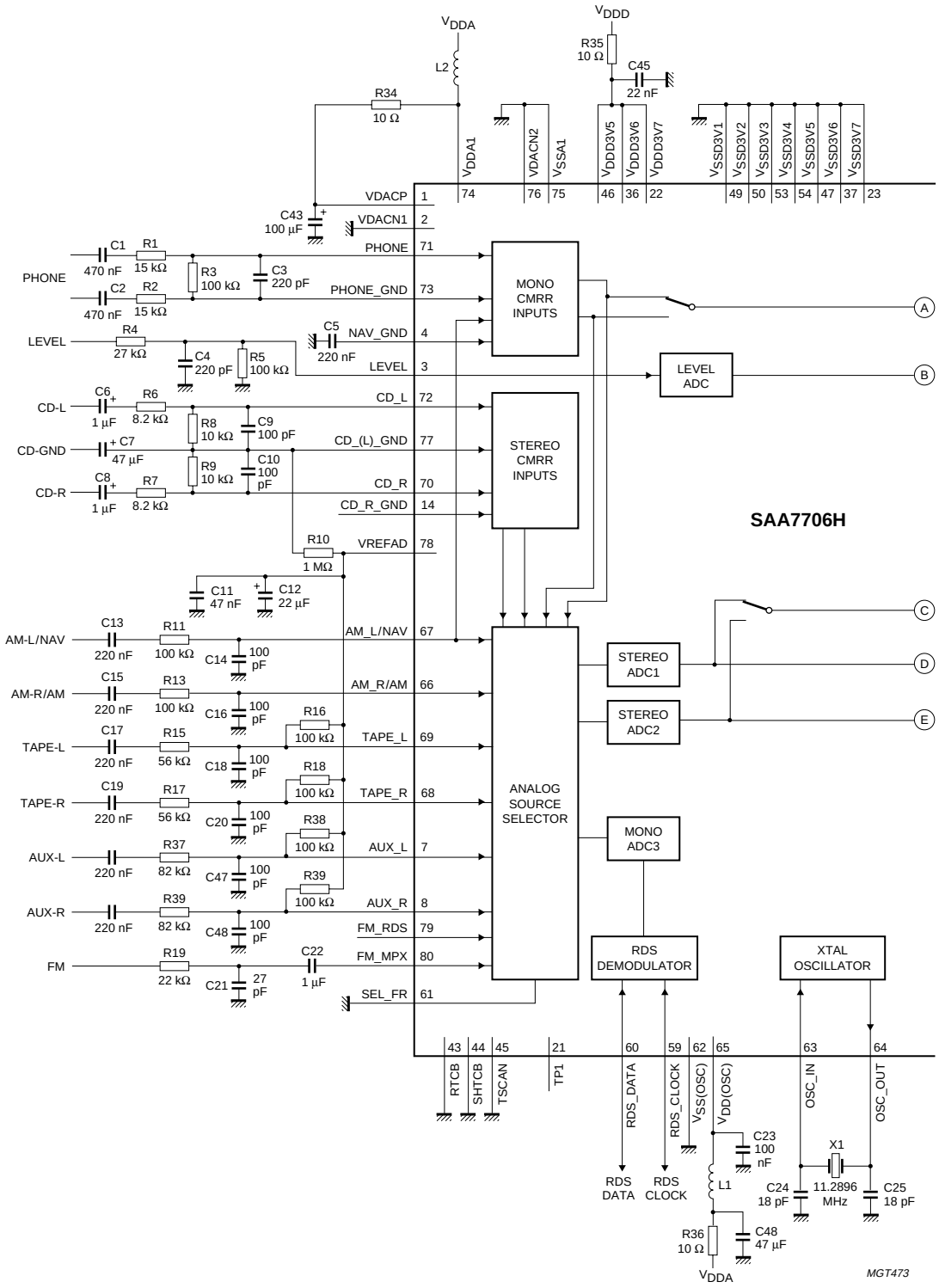


Fig.25 Application diagram (continued in Fig.26).

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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