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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Car Signal Processor
Interface	I²C, I²S, LSB, SPDIF
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n210s-518

CONTENTS

1 FEATURES

1.1 Hardware

- 5-bitstream 3rd-order sigma-delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filter
- 1-bitstream 1st-order sigma-delta ADC with anti-aliasing broadband input filter
- 4-bitstream Digital-to-Analog Converters (DACs) with 128-fold oversampling and noise shaping
- Integrated semi-digital filter; no external post filter required for DAC
- Dual media support: allowing separate front-seat and rear-seat signal sources and separate control
- Simultaneous radio and audio processing
- Digital FM stereo decoder
- Digital FM interference suppression
- RDS demodulation via separate ADC; with buffered output option
- Two mono Common-Mode Rejection Ratio (CMRR) input stages for voice signals from phone and navigation inputs
- Phone and navigation mixing at DAC front outputs
- Two stereo CMRR input stages (CD-walkman and CD-changer etc.)
- Analog single-ended TAPE and AUX input
- Separate AM-left and AM-right inputs in the event of use of external AM stereo decoder
- One digital input: I^{2}S-bus or LSB-justified format
- Two digital inputs: SPDIF format
- Co-DSP support via I^{2}S-bus or LSB-justified format
- Audio output short-circuit protected
- I^{2}C-bus controlled (including fast mode)
- MOST bus interfacing (details in separate manual)
- Phase-locked loop derives the internal clocks from one common fundamental crystal oscillator
- Combined AM/FM level input
- Pin compatible with SAA7705 and SAA7708
- All digital inputs are tolerant of 5 V input levels
- All analog inputs have high GSM immunity
- Low number of external components required
- –40 to +85 °C operating temperature range
- Easy applicable.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter; de-emphasis and stereo detection
- Electronic adjustments: FM or AM level, FM channel separation, Dolby®(1) level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Four channel 5-band parametric equalizer
- 9-bands mono audio spectrum analyzer
- Extended beep functions with tone sequencer for phone rings
- Large volume jumps e-power interpolated to prevent zipper noise
- Dual media support; allowing separate front-seat and rear-seat signal sources and separate control
- Dynamic loudness or bass boost
- Audio level monitor
- Tape equalization and Music Search System (MSS) detection for tape
- Dolby-B tape noise reduction (at 44.1 kHz only)
- Dynamics compression available in all modes
- CD de-emphasis processing
- Voice-over possibility for phone and navigation signals
- Improved AM signal processing
- Digital AM CQUAM stereo decoder (not in all rom_codes available)
- Digital AM interference suppression
- Soft audio mute
- RDS update processing: pause detection, mute and signal-quality sensor-freeze
- General purpose tone generator

(1) **Dolby** — Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

6 BLOCK DIAGRAM

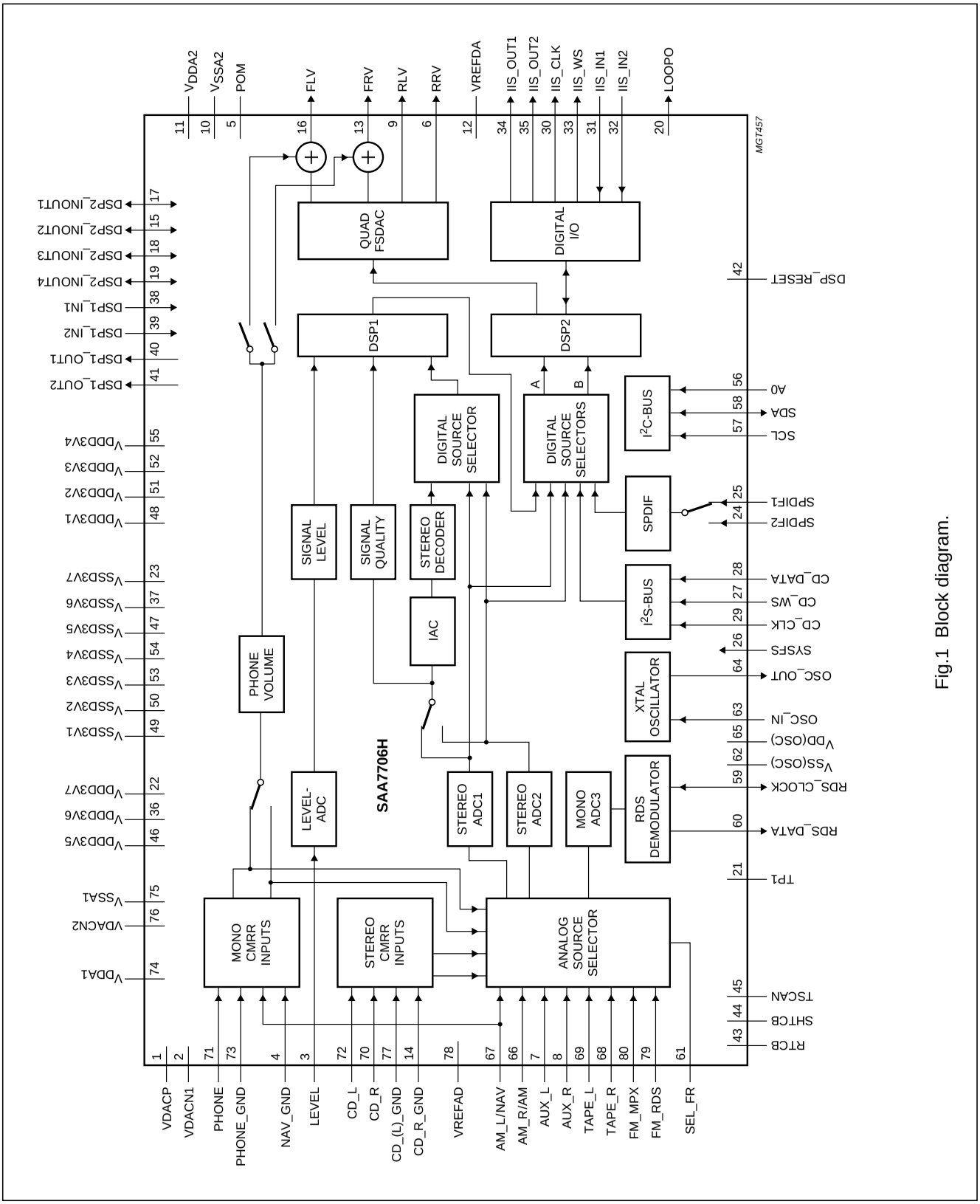


Fig.1 Block diagram.

8 FUNCTIONAL DESCRIPTION

8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via I^2C-bus.

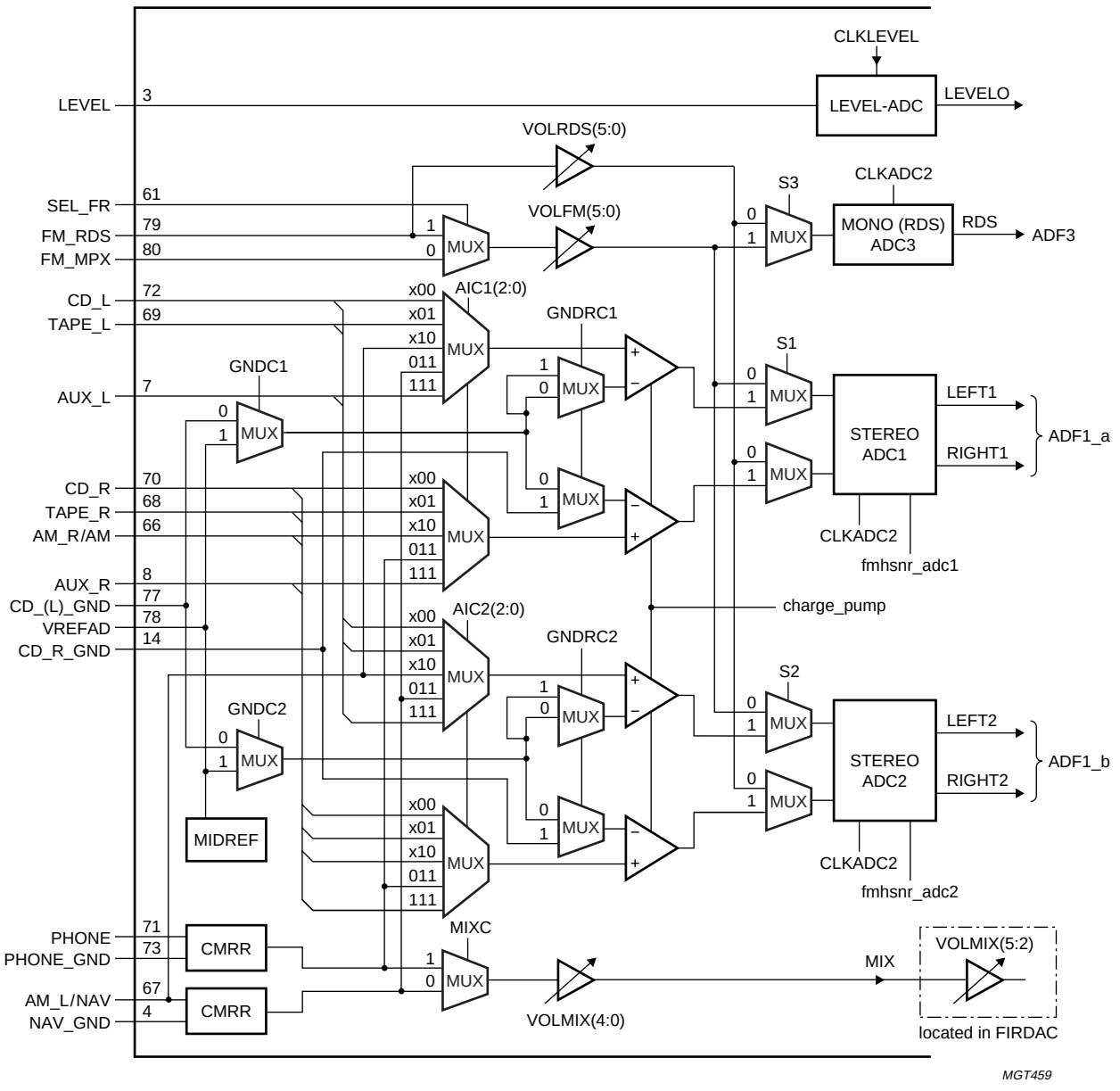


Fig.3 Analog front-end switch diagram.

8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

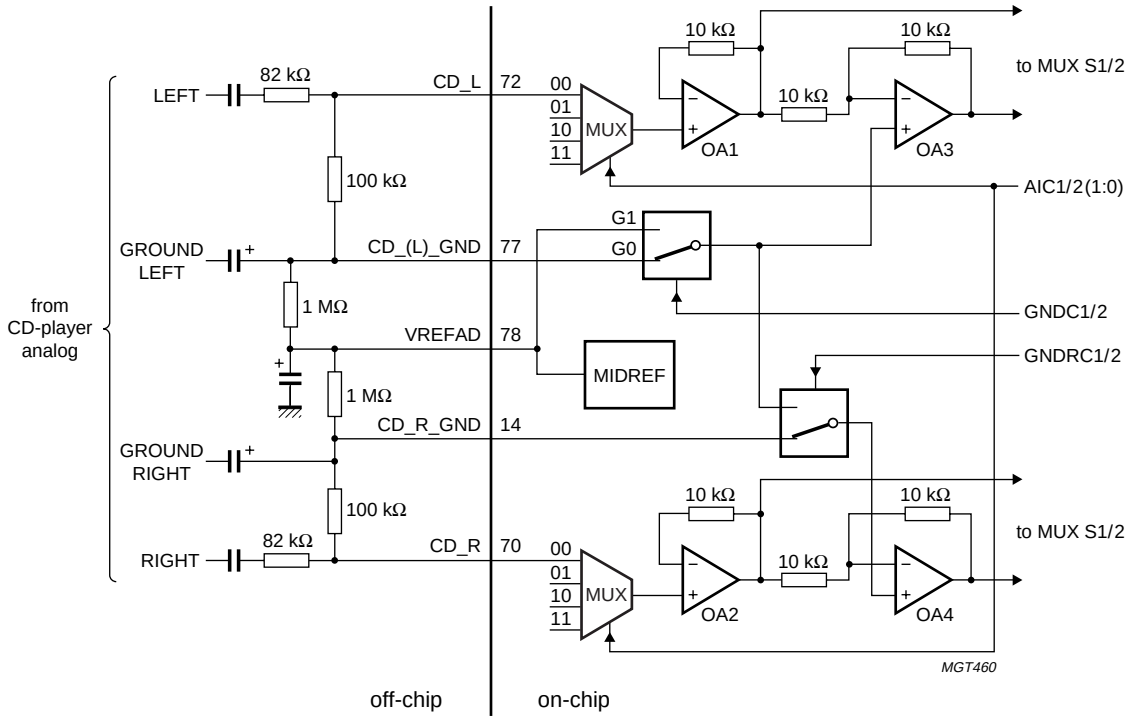


Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

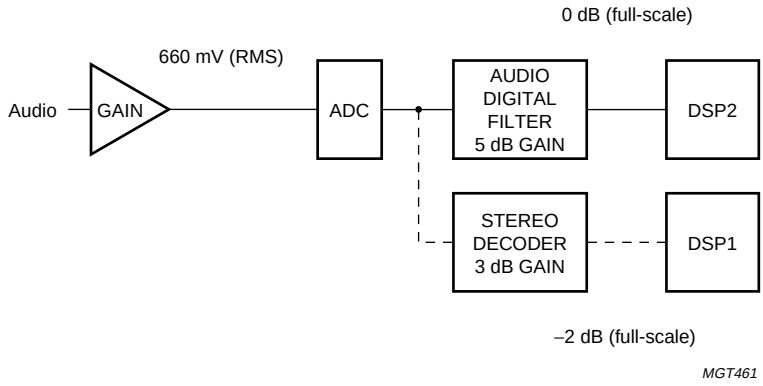


Fig.5 Audio gain through ADC and digital filter path to DSP.

8.1.2 Realization of the auxiliary input with volume control

A differential input with volume control for mixing to the front left or front right of both DAC outputs is provided. The inputs consist of a PHONE and NAV input. Both are accompanied with their ground return lines. After selection of PHONE or NAV the volume can be changed from about +18 to −22.5 dB in 27 steps and mute (MIX output). This signal can be added to the left and/or right front DAC channels.

The output signals of both input circuits can also be switched to ADC1 and/or ADC2, depending on the settings of audio input control 1 (AIC1) and audio input control 2 (AIC2), without volume control (see Fig.3).

8.1.3 Realization of the FM input control

The gain of the circuit has a maximum of 2.26 (7.08 dB). This results in an input level of 368 mV for full-scale, which means 0 dB (full-scale) at the DSP1 input via the stereo decoder (see Fig.6). The gain can be reduced in steps of 1.5 dB. When the gain is set to −3.4 dB the input level becomes 1229 mV for full-scale. This setting accounts for the 200 mV (RMS) input sensitivity at 22.5 kHz sweep and a saturation of the input at 138 kHz sweep.

RDS update: for RDS update the fast access pin SEL_FR must be made HIGH. In that case the FM_RDS signal also goes through the path that was set for FM_MPX. In this situation the signal must be obtained via the FM_RDS input and a noise sample can be retrieved. The input FM_MPX gets high-ohmic. Charging of the coupling capacitor connected to pin FM_MPX is no longer possible.

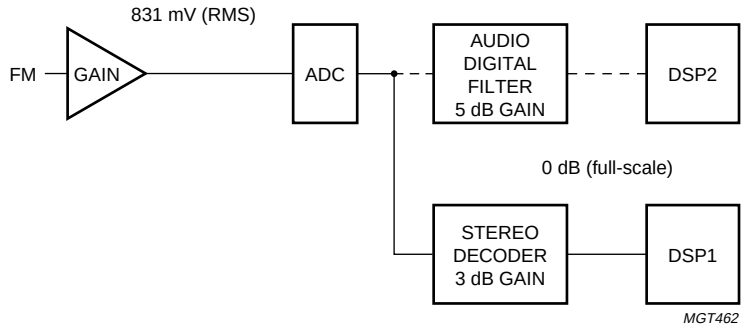


Fig.6 FM gain path through stereo decoder to DSP1.

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

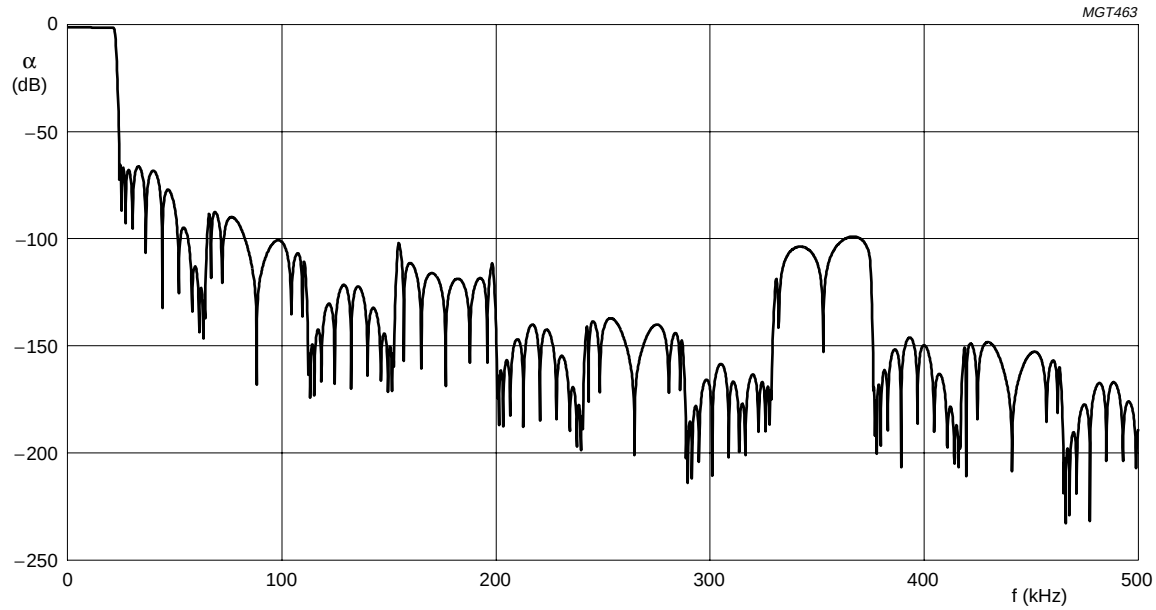


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

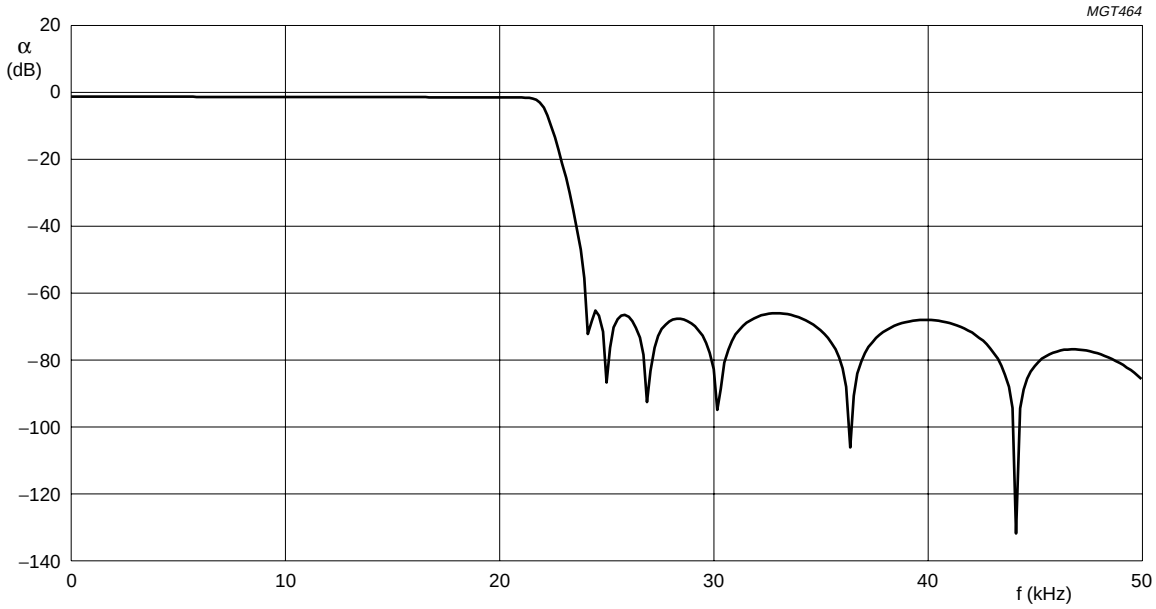


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.4 Signal path from FM_MPX input to IAC and stereo decoder

The FM_MPX signal is after selection available at one of three ADCs (ADC1, 2 and 3). The multiplex FM signal is converted to the digital domain in ADC1, 2 and 3 through a bitstream ADC. Improved performance for FM stereo can be achieved by means of adapting the noise shaper curve of the ADC to a higher bandwidth.

The first decimation takes place in two down-sample filters. These decimation filters are switched by means of the I^2C-bus bit wide_narrow in the wide or narrow band position. In the event of FM reception it must be in the narrow position.

After selection of one of the ADCs, the FM_MPX path it is followed by the IAC and the FM stereo decoder. One of the two MPX filter outputs contains the multiplex signal with a frequency range of 0 to 60 kHz. The overall low-pass frequency response of the decimation filters is shown in Fig.10.

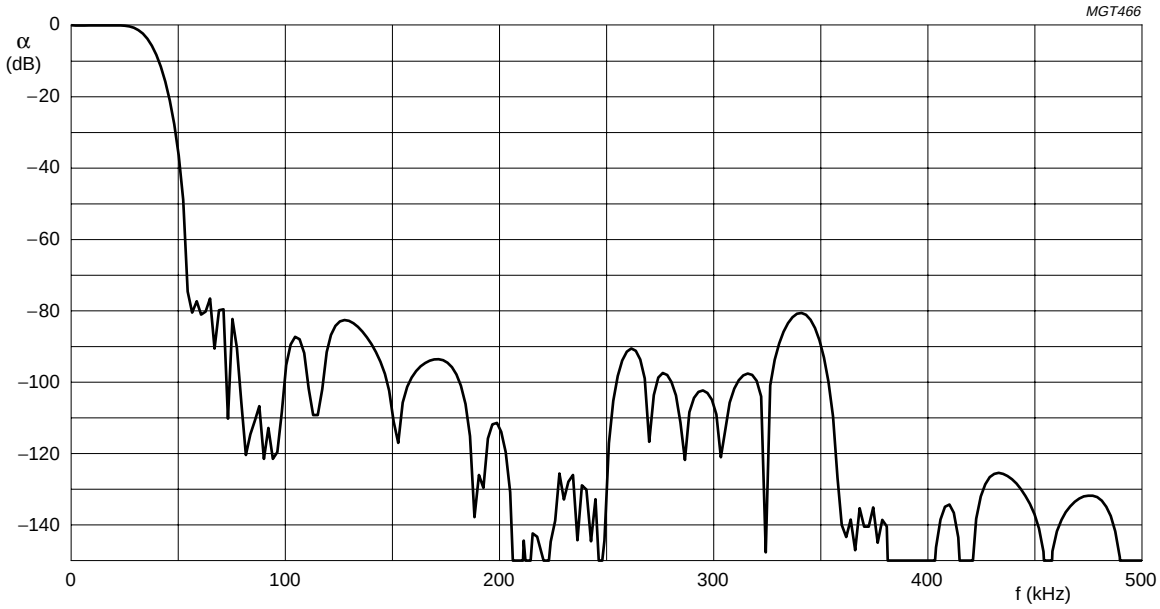


Fig.10 Overall frequency response of ADC1, ADC2 and decimation filters.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I^2C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I^2C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I^2C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

8.7.3 Function of pin POM

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has past a particular level. This results in an almost dB-linear behaviour. This must prevent 'plop' effects during power on or off.

8.7.4 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate power supply of 3.3 V. A capacitor connected to this power supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

8.7.5 Pin VREFDA for internal reference

With two internal resistors half the supply voltage V_{DDA2} is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC.

In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin V_{SSA2}.

8.7.6 Supply of the filter stream DAC

The entire analog circuitry of the DACs and the operational amplifiers are supplied by 2 supply pins: V_{DDA2} and V_{SSA2}. V_{DDA2} must have sufficient decoupling to prevent total harmonic distortion degradation and to ensure a good power supply rejection ratio. The digital part of the DAC is fully supplied from the chip core supply.

8.8 Clock circuit and oscillator

The chip has an on-chip crystal clock oscillator. The block diagram of this Pierce oscillator is shown in Fig.13. The active element needed to compensate for the loss resistance of the crystal is the block G_m. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to the clock signal.

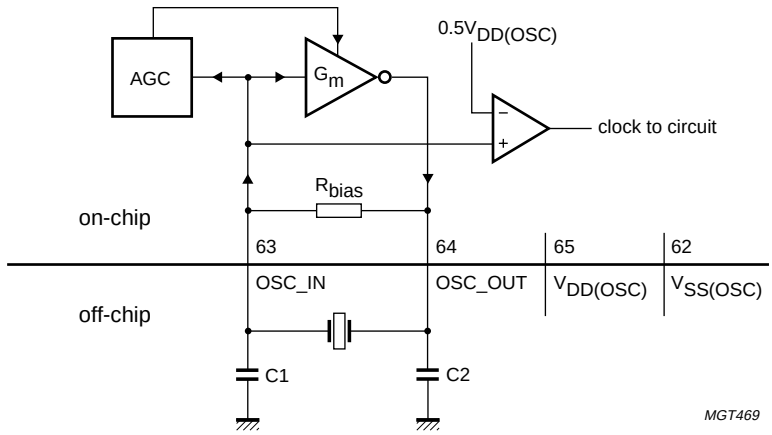


Fig.13 Block diagram oscillator circuit.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I^2S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I^2S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I^2C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I^2C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

9 I²C-BUS FORMAT

For more general information on the I²C-bus protocol, see the Philips I²C-bus specification.

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

9.2 Slave address (pin A0)

The SAA7706H acts as slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The SAA7706H slave address is shown in Table 3.

Table 3 Slave address

MSB							LSB
0	0	1	1	1	0	A0	R/$\overline{W}$

The sub-address bit A0 corresponds to the hardware address pin A0 which allows the device to have 2 different addresses. The A0 input is also used in test mode as a serial input of the test control block.

9.3 Write cycles

The I²C-bus configuration for a write cycle is shown in Fig.20. The write cycle is used to write the bytes to both DSP1 and DSP2 for manipulating the data and coefficients. Depending on which DSP is accessed the data protocol exists out of 2, 3 or 4 bytes. More details can be found in the I²C-bus memory map (see Table 5).

The data length is 2, 3 or 4 bytes depending on the accessed memory. If the Y-memory of DSP1 is addressed the data length is 2 bytes, in the event of the X-memory of DSP1 or X/Y-memory of DSP2 the length is 3 bytes. The slave receiver detects the address and adjusts the number of bytes accordingly. The data length of 4 bytes is not used in the SAA7706H.

9.4 Read cycles

The I²C-bus configuration for a READ cycle is shown in Fig.21. The read cycle is used to read the data values from XRAM or YRAM of both DSPs. The master starts with a START condition S, the SAA7706H address ‘0011100’ and a logic 0 (write) for the R/$\overline{W}$ bit. This is followed by an acknowledge of the SAA7706H.

Then the master writes the high memory address and low memory address where the reading of the memory content of the SAA7706H must start. The SAA7706H acknowledges these addresses both. Then the master generates a repeated START (Sr) and again the SAA7706H address ‘0011100’ but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit.

From this moment on the SAA7706H will send the memory content in groups of 2 (Y-memory DSP1) or 3 (X-memory DSP1, X/Y-memory DSP2 or registers) bytes to the I²C-bus each time acknowledged by the master. The master stops this cycle by generating a negative acknowledge, then the SAA7706H frees the I²C-bus and the master can generate a STOP condition. The data is transferred from the DSP register to the I²C-bus register at execution of the MPI instruction in the DSP2 program. Therefore at least once every DSP routine an MPI instruction should be added. The data length of 4 bytes is not used in the SAA7706H.

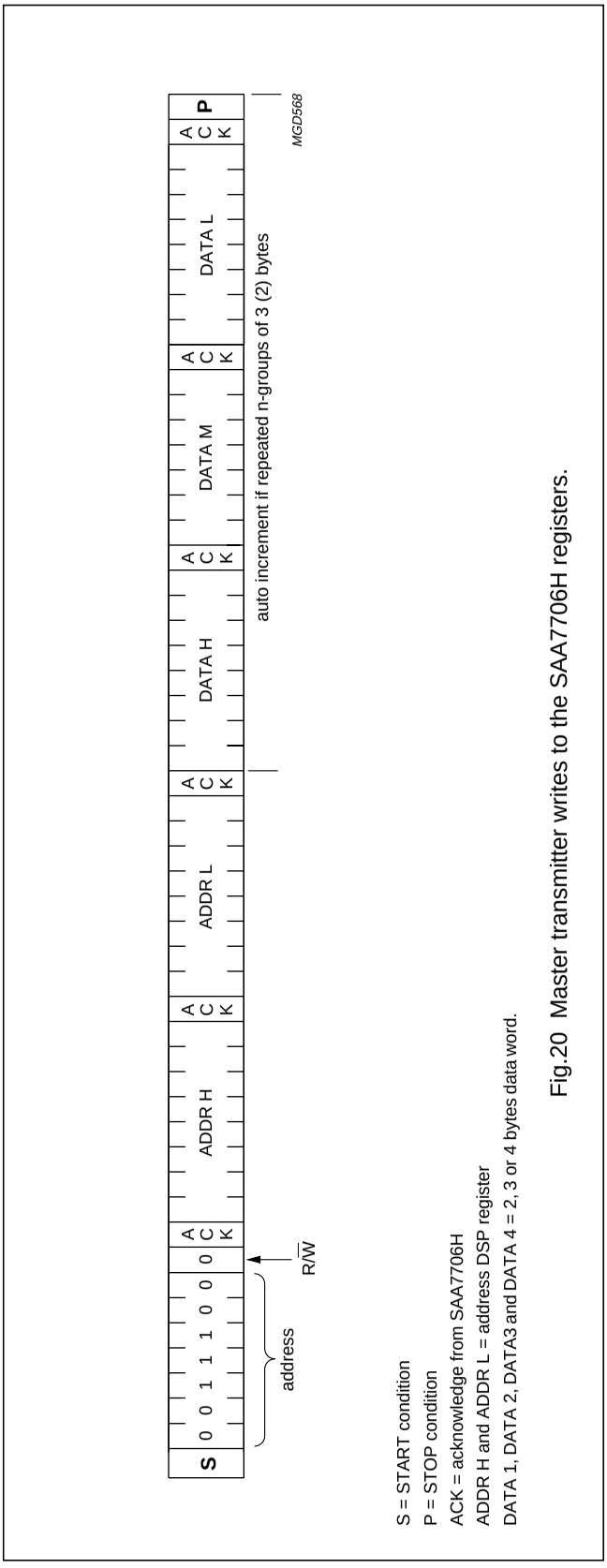
9.5 SAA7706H hardware registers

The write cycle can be used to write the bytes to the hardware registers to control the DCS block, the PLL for the DSP clock generation, the IAC settings, the AD volume control settings, the analog input selection, the format of the I²S-bus and some other settings. It is also possible to read these locations for chip status information. More detail can be found in the I²C-bus memory map, Tables 4 and 5.

9.5.1 SAA7706H DSPs REGISTERS

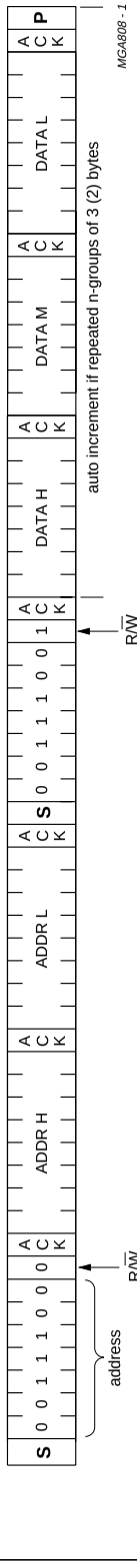
The hardware registers have two different address blocks. One block exists out of hardware register locations which control both DSPs and some major settings such as the PLL division. These locations have a maximum of 16 bits, which means 2 bytes need to be sent to or read from. For the SAA7706H one register is located at the DSPs and general control register (0FFFH).

The second block has an address space of 16 addresses and are all X-memory mapped on DSP2. While this space is 24 bits wide 3 bytes should be sent to or read from. These addresses are DSP2 mapped which means an MPI instruction is needed for accessing those locations and there is no verifying mechanism if all addresses are really mapped to physical registers. Therefore, all those locations will be acknowledged even if the data is not valid. For the SAA7706H several registers are located in this section. A few registers are predefined for DSP2 purposes (see Table 5).



S = START condition
P = STOP condition
ACK = acknowledge from SAA7706H
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.20 Master transmitter writes to the SAA7706H registers.



S = START condition
Sr = repeated START condition
P = STOP condition
ACK = acknowledge from SAA7706H (SDA LOW)
R = repeat n-times the 2, 3 or 4 bytes data group
NA = negative acknowledge master (SDA HIGH)
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA 3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.21 Master transmitter reads from the SAA7706H registers.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

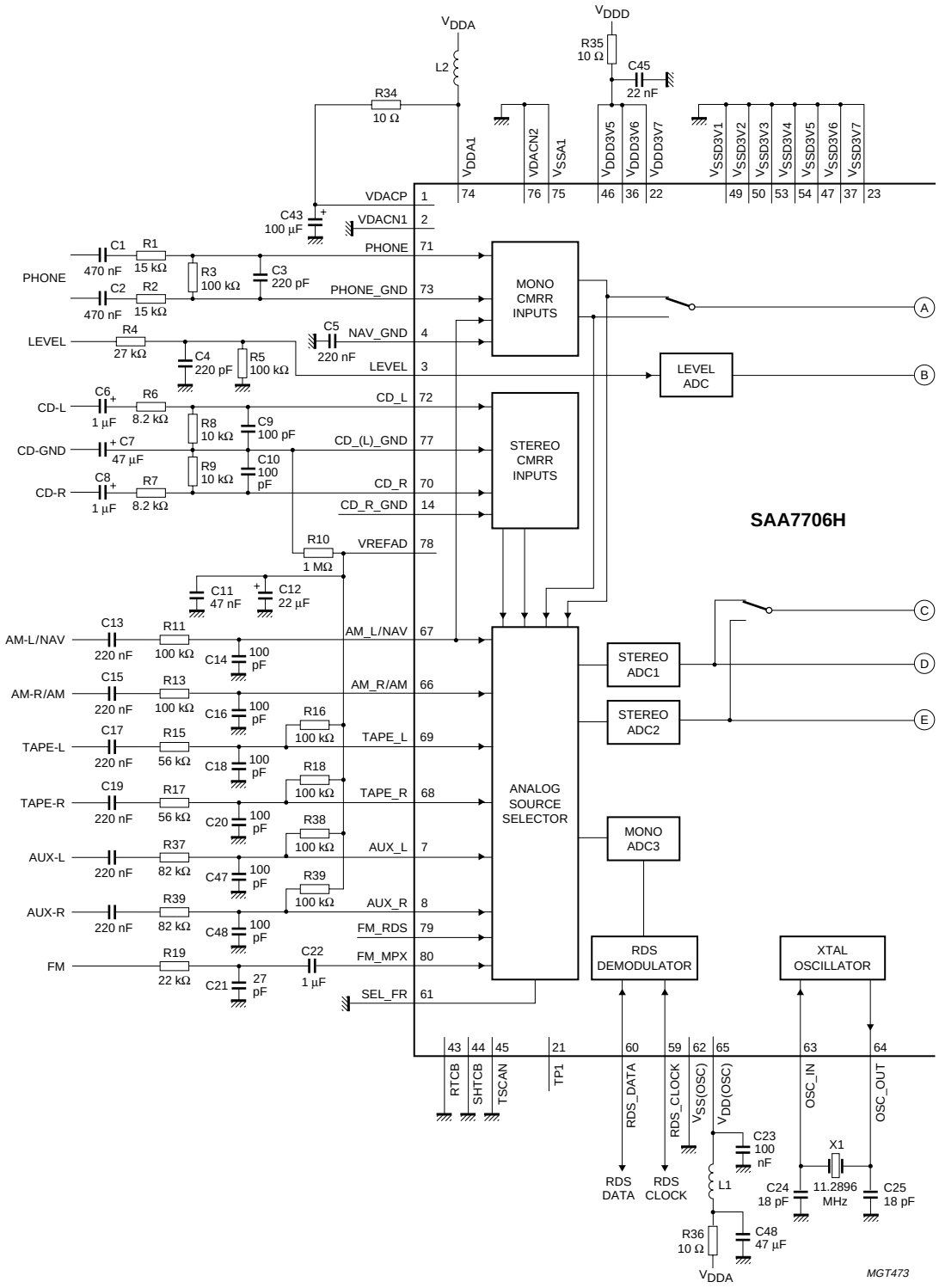


Fig.25 Application diagram (continued in Fig.26).

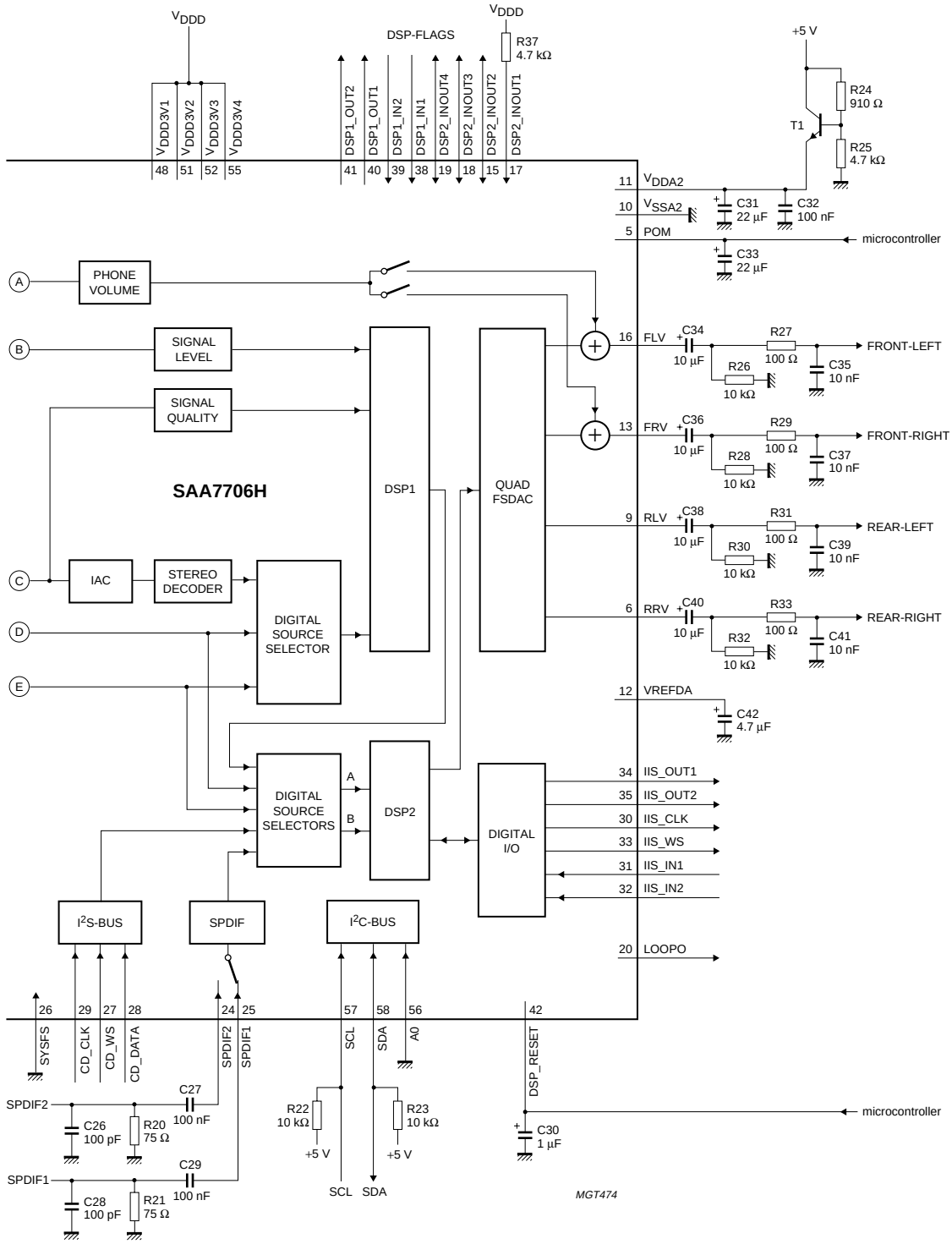


Fig.26 Application diagram (continued from Fig.25).

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.