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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Car Signal Processor |
| Interface | I²C, I²S, LSB, SPDIF |
| Clock Rate | - |
| Non-Volatile Memory | - |
| On-Chip RAM | - |
| Voltage - I/O | 3.30V |
| Voltage - Core | 3.30V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-BQFP |
| Supplier Device Package | 80-PQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/saa7706h-n210s-557 |

**CONTENTS**

## 6 BLOCK DIAGRAM

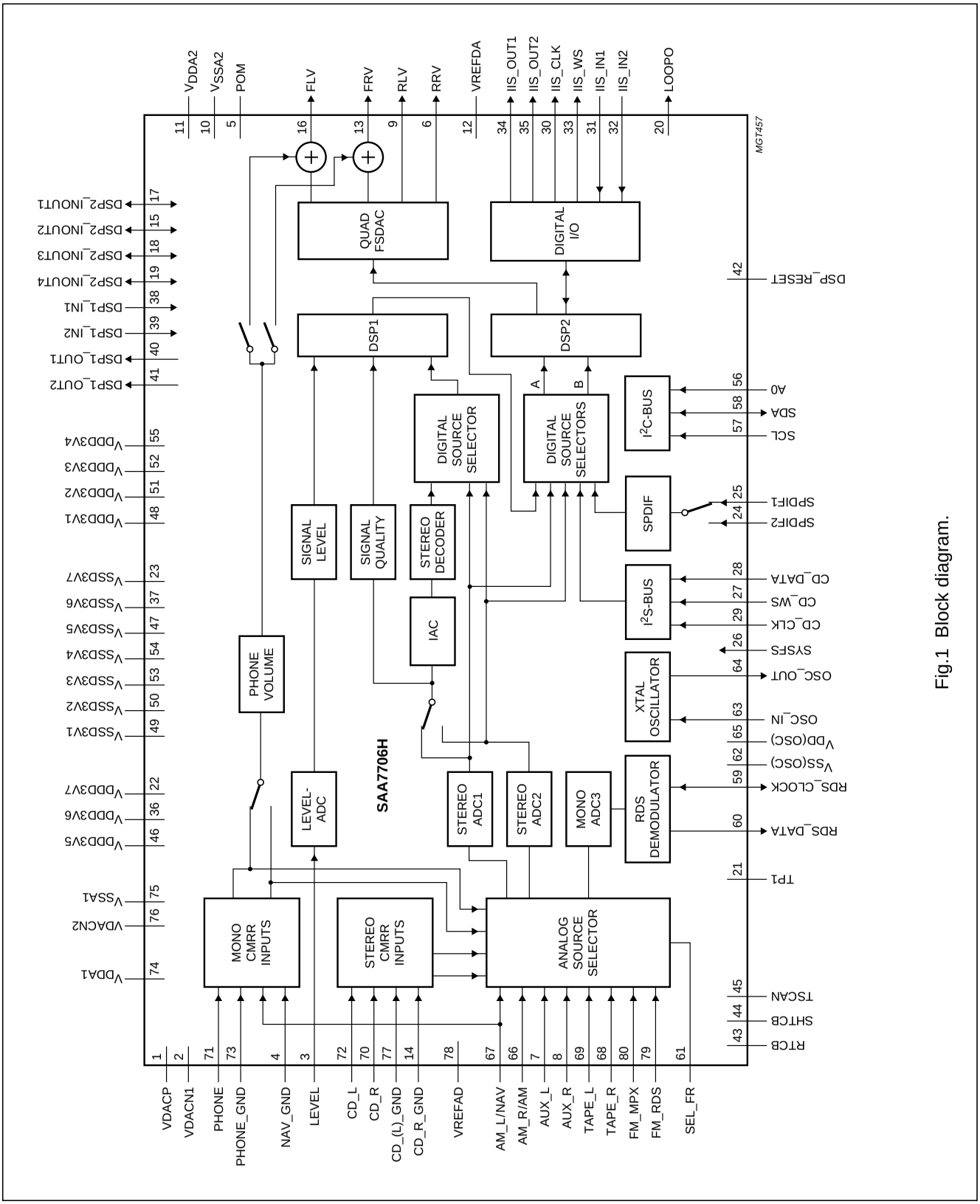



Fig.1 Block diagram.

## 7 PINNING

| SYMBOL | PIN | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| VDACP | 1 | apio | positive reference voltage ADC1, ADC2, ADC3 and level-ADC |
| VDACN1 | 2 | apio | ground reference voltage ADC1 |
| LEVEL | 3 | apio gsmcap | LEVEL input pin; via this pin the level of the FM signal or level of the AM signal is fed to the DSP1; the level information is used in the DSP1 for dynamic signal processing |
| NAV_GND | 4 | apio gsmcap | common mode reference input pin of the navigation signal (pin AM_L/NAV) |
| POM | 5 | apio | power-on mute of the QFSDAC; timing is determined by an external capacitor |
| RRV | 6 | apio | rear; right audio output of the QFSDAC |
| AUX_L | 7 | apio | left channel of analog AUX input |
| AUX_R | 8 | apio | right channel of analog AUX input |
| RLV | 9 | apio | rear; left audio output of the QFSDAC |
| $V_{SSA2}$ | 10 | vssco | ground supply analog part of the QFSDAC and SPDIF bitslicer |
| $V_{DDA2}$ | 11 | vddco | positive supply analog part of the QFSDAC and SPDIF bitslicer |
| VREFDA | 12 | apio | voltage reference of the analog part of QFSDAC |
| FRV | 13 | apio | front; right audio output of the QFSDAC |
| CD_R_GND | 14 | apio | common-mode reference input pin for analog CD_R or TAPE_R in the event of separated ground reference pins for left and right are used |
| DSP2_INOUT2 | 15 | bpts5thdt5v | flag input/output 2 of the DSP2-core (DSP2-flag) $I^2C$-bus configurable |
| FLV | 16 | apio | front; left audio voltage output of the QFSDAC |
| DSP2_INOUT1 | 17 | bpts5thdt5v | flag input/output 1 of the DSP2-core (DSP2-flag) $I^2C$-bus configurable |
| DSP2_INOUT3 | 18 | bpts5thdt5v | flag input/output 3 of the DSP2-core (DSP2-flag) $I^2C$-bus configurable |
| DSP2_INOUT4 | 19 | bpts5thdt5v | flag input/output 4 of the DSP2-core (DSP2-flag) $I^2C$-bus configurable |
| LOOPO | 20 | bpts5tht5v | SYSCLK output ($256f_s$) |
| TP1 | 21 | ipthdt5v | for test purpose only; this pin may be left open or connected to ground |
| $V_{DDD3V7}$ | 22 | vdde | positive supply (peripheral cells only) |
| $V_{SSD3V7}$ | 23 | vsse | ground supply (peripheral cells only) |
| SPDIF2 | 24 | apio | SPDIF input 2; can be selected instead of SPDIF1 via $I^2C$-bus bit |
| SPDIF1 | 25 | apio | SPDIF input 1; can be selected instead of SPDIF2 via $I^2C$-bus bit |
| SYSFS | 26 | ipthdt5v | system $f_s$ clock input |
| CD_WS | 27 | ipthdt5v | digital CD-source word select input; $I^2S$-bus or LSB-justified format |
| CD_DATA | 28 | bpts10thdt5v | digital CD-source left-right data input; $I^2S$-bus or LSB-justified format |
| CD_CLK | 29 | ipthdt5v | digital CD-source clock input $I^2S$-bus or LSB-justified format |
| IIS_CLK | 30 | ots10ct5v | clock output for external $I^2S$-bus receiver; for example headphone or subwoofer |
| IIS_IN1 | 31 | ipthdt5v | data 1 input for external $I^2S$-bus transmitter; e.g. audio co-processor |
| IIS_IN2 | 32 | ipthdt5v | data 2 input for external $I^2S$-bus transmitter; e.g. audio co-processor |
| IIS_WS | 33 | ots10ct5v | word select output for external $I^2S$-bus receiver; for example headphone or subwoofer |
| IIS_OUT1 | 34 | ots10ct5v | data 1 output for external $I^2S$-bus receiver or co-processor |
| IIS_OUT2 | 35 | ots10ct5v | data 2 output for external $I^2S$-bus receiver or co-processor |

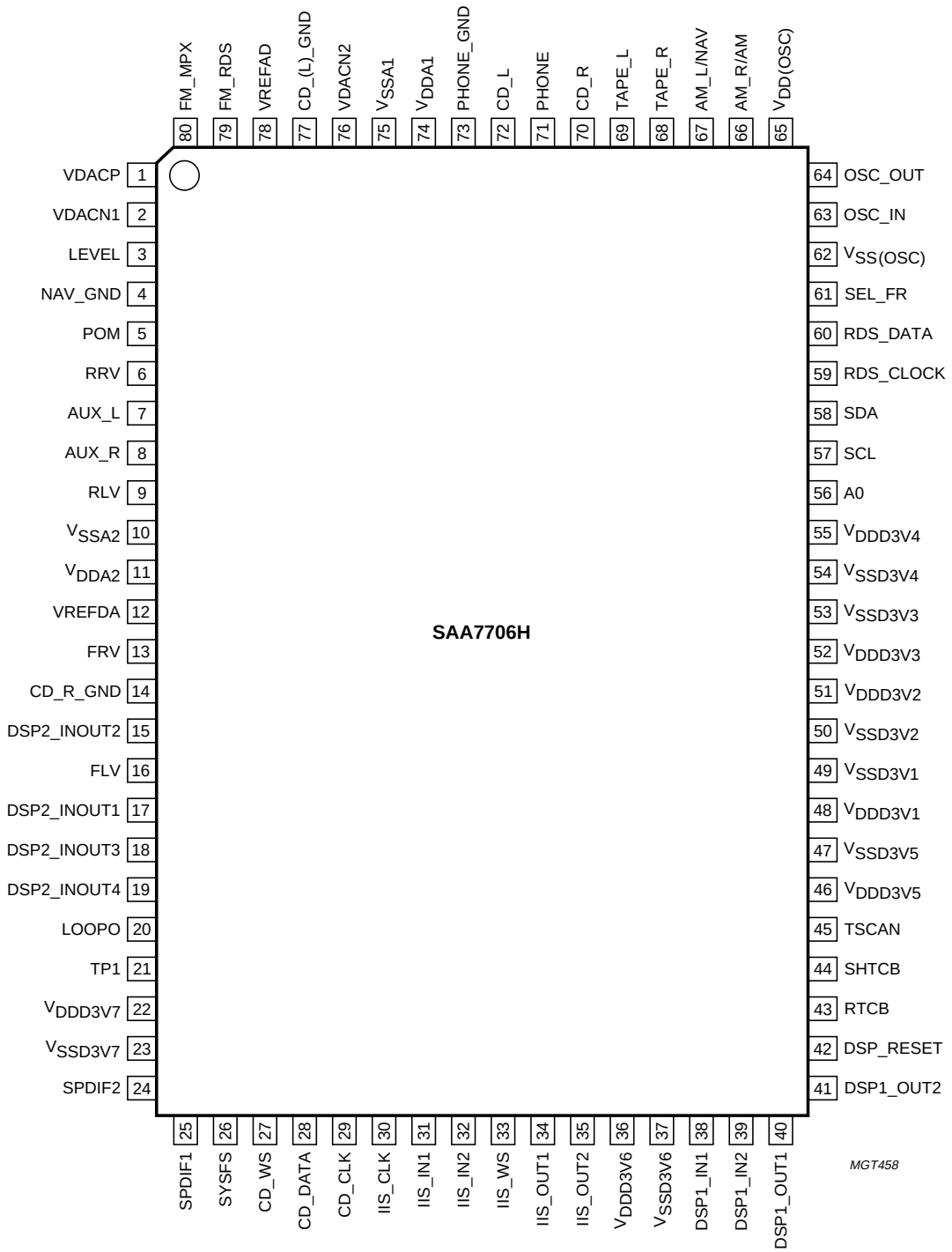



Fig.2 Pinning diagram.

## 8 FUNCTIONAL DESCRIPTION

### 8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via $I^2C$-bus.

### 8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

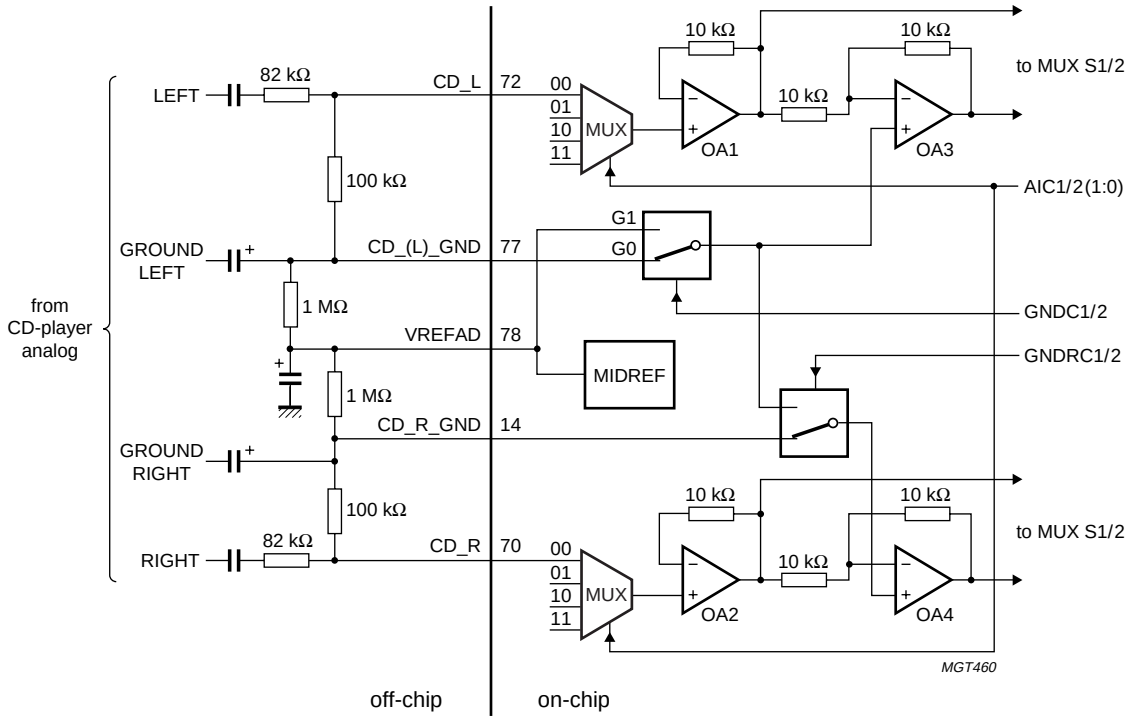



Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

#### 8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the $V_{SSA1}$ and filtered $V_{DDA1}$ for optimal performance (see Figs 25 and 26).

#### 8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to $V_{SSA1}$) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

#### 8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are $V_{SSA1}$ for the analog ground and $V_{DDA1}$ for the analog power supply.

### 8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

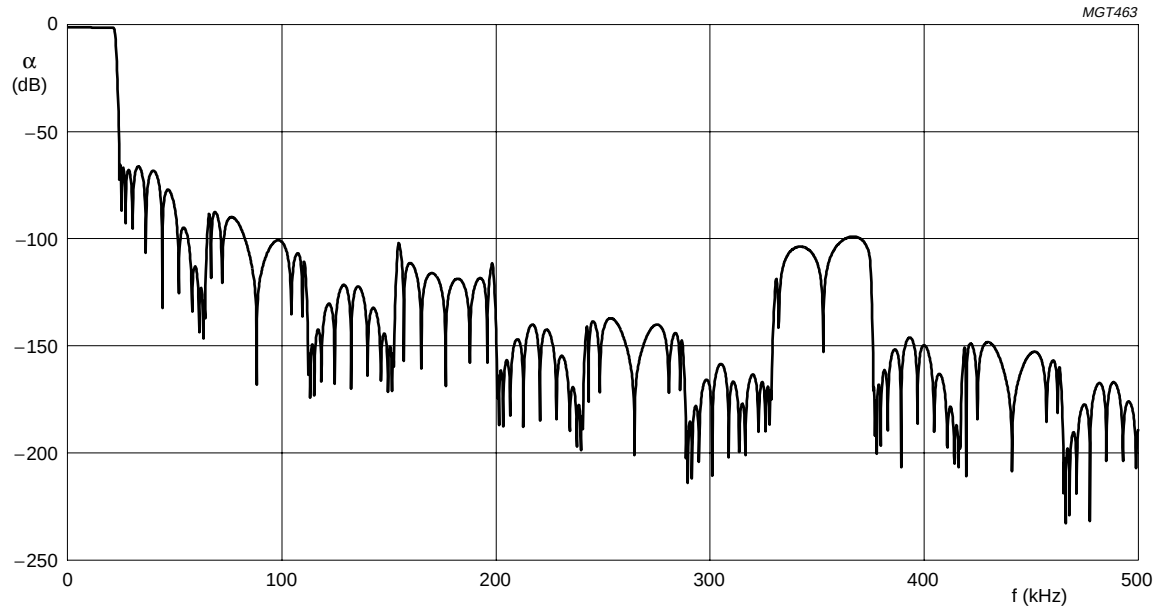



Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

The outputs of the stereo decoder to the DSP1, which are all running on a sample frequency of 38 kHz are:

- Pilot presence indication: pilot-I. This 1-bit signal is LOW for a pilot frequency deviation <4 kHz and HIGH for a pilot frequency deviation >4 kHz and locked on a pilot tone.
- 'Left' and 'right' FM reception stereo signal: this is the 18-bit output of the stereo decoder after the matrix decoding.
- Noise level (see also Section 8.4.1): which is retrieved from the high-pass output of the MPX filter. The noise level is detected and filtered in the DSP1 and is used to optimize the FM weak signal processing.

Normally the FM_MPX input and the FM_RDS input have the same source. If the FM input contains a stereo radio channel, the pilot information is switched to the Digitally Controlled Sampling (DCS) clock generation and the DCS clock is locked to the 256 $\times$ 38 kHz of the pilot. In this case this locked frequency is also used for the RDS path ensuring the best possible performance.

Except from the above mentioned theoretical response also the non-flat frequency response of the ADC has to be compensated in the DSP1 program.

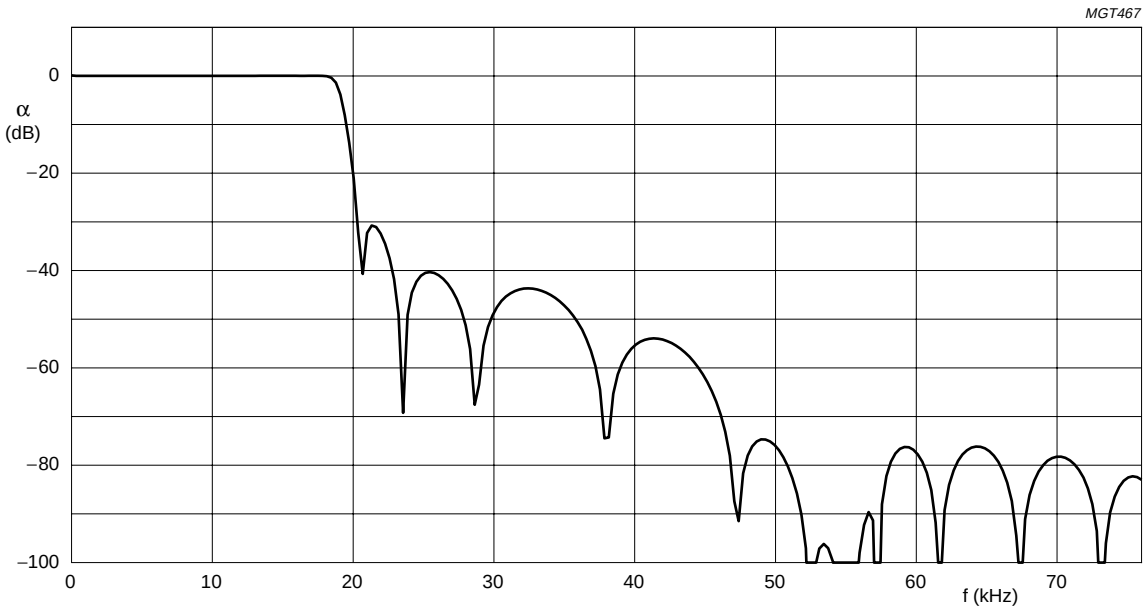



Fig.11 Transfer of MPX signal at the output of the stereo decoder.

### 8.12 External control pins

#### 8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

#### 8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

### 8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

### 8.14 Digital serial inputs/outputs and SPDIF inputs

#### 8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips $I^2S$-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

#### 8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. $I^2S$-bus) is made, consisting of a word select, data and bit clock line. The sample frequency $f_s$ depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the $I^2C$-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the $I^2C$-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

### 8.15 RDS demodulator (pins RDS_CLOCK and RDS_DATA)

The RDS demodulator recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting. The (buffered) data is provided as output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with the EBU specification *"EN 50067"*.

The RDS demodulator has three different functions:

- Clock and data recovery from the MPX signal
- Buffering of 16 bits, if selected
- Interfacing with the microcontroller.

#### 8.15.1 CLOCK AND DATA RECOVERY

The RDS-chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from an other transmitter (double tuner concept). It can as such be done without interruption of the audio program. The MPX signal from the main tuner of the car radio can be connected to this RDS input via the built-in source selector. The input selection is controlled by an $I^2C$-bus bit.

The RDS chain contains a sigma-delta ADC (ADC3), followed by two decimation filters. The first filter passes the multiplex band including the signals around 57 kHz and reduces the sigma-delta noise. The second filter reduces the RDS bandwidth around 57 kHz. The overall filter curve is shown in Fig.16 and a more detailed curve of the RDS 57 kHz band in Fig.17.

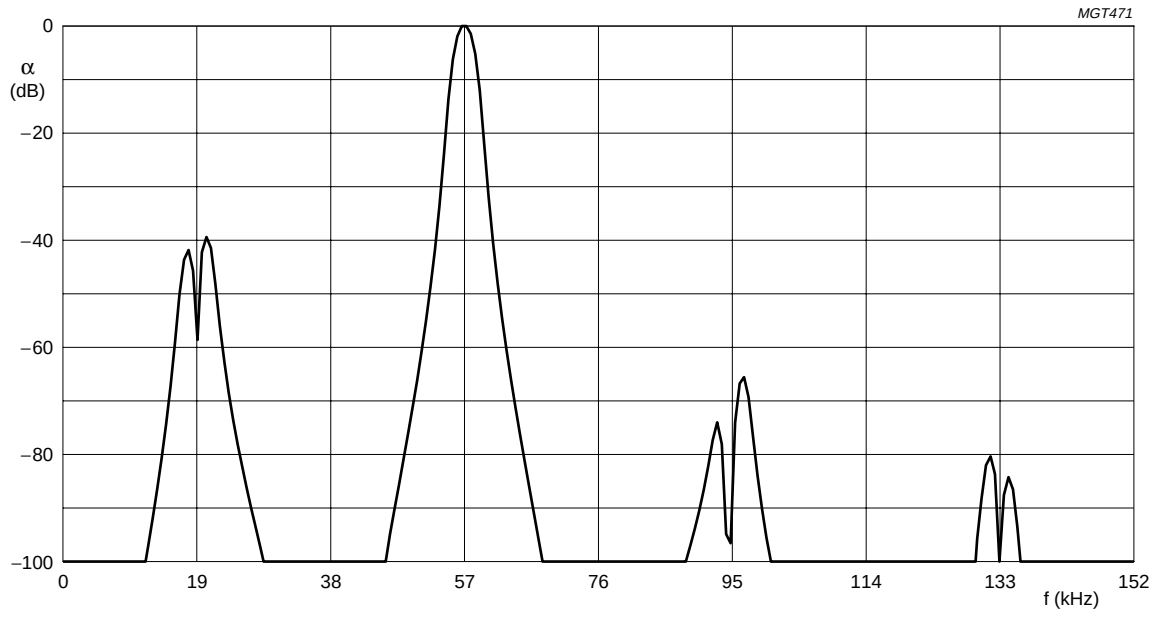



Fig.16 Overall frequency response curve decimation filters.

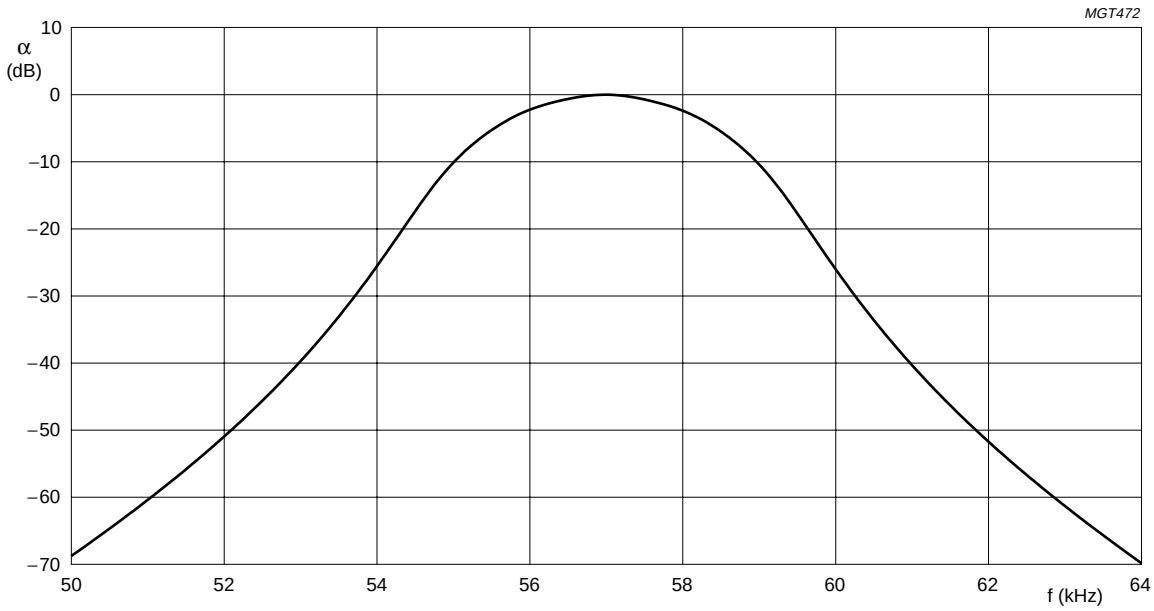



Fig.17 Detailed frequency response curve RDS channel.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDS_CLOCK and RDS_DATA. In the event of FM-stereo reception the clock of the total chip is locked to the stereo pilot (19 kHz multiple). In the event of FM-mono the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases like AM reception or tape, the DCS circuit has to be set in a preset position by means of an $I^2C$-bus bit. Under these conditions the RDS system is always clocked by the DCS clock in a 38 kHz ($4 \times 9.5$ kHz) based sequence.

### 8.15.2 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 μs after the clock transition. The timing of the data change is 100 μs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller. The RDS timing is shown in Fig.18. During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

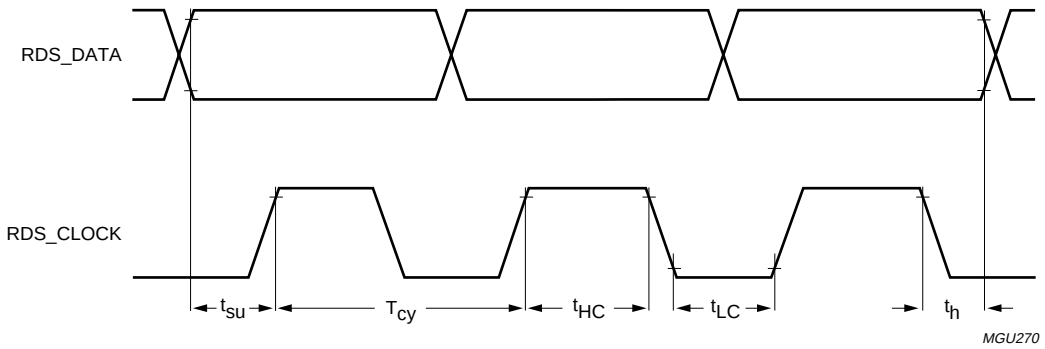



Fig.18 RDS timing in the direct output mode.

### 8.15.3 Buffering of RDS data

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microcontroller for every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

### 8.15.4 Buffer interface

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled down and the buffer is overwritten. The microcontroller has to monitor the data line in at most every 13.5 ms. This mode can be selected via an $I^2C$-bus.

In Fig.19 the interface signals from the RDS decoder and the microcontroller in buffer mode are shown. When the buffer is filled with 16 bits the data line is pulled down. The data line will remain LOW until reading of the buffer is started by pulling down the clock line. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the line HIGH. The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH. When a new 16-bit buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| S/N | signal-to-noise ratio | | | | | |
| | CD, TAPE, AM and AUX input signals | input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS); $f_s$ = 44.1 kHz | 85 | 90 | – | dB |
| | FM_MPX input signal mono | input signal at 1 kHz; bandwidth = 19 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H | 80 | 83 | – | dB |
| | FM_MPX input signal stereo | input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H | 75 | 81 | – | dB |
| $\alpha_{19}$ | carrier and harmonic suppression at the output | pilot signal frequency = 19 kHz | – | 81 | – | dB |
| | | unmodulated | – | 98 | – | dB |
| $\alpha_{38}$ | carrier and harmonic suppression at the output | subcarrier frequency = 38 kHz | – | 83 | – | dB |
| | | unmodulated | – | 91 | – | dB |
| $\alpha_{57}$ | carrier and harmonic suppression for 19 kHz, including notch | subcarrier frequency = 57 kHz | – | 83 | – | dB |
| | | unmodulated | – | 96 | – | dB |
| $\alpha_{76}$ | carrier and harmonic suppression for 19 kHz, including notch | subcarrier frequency = 76 kHz | – | 84 | – | dB |
| | | unmodulated | – | 94 | – | dB |
| $IM_{\alpha 10}$ | intermodulation | $f_{mod}$ = 10 kHz; $f_{spur}$ = 1 kHz | 77 | – | – | dB |
| $IM_{\alpha 13}$ | intermodulation | $f_{mod}$ = 13 kHz; $f_{spur}$ = 1 kHz | 76 | – | – | dB |
| $\alpha_{57(VF)}$ | traffic radio suppression | f = 57 kHz | – | 110 | – | dB |
| $\alpha_{67(SCA)}$ | Subsidiary Communication Authority (SCA) suppression | f = 67 kHz | – | 110 | – | dB |
| $\alpha_{114}$ | adjacent channel suppression | f = 114 kHz | – | 110 | – | dB |
| $\alpha_{190}$ | adjacent channel suppression | f = 190 kHz | – | 110 | – | dB |
| $V_{th(pilot)(rms)}$ | pilot threshold voltage (RMS value) at pin DSP1_OUT1 | stereo on; VOLFM = 07H | – | 35.5 | – | mV |
| | | stereo off; VOLFM = 07H | – | 35.4 | – | mV |
| hys | hysteresis of $V_{th(pilot)(rms)}$ | | – | 0 | – | dB |
| $\alpha_{cs1}$ | channel separation FM-stereo input | $f_i$ = 1 kHz | 40 | 45 | – | dB |
| | | $f_i$ = 10 kHz | 25 | 30 | – | dB |
| $\alpha_{cs2}$ | channel separation CD, TAPE, AM and AUX input signals | | 60 | 70 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $f_{res}$ | audio frequency response | | | | | |
| | CD, TAPE, AM and AUX input signals | $f_s$ = 44.1 kHz; at –3 dB | 20 | – | – | kHz |
| | FM_MPX input signal | at –3 dB via DSP at DAC output | 17 | – | – | kHz |
| $\Delta G_{L-R}$ | overall left/right gain unbalance (TAPE, CD, AUX and AM input signals) | | – | – | 0.5 | dB |
| $\alpha_{ct}$ | crosstalk between inputs | $f_i$ = 1 kHz | 65 | – | – | dB |
| | | $f_i$ = 15 kHz | 50 | – | – | dB |
| $PSRR_{MPX/RDS}$ | power supply ripple rejection MPX and RDS ADCs | output via $I^2S$-bus; ADC input short-circuited; $f_{ripple}$ = 1 kHz; $V_{ripple}$ = 100 mV (peak); $C_{VREFAD}$ = 22 µF; $C_{VDACP}$ = 10 µF | 35 | 45 | – | dB |
| $PSRR_{LAD}$ | power supply ripple rejection level-ADC | output via DAC; ADC input short-circuited; $f_{ripple}$ = 1 kHz; $V_{ripple}$ = 100 mV (peak); $C_{VREFAD}$ = 22 µF | 29 | 39 | – | dB |
| $CMRR_{CD}$ | common-mode rejection ratio for CD input mode | $R_{CD\_(L)\_GND}$ = 1 MΩ; resistance of CD player ground cable < 1 kΩ; $f_i$ = 1 kHz | 60 | – | – | dB |
| **AC characteristics PHONE and NAV inputs; $T_{amb}$ = 25 °C; $V_{DDA1}$ = 3.3 V** | | | | | | |
| THD | total harmonic distortion of PHONE and NAV input signals at maximum input voltage | $V_i$ = 0.75 V (RMS); $f_i$ = 1 kHz; VOLMIX = 30H; measured at FLV and FRV outputs | 40 | – | – | dB |
| CMRR | common mode rejection ratio of PHONE and NAV input signals | $V_i$ = 0.75 V(RMS); $f_i$ = 1 kHz; VOLMIX = 30H | 25 | 50 | – | dB |
| $R_i$ | input impedance of PHONE, NAV/AM_L and AM_R input signals | | 90 | 120 | 150 | kΩ |
| $V_{i(max)(rms)}$ | maximum input level of PHONE and NAV input signals (RMS value) | $f_i$ = 1 kHz; VOLMIX = 30H | 0.75 | 1 | – | V |
| **AC characteristics FM_RDS input; $T_{amb}$ = 25 °C; $V_{DDA1}$ = 3.3 V** | | | | | | |
| $V_{i(con)(max)(rms)}$ | maximum conversion level of FM_RDS input (RMS value) | THD < 1%; VOLRDS = 00H | 0.33 | 0.368 | – | V |
| $R_{i(FM\_RDS)}$ | input resistance FM_RDS input | | 40 | 60 | 72 | kΩ |
| $THD_{FM\_RDS}$ | total harmonic distortion RDS ADC | $f_c$ = 57 kHz | –60 | –67 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **I²S-bus timing** (see Fig.23) | | | | | | |
| $t_r$ | rise time | $T_{cy}$ = 325 ns | – | – | $0.15T_{cy}$ | ns |
| $t_f$ | fall time | $T_{cy}$ = 325 ns | – | – | $0.15T_{cy}$ | ns |
| $T_{cy}$ | bit clock cycle time | | 325 | – | – | ns |
| $t_{BCK(H)}$ | bit clock time HIGH | $T_{cy}$ = 325 ns | $0.35T_{cy}$ | – | – | ns |
| $t_{BCK(L)}$ | bit clock time LOW | $T_{cy}$ = 325 ns | $0.35T_{cy}$ | – | – | ns |
| $t_{su(D)}$ | data set-up time | $T_{cy}$ = 325 ns | $0.2T_{cy}$ | – | – | ns |
| $t_{h(D)}$ | data hold time | $T_{cy}$ = 325 ns | $0.2T_{cy}$ | – | – | ns |
| $t_{d(D)}$ | data delay time | $T_{cy}$ = 325 ns | – | – | $0.15T_{cy}$ | ns |
| $t_{su(WS)}$ | word select set-up time | $T_{cy}$ = 325 ns | $0.2T_{cy}$ | – | – | ns |
| $t_{h(WS)}$ | word select hold time | $T_{cy}$ = 325 ns | $0.2T_{cy}$ | – | – | ns |

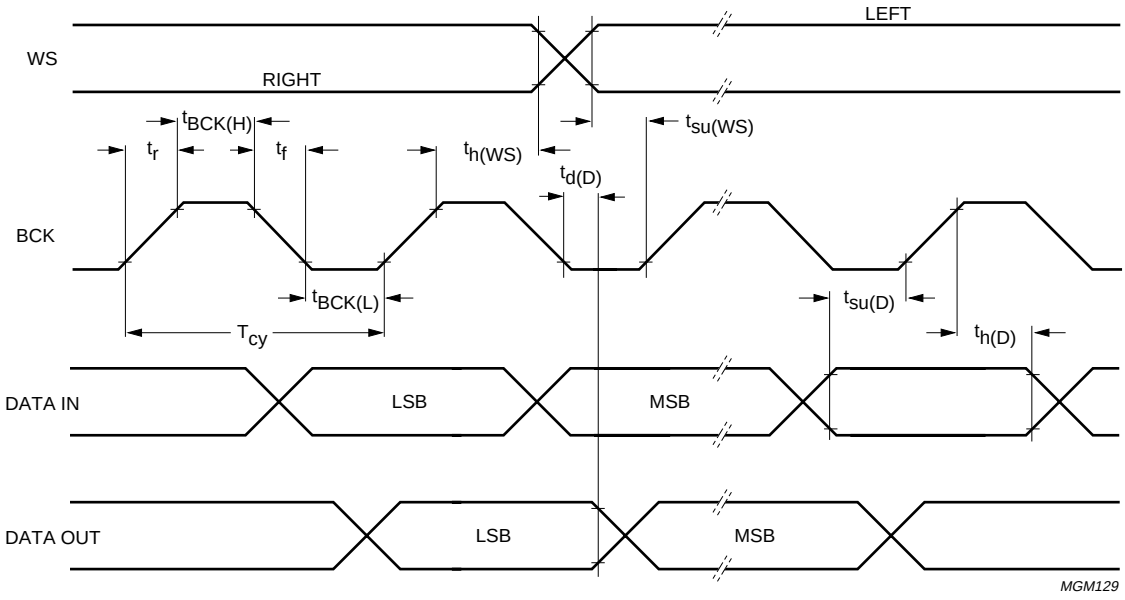



Fig.23 Input timing digital audio data inputs.

## 14 I²C-BUS TIMING

$T_{amb}$ = 25 °C; $V_{DDD}$ = 3.3 V; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | STANDARD MODE I²C-BUS | | FAST MODE I²C-BUS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| $f_{SCL}$ | SCL clock frequency | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | | 4.7 | – | 1.3 | – | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition. After this period, the first clock pulse is generated | | 4.0 | – | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | 4.7 | – | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 4.0 | – | 0.6 | – | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 4.7 | – | 0.6 | – | µs |
| $t_{HD;DAT}$ | data hold time | | 0 | – | 0 | 0.9 | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | 100 | – | ns |
| $t_r$ | rise time of both SDA and SCL signals | $C_b$ in pF | – | 1000 | $20 + 0.1C_b$ | 300 | ns |
| $t_f$ | fall time of both SDA and SCL signals | $C_b$ in pF | – | 300 | $20 + 0.1C_b$ | 300 | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | 4.0 | – | 0.6 | – | µs |
| $C_b$ | capacitive load for each bus line | | – | 400 | – | 400 | pF |
| $t_{SP}$ | pulse width of spikes to be suppressed by input filter | | – | – | 0 | 50 | ns |

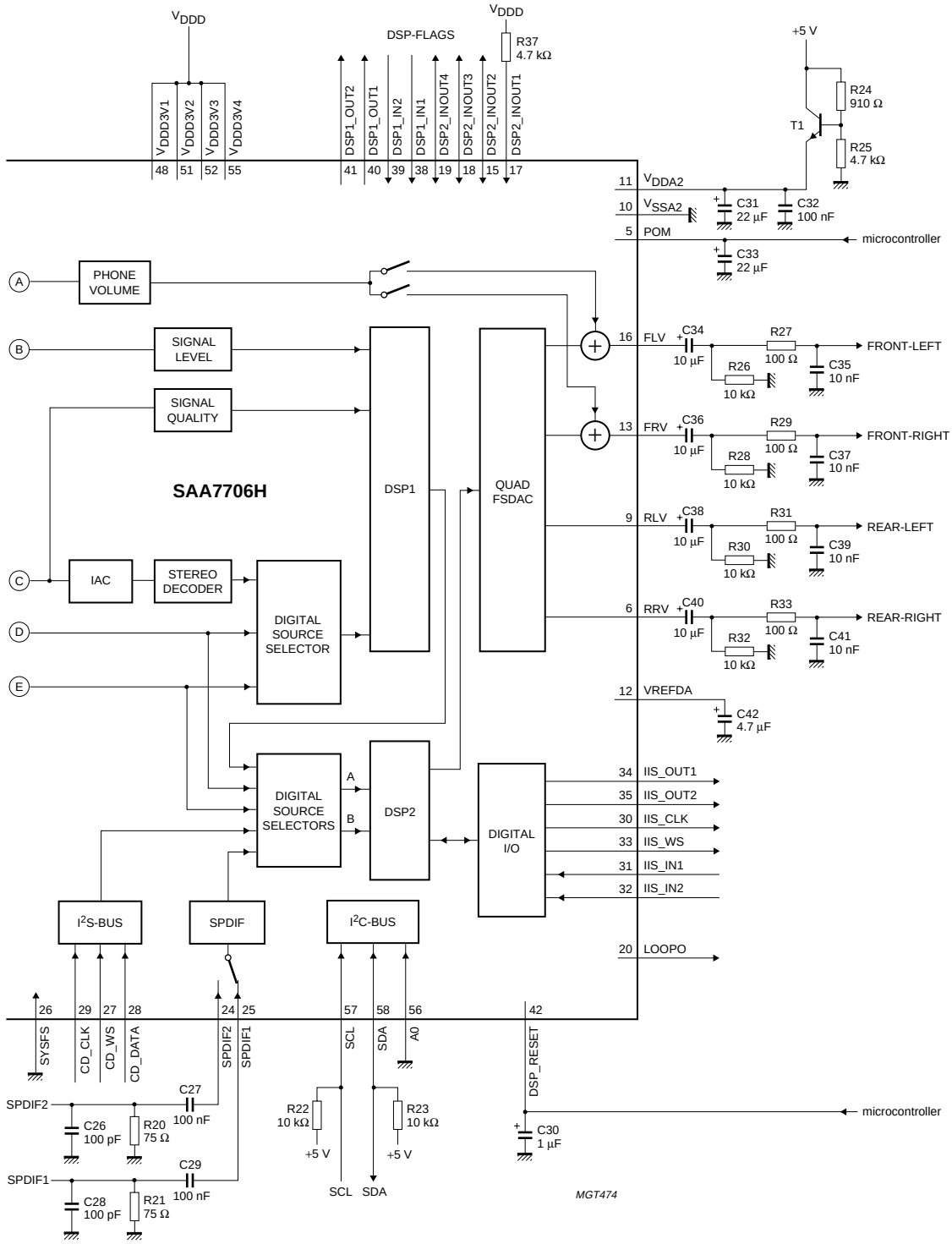
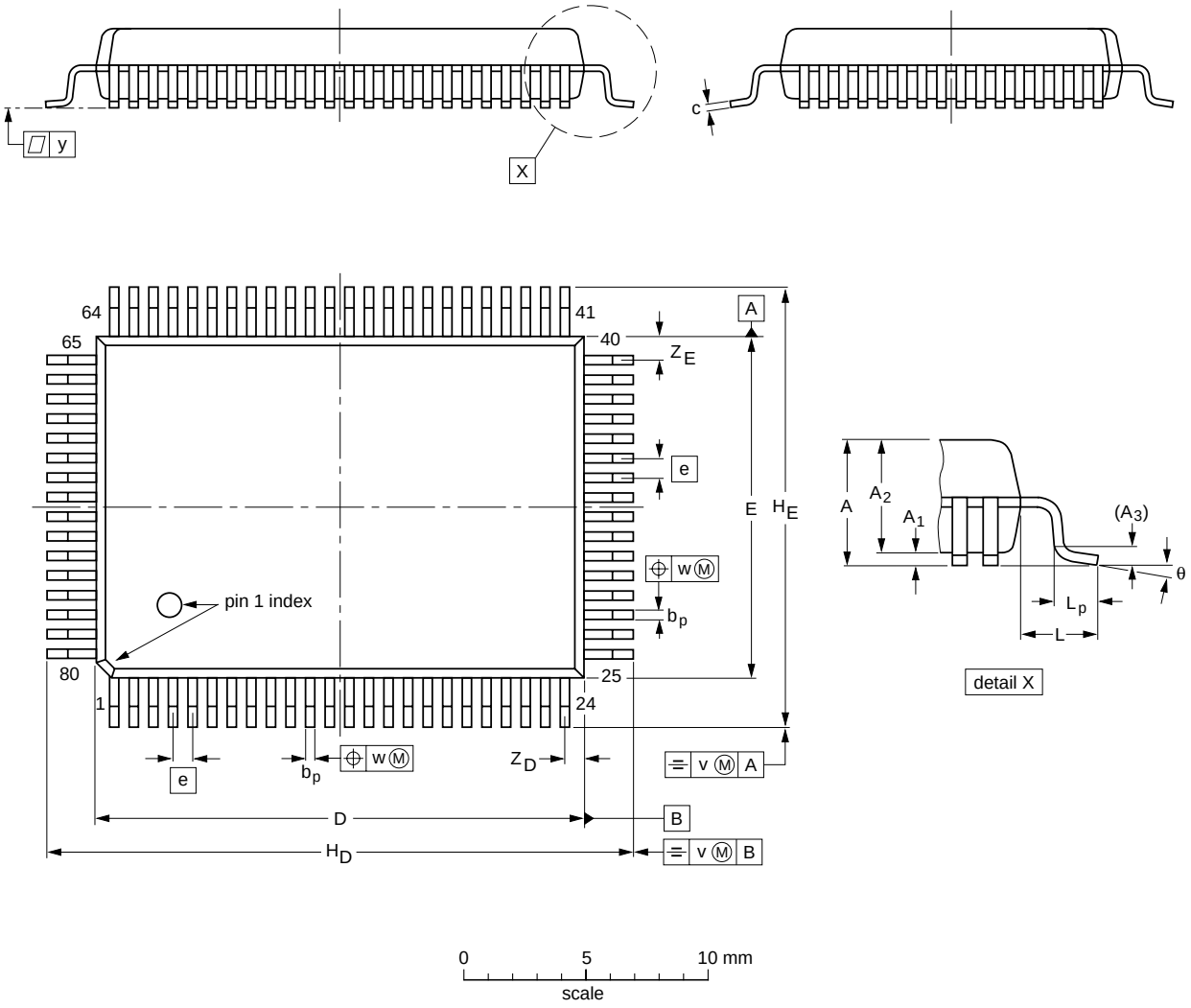



Fig.26 Application diagram (continued from Fig.25).

## 17 PACKAGE OUTLINE

**QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm** **SOT318-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 3.2 | 0.25<br>0.05 | 2.90<br>2.65 | 0.25 | 0.45<br>0.30 | 0.25<br>0.14 | 20.1<br>19.9 | 14.1<br>13.9 | 0.8 | 24.2<br>23.6 | 18.2<br>17.6 | 1.95 | 1.0<br>0.6 | 0.2 | 0.2 | 0.1 | 1.0<br>0.6 | 1.2<br>0.8 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT318-2 | | MO-112 | | | | ~~97-08-01~~<br>99-12-27 |

### 18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.