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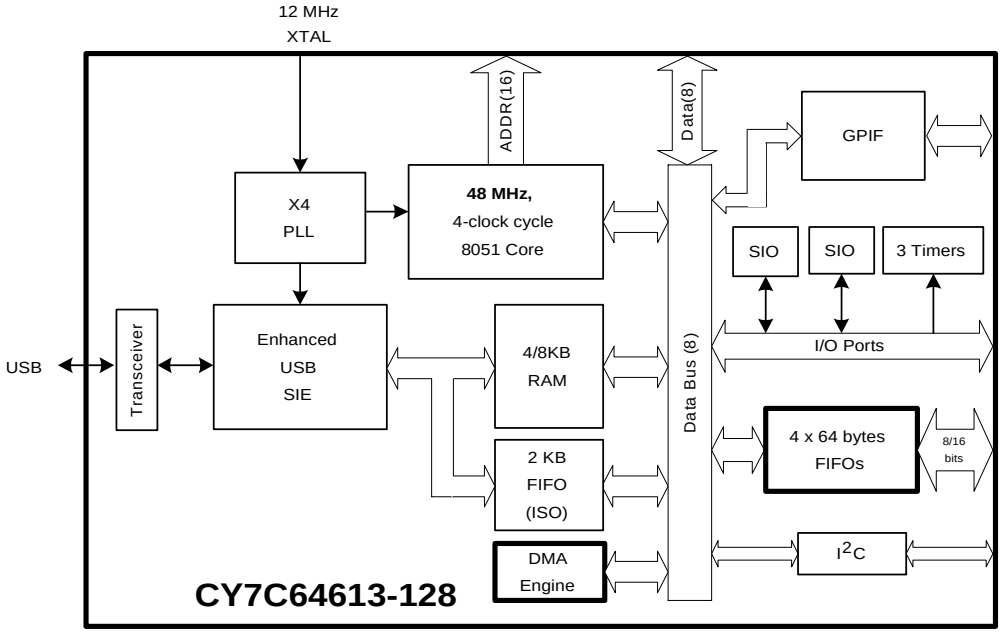
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C646xx
RAM Size	8K x 8
Interface	I²C, USB, USART
Number of I/O	40
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64613-128nc

1.0 Features

The CY7C646xx (EZ-USB *FX)* is Cypress Semiconductor's second-generation full-speed USB family. *FX* products offer higher performance and a higher level of integration than first-generation EZ-USB products. The FX builds on the EZ-USB feature set, including an intelligent USB core, enhanced 8051, 8-Kbyte RAM, and high-performance I/O. The CY7C646xx enhances the EZ-USB family by providing faster operation and more ways to transfer data into and out of the chip at very high speed.



1.1 EZ-USB *FX* Features

- **Single-chip integrated USB Transceiver, Serial Interface Engine (SIE), and Enhanced 8051 Microprocessor**
- **Soft: 8051 runs from internal RAM, which is:**
  - **Downloaded via USB, or**
  - **Loaded from EEPROM**
- **14 Bulk/Interrupt endpoints, each with a maximum packet size of 64 bytes**
- **16 Isochronous endpoints, with 2 KB of buffer space (1 KB, double buffered) which may be divided among the sixteen isochronous endpoints**
- **Integrated, industry standard 8051 with enhanced features:**
  - **Four clocks per cycle**
  - **Two UARTS**
  - **Three counter/timers**
  - **Expanded interrupt system**
  - **Two data pointers**
- **3.3-volt operation**
- **Smart Serial Interface Engine (SIE)**
- **Vectored USB interrupts**
- **Separate buffers for the SETUP and DATA portions of a CONTROL transfer**
- **Integrated I^2C™ controller**
- **48-MHz or 24-MHz 8051 operation**
- **Enhanced IO**
  - **IO port registers mapped to SFRs**
  - **Port bits can be controlled using 8051 bit addressing instructions**
- **Four integrated general purpose 8-bit FIFOs**
  - **64 bytes each**
  - **Automatic conversion to and from 16-bit buses**

  - **FIFOs can use externally supplied clock**
  - **Easy interface to ASIC and DSP ICs**
  - **Brings glue FIFOs inside for lower system cost**
- **DMA Controller**
  - **Moves data between slave FIFOs, memory, and ports**
  - **Very fast transfers—one clock (20.8 ns) per byte for internal transfers**
  - **Can use external RAM as additional FIFO (addressed through A/D buses)**
- **Special Autovectors for DMA and FIFO interrupts**
- **400-kHz or 100-kHz I^2C operation**
- **General Programmable Interface (GPIF)**
  - **Allows direct connection to most parallel interfaces: 8- and 16-bit**
  - **Programmable Waveform Descriptors and Configuration Registers to define waveforms**
  - **Supports multiple Ready (RDY) inputs and Control (CTL) outputs**
- **Three package options - 128-pin PQFP, 80-pin PQFP, and 52-pin PQFP**

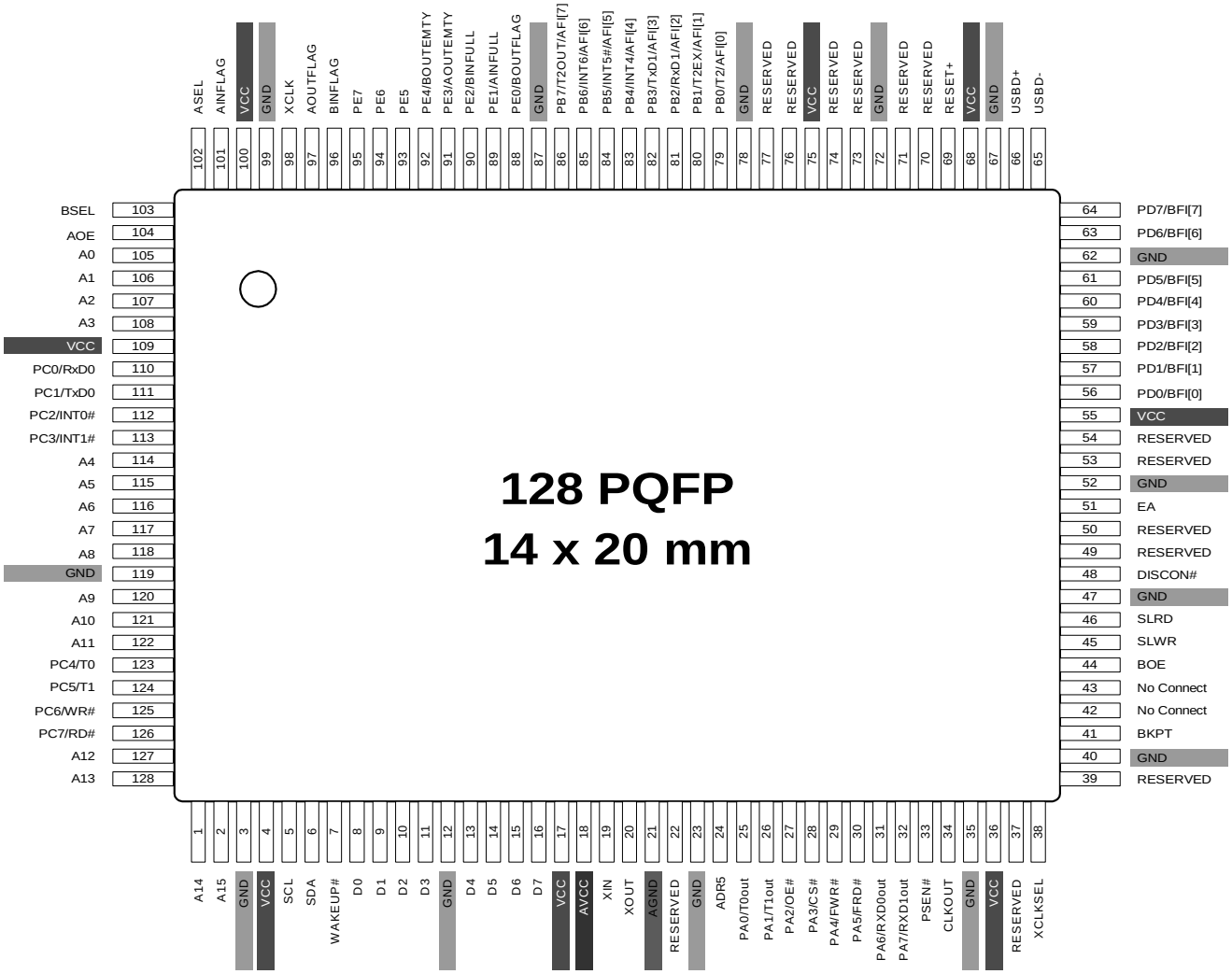
1.2 Example Applications

- **DSL modems**
- **ATAPI interface**
- **Memory card readers**
- **Legacy conversion devices**
- **Cameras**
- **Scanners**
- **Home PNA**
- **Wireless LAN**
- **MP3 players**
- **Networking**

2.0 Functional Overview

The CY7C646xx enhances the line of Cypress EZ-USB chips while maintaining code compatibility. The CY7C646xx builds on the feature set that has already made the EZ-USB family a popular choice for high-integration, high-speed USB applications:

- **Soft operation.** Program code can be downloaded into on-chip RAM via the USB cable, eliminating the need for external program memory or mask ROM headaches.
- **Enhanced 8051.** A speedy four clocks per cycle, plus expanded features.
- **Smart SIE.** The USB Serial Interface Engine does much of the low-level USB overhead in logic, simplifying the 8051 code.
- **DMA for very fast 8-bit or 16-bit transfers.** In the fastest (synchronous byte) mode, one byte can be transferred per 48-MHz clock, or every 20.8 nanoseconds.
- **General Programmable Interface (GPIF).** A reconfigurable 8- or 16-bit parallel interface allows the CY7C646xx to perform local bus mastering, and can implement a wide variety of protocols such as ATAPI, printer parallel port, and Utopia.
- **Abundant endpoints and buffers.** 16x64 byte buffers for bulk/interrupt/control endpoints, 2x1024 byte FIFOs for up to 16 isochronous endpoints.
- **Glueless memory expansion.** The 8051 16-bit address bus and 8-bit data bus is available, along with strobes RD#, WR#, OE# and CS#. The buses are brought out on separate pins (not multiplexed, as in the standard 8051), saving one clock per external memory cycle.
- **48-MHz or 24-MHz 8051 selectable by EEPROM configuration byte.**
- **Five 8-bit IO ports.**
- **Optimum 8051 IO efficiency.** IO pins can be addressed as external registers (as in EZ-USB) or through 8051 SFR (Special Function Register) bits for faster operation.
- **Four internal FIFOs for glueless interface to ASICs, DSPs, or external logic.** These FIFOs can be clocked either by an internal or external clock, and can operate either synchronously (using strobes and a clock) or asynchronously (using strobes only). The FIFOs have 8-16 and 16-8 bit conversion modes that simplify interface to external data buses.
- **The vectored interrupt system is expanded to accommodate the FIFO flags and DMA systems.** Also, the 8051 can clear the USB (INT2) or the FIFO/DMA (INT4) interrupt request bit for the interrupt currently being serviced by writing an SFR location, saving time and code in the interrupt service routine.
- **400-kHz or 100-kHz I^2C bus controller speed.**



3.2 CY7C646xx Pin Descriptions

128	80	52	Name	Type	Default	Description
18	5	5	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
21	8	8	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
48	28	18	DISCON#	O/Z	H	**Disconnect**. This pin can drive HIGH, LOW, or float. DISCON# pin floats when the register bit USBCS.2 is LOW, and drives when it is HIGH. The drive level of the DISCON# pin is the invert of register bit USBCS.3. The DISCON# pin is normally connected to the USB D+ line through a 1500Ω resistor. The CY7C646xx signals a USB connection by setting USBCS.3=0 (drive 3.3V) and USBCS.2=1 (output enable). The CY7C646xx signals a USB disconnect by setting USBCS.2=0 which floats the pin and disconnects the 1500Ω resistor from D+.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
82	50	32	PB3 or TXD1 or D[3] or GDA[3] or AFI [3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.3 and IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **TXD1**is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode. **AFI [3]** is the bidirectional A-FIFO data bus.
83	51	33	PB4 or INT4 or D[4] or GDA[4] or AFI [4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.4 and IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH. **AFI [4]** is the bidirectional A-FIFO data bus.
84	52	34	PB5 or INT5# or D[5] or GDA[5] or AFI [5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.5 and IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW. **AFI [5]** is the bidirectional A-FIFO data bus.
85	53	35	PB6 or INT6 or D[6] or GDA[6] or AFI [6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.6 and IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **INT6** is the 8051 INT5 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH. **AFI [6]** is the bidirectional A-FIFO data bus.
86	54	36	PB7 or T2OUT or D[7] or GDA[7] or AFI [7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.7 and IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **T2OUT** is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows. **AFI [7]** is the bidirectional A-FIFO data bus.
Port C						
110	68	43	PC0 or RXD0 or RDY0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by the PORTCCFG.0 and PORTCGPIF.0 bits. **PC0** is a bidirectional I/O port pin. **RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes. **RDY0** is a GPIF input signal.
111	69	44	PC1 or TXD0 or RDY1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by the PORTCCFG.1 and PORTCGPIF.1 bits. **PC1** is a bidirectional I/O port pin. **TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. **RDY1** is a GPIF input signal.
112	70	45	PC2 or INT0#	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by the PORTCCFG.2 bit. **PC2** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
113	71	46	PC3 or INT1# or RDY3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by the: PORTCCFG.3 and PORTCGPIF.3 bits. **PC3** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0). **RDY3** is a GPIF input signal.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
123	73	48	PC4 or T0 or CTL1	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by the PORTCCFG.4 and PORTCGPIF.4 bits. **PC4** is a bidirectional I/O port pin. **T0** is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit. **CTL1** is a GPIF output signal.
124	74	49	PC5 or T1 or CTL3	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by the PORTCCFG.5 and PORTCGPIF.5 bits. **PC5** is a bidirectional I/O port pin. **T1** is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit. **CTL3** is a GPIF output signal.
125	75	50	PC6 or WR# or CTL4	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by the PORTCCFG.6 and PORTCGPIF.6 bits. **PC6** is a bidirectional I/O port pin. **WR#** is the active-LOW write strobe output for external memory. If the WR# signal is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on. **CTL4** is a GPIF output signal.
126	76	51	PC7 or RD# or CTL5	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by the PORTCCFG.7 and PORTCGPIF.7 bits. **PC7** is a bidirectional I/O port pin. **RD#** is the active-LOW read strobe output for external memory. If the RD# signal is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on. **CTL5** is a GPIF output signal.
Port D						
						Port D is multiplexed between three sources: **PD0–PD7** are bidirectional I/O port pins. **GDB[7..0]** is the GPIF B data bus. **BFI[7..0]** is the bidirectional B-FIFO data bus.
56	30		PD0 or GDB[0] or BFI [0]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [0]** is the bidirectional B-FIFO data bus.
57	31		PD1 or GDB[1] or BFI [1]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [1]** is the bidirectional B-FIFO data bus.
58	32		PD2 or GDB[2] or BFI [2]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [2]** is the bidirectional B-FIFO data bus.
59	33		PD3 or GDB[3] or BFI [3]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [3]** is the bidirectional B-FIFO data bus.
60	34		PD4 or GDB[4] or BFI [4]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [4]** is the bidirectional B-FIFO data bus.
61	35		PD5 or GDB[5] or BFI [5]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [5]** is the bidirectional B-FIFO data bus.
63	36		PD6 or GDB[6] or BFI [6]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [6]** is the bidirectional B-FIFO data bus.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
64	37		PD7 or GDB[7] or BFI [7]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [7]** is the bidirectional B-FIFO data bus.
Port E						
88			PE0 or ADR0 or BOUTFLAG	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **PE0** is a bidirectional I/O port pin. **ADR0** is a GPIF address output pin. **BOUTFLAG** is the B-OUT FIFO flag output, which indicates a programmable level of FIFO fullness.
89			PE1 or ADR1 or AINFULL	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **PE1** is a bidirectional I/O port pin. **ADR1** is a GPIF address output pin. **AINFULL** is the A-IN FIFO flag output, which indicates FIFO full.
90			PE2 or ADR2 or BINFULL	I/O/Z	I (PE2)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **PE2** is a bidirectional I/O port pin. **ADR2** is a GPIF address output pin. **BINFULL** is the B-IN FIFO flag output, which indicates FIFO full.
91			PE3 or ADR3 or AOUTEMTY	I/O/Z	I (PE3)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **PE3** is a bidirectional I/O port pin. **ADR3** is a GPIF address output pin. **AOUTEMTY** is the A-OUT FIFO flag output, which indicates FIFO empty.
92			PE4 or ADR4 or BOUTEMTY	I/O/Z	I (PE4)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **PE4** is a bidirectional I/O port pin. **ADR4** is a GPIF address output pin. **BOUTEMTY** is the B-OUT FIFO flag output, which indicates FIFO empty.
93			PE5 or CTL3	I/O/Z	I (PE5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PE5** is a bidirectional I/O port pin. **CTL3** is a GPIF output signal.
94			PE6 or CTL4	I/O/Z	I (PE6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PE6** is a bidirectional I/O port pin. **CTL4** is a GPIF output signal.
95			PE7 or CTL5	I/O/Z	I (PE7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PE7** is a bidirectional I/O port pin. **CTL5** is a GPIF output signal.
24			ADR5	O	X	**ADR5** is a GPIF address output pin.
102	63		RDY0 or ASEL	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY0** is a GPIF input signal. **ASEL** is the select input for the A-IN and A-OUT FIFOs.
103	64		RDY1 or BSEL	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY1** is a GPIF input signal. **BSEL** is the select input for the B-IN and B-OUT FIFOs.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
104	65	42	RDY2 or AOE	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY2** is a GPIF input signal. **AOE** is the output enable input for the A-OUT FIFO.
44	25		RDY3 or BOE	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY3** is a GPIF input signal. **BOE** is the output enable input for the B-OUT FIFO.
45	26		RDY4 or SLWR	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY4** is a GPIF input signal. **SLWR** is the input-only write strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
46	27		RDY5 or SLRD	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY5** is a GPIF input signal. **SLRD** is the input-only read strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
101	62	41	CTL0 or AINFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL0** is a GPIF control output. **AINFLAG** is the A-IN FIFO flag output which indicates a programmable level of FIFO fullness.
96	57		CTL1 or BINFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL1** is a GPIF control output. **BINFLAG** is the B-IN FIFO flag output which indicates a programmable level of FIFO fullness.
97	58	37	CTL2 or AOUTFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL2** is a GPIF control output. **AOUTFLAG** is the A-OUT FIFO flag output which indicates a programmable level of FIFO fullness.
98	59	38	XCLK	Input	N/A	External clock input, used for synchronously clocking data into the slave FIFOs. XCLK also serves as a timing reference for all slave FIFO control signals and GPIF.
53		22	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
54		23	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
70			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
71			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
73			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
74			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
76			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
77			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
50		20	Reserved	Rsrvd	N/A	Reserved. Leave open.
49		19	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
7	4	4	WAKEUP#	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, a HIGH-to-LOW edge on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP# LOW inhibits the EZ-USB chip from suspending.
5	2	2	SCL	OD	Z	**I^2C Clock**. Connect to V_{CC} with a 1K resistor, **even if no I^2C peripheral is attached.**

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
6	3	3	SDA	OD	Z	**I^2C Data**. Connect to V_{CC} with a 1K resistor, **even if no I^2C peripheral is attached.**
38	23	16	XCLKSEL	Input	N/A	HIGH: Use XCLK pin for GPIF and slave FIFOs. LOW: Use internal 48-MHz clock for GPIF and slave FIFOs.
39	24	17	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
37	22	15	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
22	9	9	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
4	1	1	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
17			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
36	21	14	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
55			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
68	41	27	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
75			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
100	61	40	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
109			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
3	80	52	GND	Ground	N/A	Ground.
12			GND	Ground	N/A	Ground.
23	10		GND	Ground	N/A	Ground.
35	20	13	GND	Ground	N/A	Ground.
40			GND	Ground	N/A	Ground.
47			GND	Ground	N/A	Ground.
52	29	21	GND	Ground	N/A	Ground.
62			GND	Ground	N/A	Ground.
67	40	26	GND	Ground	N/A	Ground.
72	43		GND	Ground	N/A	Ground.
78			GND	Ground	N/A	Ground.
87			GND	Ground	N/A	Ground.
99	60	39	GND	Ground	N/A	Ground.
119	72	47	GND	Ground	N/A	Ground.
42	79		NC	N/A	N/A	No-connect. This pin must be left open.
43	44		NC	N/A	N/A	No-connect. This pin must be left open.
	45		NC	N/A	N/A	No-connect. This pin must be left open.
	46		NC	N/A	N/A	No-connect. This pin must be left open.
	55		NC	N/A	N/A	No-connect. This pin must be left open.
	56		NC	N/A	N/A	No-connect. This pin must be left open.
	66		NC	N/A	N/A	No-connect. This pin must be left open.
	67		NC	N/A	N/A	No-connect. This pin must be left open.
	77		NC	N/A	N/A	No-connect. This pin must be left open.
	78		NC	N/A	N/A	No-connect. This pin must be left open.

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
781D	ABPOLAR	FIFO Control Signals Polarity	0	0	BOE	AOE	SLRD	SLWR	ASEL	BSEL
781E	ABFLUSH	Write (data=x) to reset all flags	*	*	*	*	*	*	*	*
781F-7823 (reserved)										
7824	WFSELECT	Waveform Selector	SINGLEWR		SINGLERD		FIFOWR		FIFORD	
7825	IDLE_CS	GPIF IDLE State control	DONE	0	0	0	0	0	0	IDLEDRV
7826	IDLECTLOUT	GPIF IDLE CTL states	IOE3	IOE2	IOE1/ CTL5	IOE0/ CTL4	CTL3	CTL2	CTL1	CTL0
7827	CTLOUTCFG	GPIF CTL Drive mode	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0
7828-7829 (reserved)										
782A	GPIFADRL	GPIF Address	*	*	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
782B (reserved)										
782C	AINTC	FIFO A In Transfer Count	FITC	Transfer Count						
782D	AOUTTC	FIFO A Out Transfer Count	FITC	Transfer Count						
782E	ATRIG	Trigger a FIFO A RD/WR	*	*	*	*	*	*	*	*
782F (reserved)										
7830	BINTC	FIFO B In Transfer Count	FITC	Transfer Count						
7831	BOUTTC	FIFO B Out Transfer Count	FITC	Transfer Count						
7832	BTRIG	Trigger a FIFO B RD/WR	*	*	*	*	*	*	*	*
7833 (reserved)										
7834	SGLDATH	GPIF Data High	D15	D14	D13	D12	D11	D10	D9	D8
7835	SGLDATLTRIG	GPIF Data Low and Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7836	SGLDATLN-TRIG	GPIF Data Low and No Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7837(reserved)										
7838	READY	GPIF Ready flags	INTRDY	SAS	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
7839	ABORT	Abort current GPIF cycle	*	*	*	*	*	*	*	*
783A (reserved)										
783B	GENIE	GPIF/DMA Interrupt Enable	0	0	0	0	0	DMADN	GPWR	GPDONE
783C	GENIRQ	GPIF/DMA Interrupt Request	0	0	0	0	0	DMADN	GPWR	GPDONE
783D-7840 (reserved)										
	IO Ports D, E									
7841	OUTD	Output Port D	OUTD7	OUTD6	OUTD5	OUTD4	OUTD3	OUTD2	OUTD1	OUTD0
7842	PINSD	Input Port D pins	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
7843	OED	Port D Output Enable	0ED7	0ED6	0ED5	0ED4	0ED3	0ED2	0ED1	0ED0
7844 (reserved)										
7845	OUTE	Output Port E	OUTE7	OUTE6	OUTE5	OUTE4	OUTE3	OUTE2	OUTE1	OUTE0
7846	PINSE	Input Port E pins	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0
7847	OEE	Port E Output Enable	OEE7	OEE6	OEE5	OEE4	OEE3	OEE2	OEE1	OEE0
7848 (reserved)										
7849	PORTSETUP	Timer0 Clock source, Port-to-SFR mapping	0	0	0	0	0	0	T0CLK	SFRPORT
784A	IFCONFIG	Select 8/16 bit data bus, configure buses (IF)	52ONE	0	0	0	GSTATE	BUS16	IF1	IF0
784B	PORTACF2	Port A Configuration #2	0	0	SLRD	SLWR	0	0	0	0

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
784C	PORTCCF2	Port C Configuration #2	CTL5	CTL4	CTL3	CTL1	RDY3	0	RDY1	RDY0
784D-784E (reserved)										
	DMA Control									
784F	DMASRCH	DMA Source H	A15	A14	A13	A12	A11	A10	A9	A8
7850	DMASRCL	DMA Source L	A7	A6	A5	A4	A3	A2	A1	A0
7851	DMADESTH	DMA Destination H	A15	A14	A13	A12	A11	A10	A9	A8
7852	DMADESTL	DMA Destination L	A7	A6	A5	A4	A3	A2	A1	A0
7853 (reserved)										
7854	DMALEN	DMA Transfer Length	D7	D6	D5	D4	D3	D2	D1	D0
7855	DMAGO	Start DMA Transfer	DONE	*	*	*	*	*	*	*
7856 (reserved)										
7857	DMABURST	DMA Burst control	*	*	*	DSTR2	DSTR1	DSTR0	RB	WB
7858	DMAEXTFIFO	Dummy data reg for using RAM as external FIFO	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
7859 - 785C (reserved)										
785D	INT4IVEC	Interrupt 4 Vector	0	1	I4V3	I4V2	I4V1	I4V0	0	0
785E	INT4SETUP	Interrupt 4 Set-up	0	0	0	0	0	INT4SFC	INTERNAL	AV4EN
785F-78FF (reserved)										
7900-797F	WFDESC	GPIF Waveform Descriptors								
7980-7B3F (reserved)										
	Endpoint 0–7 Data Buffers									
7B40	OUT7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7B80	IN7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7BC0	OUT6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C00	IN6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C40	OUT5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C80	IN5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7CC0	OUT4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D00	IN4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D40	OUT3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D80	IN3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7DC0	OUT2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E00	IN2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E40	OUT1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E80	IN1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7EC0	OUT0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7F00	IN0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7F40-7F5F (reserved)										
	Isochronous Data									
7F60	OUT8DATA	Endpoint 8 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F61	OUT9DATA	Endpoint 9 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F62	OUT10DATA	Endpoint 10 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F63	OUT11DATA	Endpoint 11 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F64	OUT12DATA	Endpoint 12 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0
7F9F	UART230	230k Baud Configuration	0	0	0	0	0	0	UART1	UART0
	Isochronous Control/Status Registers									
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15 ERR	ISO14 ERR	ISO13 ERR	ISO12 ERR	ISO11 ERR	ISO10 ERR	ISO9 ERR	ISO8 ERR
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	0	0	ISODISAB
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8
7FA3 (reserved)										
7FA4 (reserved)										
	I^2C Registers									
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0
7FA7	I2CMODE	STOP Int Enable, I^2C bus speed	0	0	0	0	0	0	STOPIE	400KHZ
	Interrupts									
7FA8	IVEC	Interrupt Vector	0	IV4	IV3	IV2	IV1	IV0	0	0
7FA9	IN07IRQ	EPIN Interrupt Request	IN7IR	IN6IR	IN5IR	IN4IR	IN3IR	IN2IR	IN1IR	IN0IR
7FAA	OUT07IRQ	EPOUT Interrupt Request	OUT7IR	OUT6IR	OUT5IR	OUT4IR	OUT3IR	OUT2IR	OUT1IR	OUT0IR
7FAB	USBIRQ	USB Interrupt Request	0	0	IBNIR	URESIR	SUSPIR	SUTOKIR	SOFIR	SUDAVIR
7FAC	IN07IEN	EP0–7IN Int Enables	IN7IEN	IN6IEN	IN5IEN	IN4IEN	IN3IEN	IN2IEN	IN1IEN	IN0IEN
7FAD	OUT07IEN	EP0–7OUT Int Enables	OUT7IEN	OUT6IEN	OUT5IEN	OUT4IEN	OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN
7FAE	USBIEN	USB Int Enables	0	0	IBNIE	URESIE	SUSPIE	SUTOKIE	SOFIE	SUDAVIE
7FAF	USBBAV	Breakpoint & Autovector	*	*	*	INT2SFC	BREAK	BPPULSE	BPEN	AVEN
7FB0	IBNID	IN-Bulk-NAK ID	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB1	IBNMASK	IN-Bulk-NAK Intr. mask	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB2	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8
7FB3	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0
	Bulk Endpoints 0–7									
7FB4	EP0CS	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP0STALL
7FB5	IN0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB6	IN1CS	Control & Status	*	*	*	*	*	*	in1bsy	in1stl
7FB7	IN1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB8	IN2CS	Control & Status	*	*	*	*	*	*	in2bsy	in2stl
7FB9	IN2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBA	IN3CS	Control & Status	*	*	*	*	*	*	in3bsy	in3stl
7FBB	IN3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBC	IN4CS	Control & Status	*	*	*	*	*	*	in4bsy	in4stl
7FBD	IN4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBE	IN5CS	Control & Status	*	*	*	*	*	*	in5bsy	in5stl
7FBF	IN5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC0	IN6CS	Control & Status	*	*	*	*	*	*	in6bsy	in6stl
7FC1	IN6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC2	IN7CS	Control & Status	*	*	*	*	*	*	in7bsy	in7stl
7FC3	IN7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC4 (reserved)										

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7FF3	OUT11ADDR	Endpt 11 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF4	OUT12ADDR	Endpt 12 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF5	OUT13ADDR	Endpt 13 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF6	OUT14ADDR	Endpt 14 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF7	OUT15ADDR	Endpt 15 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF8	IN8ADDR	Endpt 8 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF9	IN9ADDR	Endpt 9 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFA	IN19ADDR	Endpt 10 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFB	IN11ADDR	Endpt 11 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFC	IN12ADDR	Endpt 12 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFD	IN13ADDR	Endpt 13 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFE	IN14ADDR	Endpt 14 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFF	IN15ADDR	Endpt 15 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0

* - register bit is not used and undefined if read.

5.0 Input/Output Pin Special Consideration

The EZ-USB FX has a weak internal pull-up resistor that is present on the inputs and outputs when the external signal level is a high (above 1.3V). The weak internal pull-up is not present in the circuit when the voltage level of the external signal is low. Since the weak pull-up is only in the circuit when the external signal level is high, this means that if the last voltage level driven on the pin was a high, the pull-up resistor will keep it high. However, if the last voltage level driven on the pin was a low then the pull-up is turned off and the pad can float until it gets to a high logic level. This situation affects both inputs as well as outputs that are three-stated. Use a 25-KΩ or lower pull-down resistor to bring a pin to a low level if needed.

6.0 Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Supplied .....0°C to +70°C

Supply Voltage on V_{CC} relative to V_{SS} .....–0.5V to +4.0V

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC}+0.5V

Power Dissipation .....500 mW

Static Discharge Voltage .....>1000V (per JEDEC standard)

Latch-up Current ..... >200 mA

Max Output Sink Current ..... 10 mA

7.0 Operating Conditions

T_A (Ambient Temperature Under Bias) .....0°C to +70°C

Supply Voltage .....+3.0V to +3.6V

Ground Voltage 0V

F_{OSC} (Oscillator or Crystal Frequency) ..... 12 MHz ± 0.25%

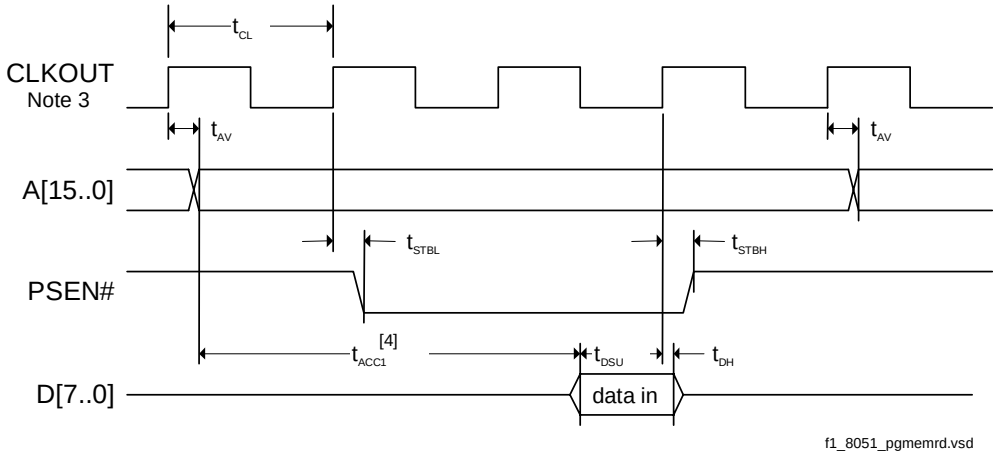
9.0 AC Electrical Characteristics

9.1 USB Transceiver

Specified Conditions: Per Table 7-6 of Revision 1.1 of USB specification

Parameter	Description	Condition	Min.	Max.	Unit
Trise	Rise and Fall Times Full Speed		4	20	ns
Tfall			4	20	ns
t_{RFM}	Rise/Fall Time Matching		90	110	%
Vcr	Crossover Point		1.3	2.0	V

9.2 Program Memory Read



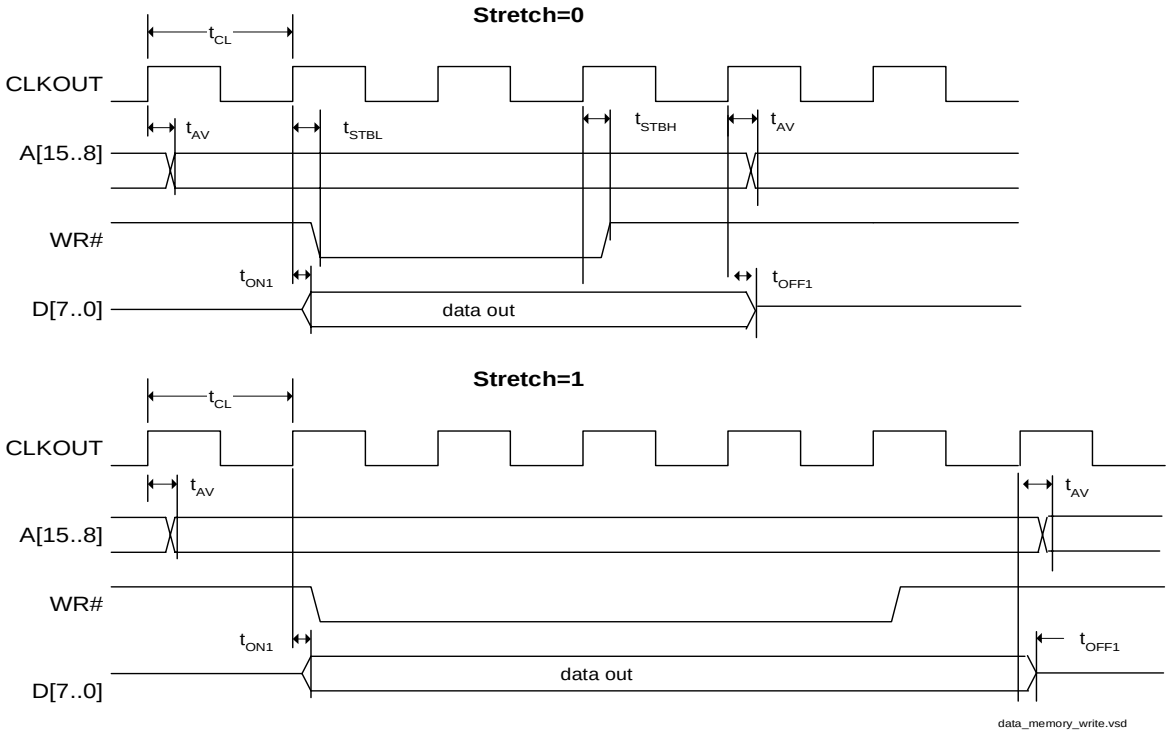
f1_8051_pgmemrd.vsd

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to PSEN Low	0		8	ns	
t_{STBH}	Clock to PSEN High	0		8	ns	
t_{DSU}	Data Set-up to Clock			10	ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

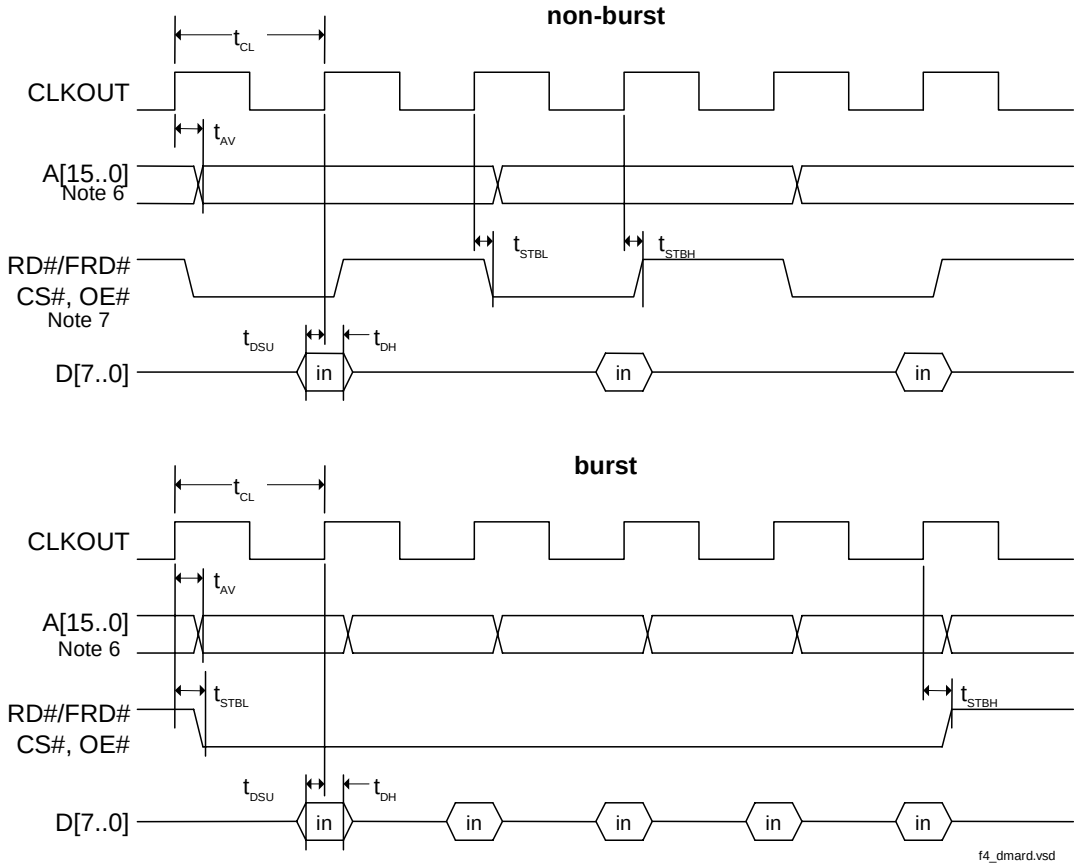
3. CLKOUT is shown with positive polarity.
4. t_{ACC1} is computed from the above parameters as follows:
   t_{ACC1}(24 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 106 ns
   t_{ACC1}(48 Mhz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 44 ns

9.4 Data Memory Write



Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to WR Pulse Low	0	8	ns	
t_{STBH}	Clock to WR Pulse High	0	8	ns	
t_{ON1}	Clock to Data Turn-on	0	7	ns	
t_{OFF1}	Clock to Data Hold Time	–2	7	ns	

9.5 DMA Read

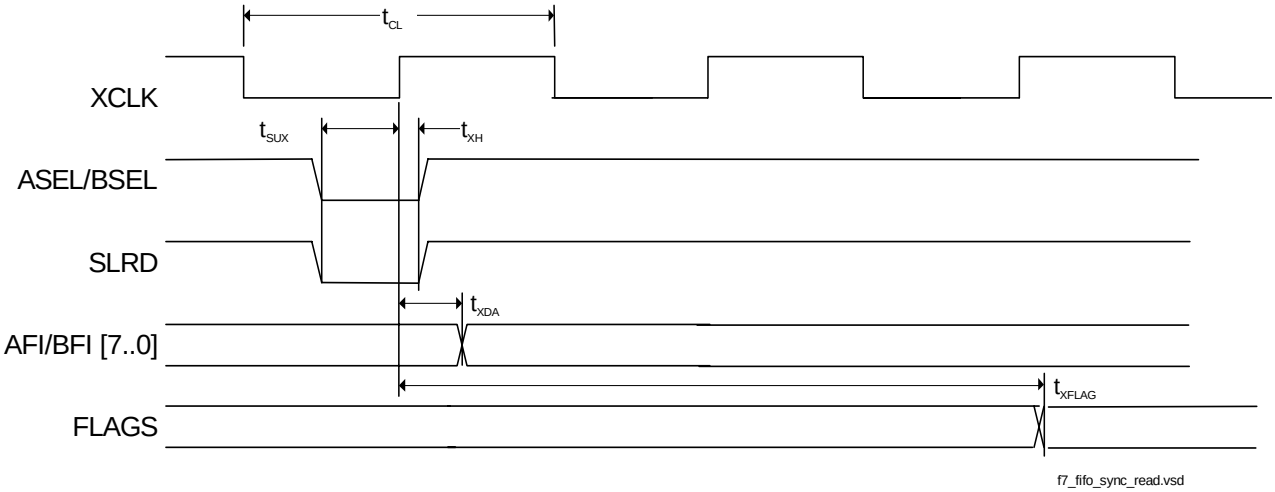


Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to Strobe Low	0	8	ns	Non-burst
t_{STBH}	Clock to Strobe High	0	8	ns	Non-burst
t_{DSU}	Data to Clock Set-up		10	ns	
t_{DH}	Clock to Data Hold	0		ns	

Notes:

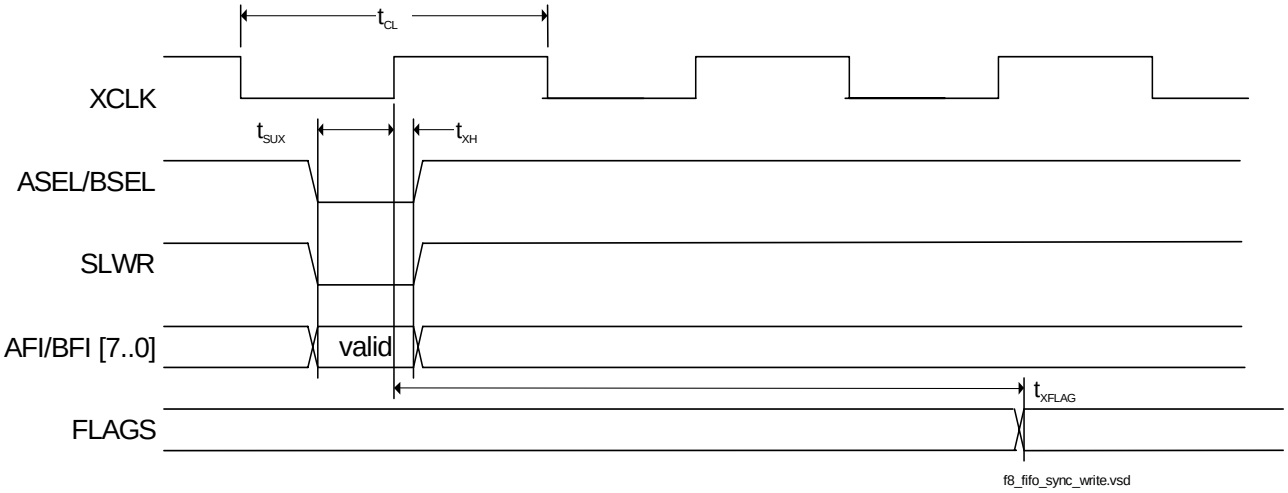
6. The address bus is not used in external FIFO transfers that use FRD#.
7. This is the maximum data rate. The strobes are programmable for longer access times.

9.8 Slave FIFOs—Synchronous Read

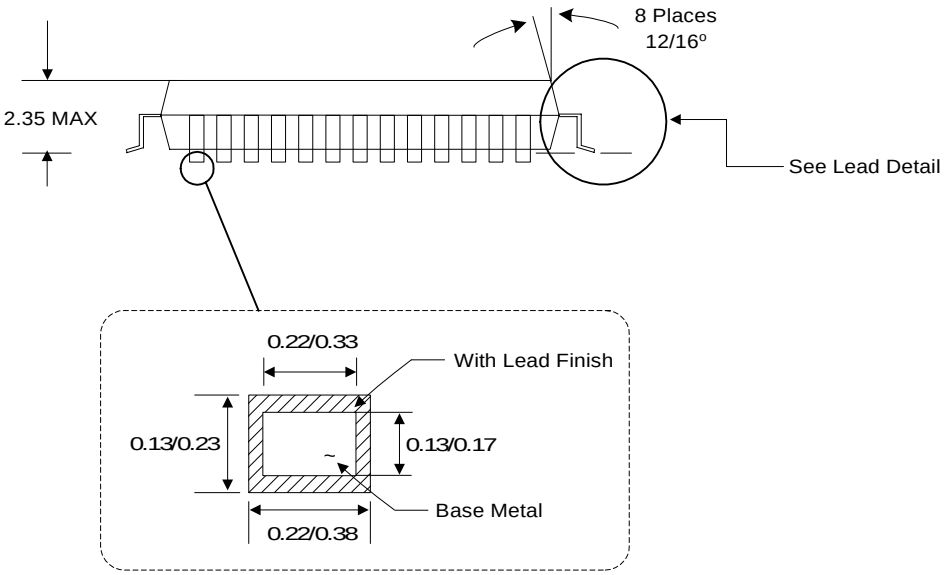


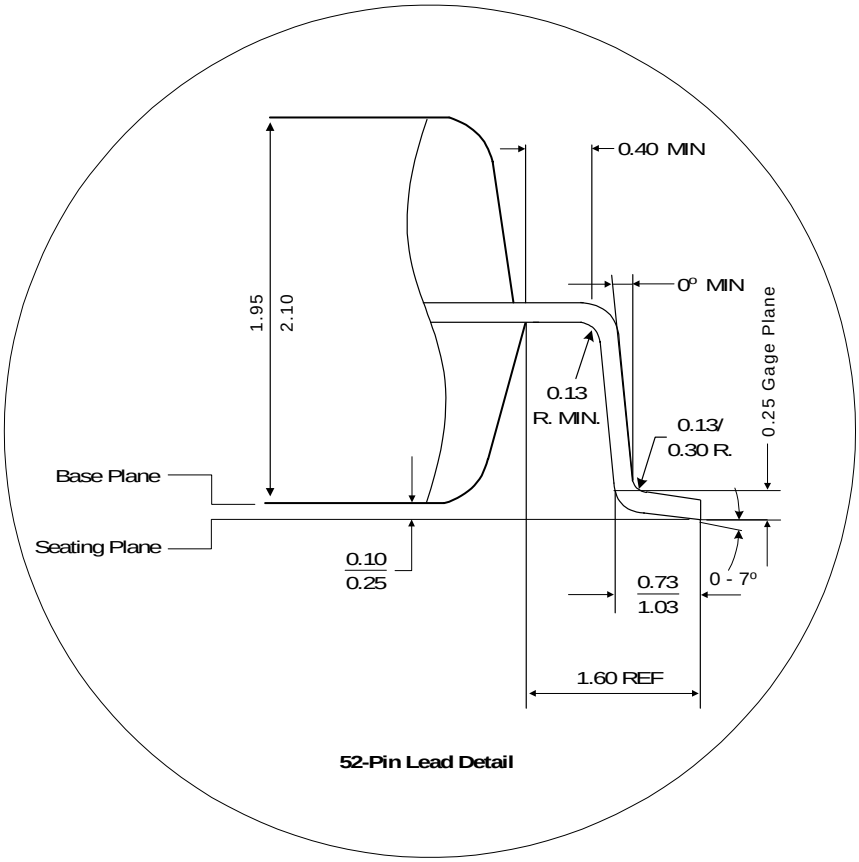
Parameter	Description	Min.	Max.	Unit
t_{SUX}	Strobe & Sel to External Clock Set-up Time		9	ns
t_{XH}	External Clock to Strobe & Sel Hold Time	6		ns
t_{XDA}	Clock to A/B FIFO data		13	ns
t_{XFLAG}	Clock to FIFO flag		$2t_{CL}$+11	ns

9.9 Slave FIFOs—Synchronous Write

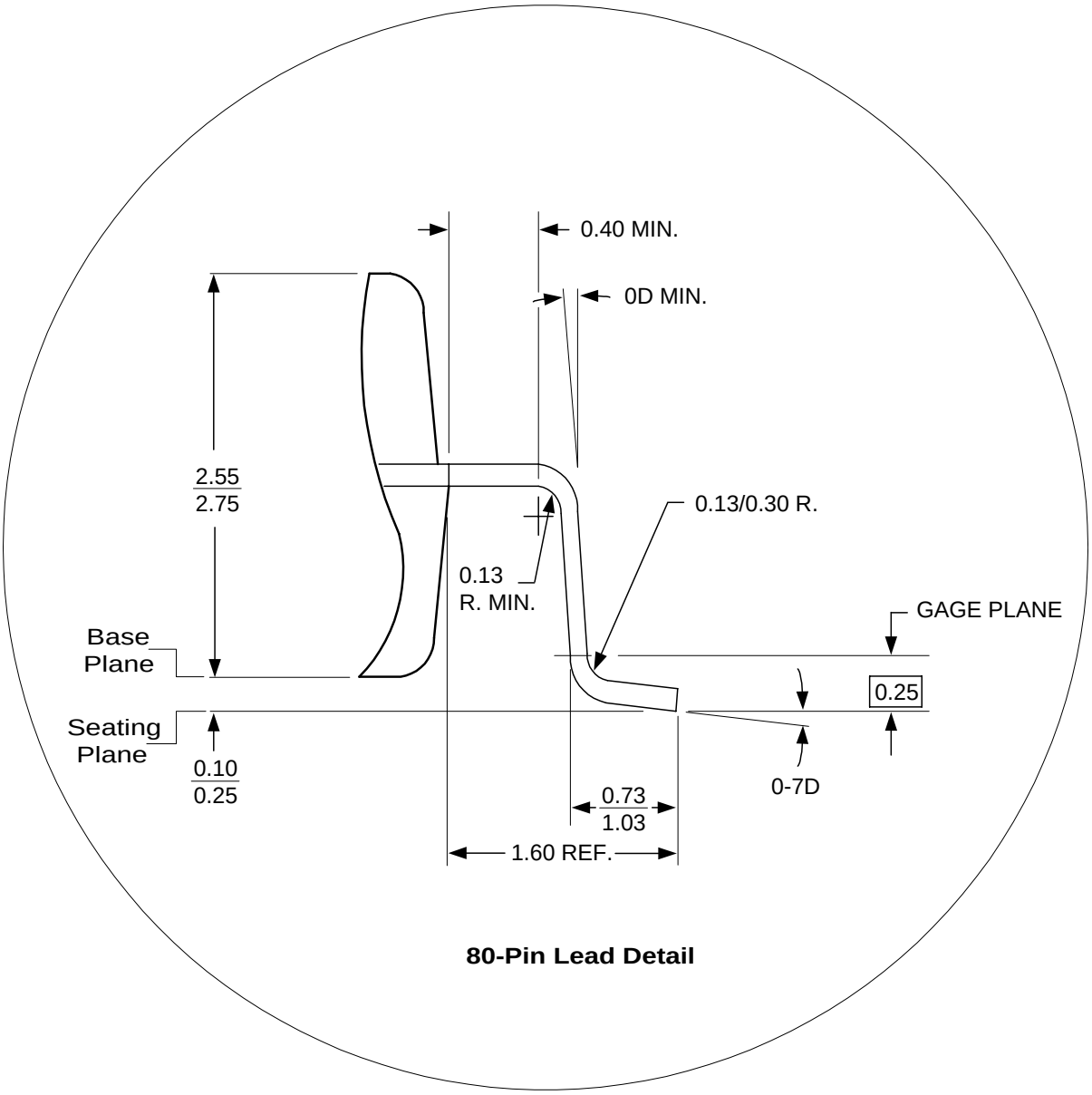


Parameter	Description	Min.	Typ.	Max.	Unit
t_{CL}	CLKOUT Period		41.66		ns
			20.83		ns
t_{SUX}	Sel, Strobe & Data Set-up to External Clock			9	ns
t_{XH}	External Clock to Sel, Strobe & Data Hold Time	2			ns
t_{XFLAG}	External Clock to FIFO Flag			$2t_{CL}$+11	ns

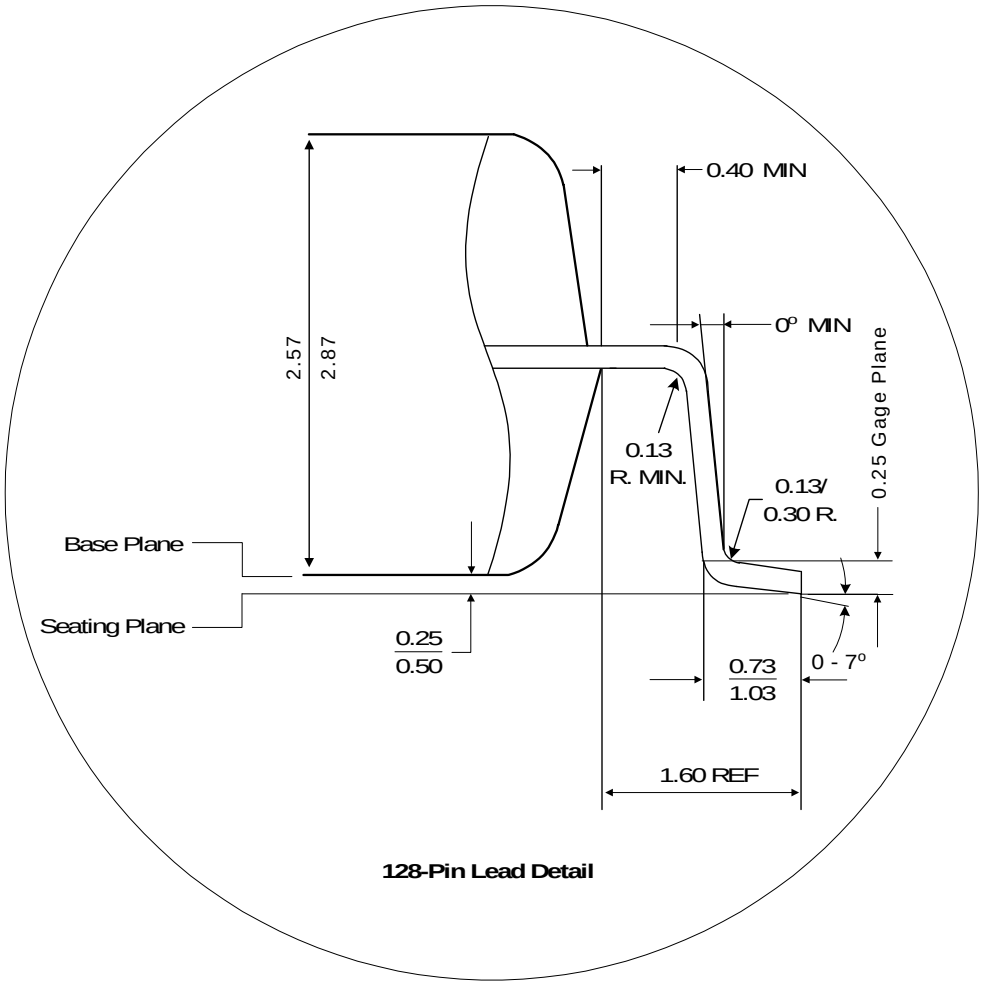




52-Pin Lead Detail



80-Pin Lead Detail



128-Pin Lead Detail

Document Title: CY7C64601/CY7C64603/CY7C64613 EZ USB FX USB Microcontroller Document Number: 38-08005				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110206	11/11/01	SZV	Change from Spec number: 38-00903 to 38-08005