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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C646xx
RAM Size	8K x 8
Interface	I²C, USB, USART
Number of I/O	16
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-PQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64613-52nc

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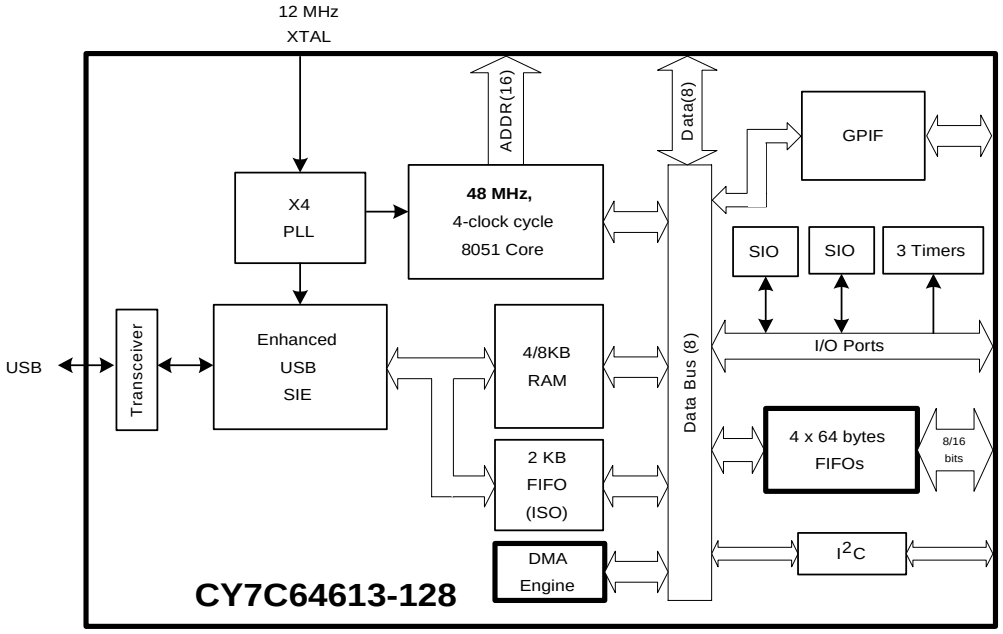
1.0 Features

The CY7C646xx (EZ-USB *FX)* is Cypress Semiconductor's second-generation full-speed USB family. *FX* products offer higher performance and a higher level of integration than first-generation EZ-USB products. The FX builds on the EZ-USB feature set, including an intelligent USB core, enhanced 8051, 8-Kbyte RAM, and high-performance I/O. The CY7C646xx enhances the EZ-USB family by providing faster operation and more ways to transfer data into and out of the chip at very high speed.



1.1 EZ-USB *FX* Features

- **Single-chip integrated USB Transceiver, Serial Interface Engine (SIE), and Enhanced 8051 Microprocessor**
- **Soft: 8051 runs from internal RAM, which is:**
  - **Downloaded via USB, or**
  - **Loaded from EEPROM**
- **14 Bulk/Interrupt endpoints, each with a maximum packet size of 64 bytes**
- **16 Isochronous endpoints, with 2 KB of buffer space (1 KB, double buffered) which may be divided among the sixteen isochronous endpoints**
- **Integrated, industry standard 8051 with enhanced features:**
  - **Four clocks per cycle**
  - **Two UARTS**
  - **Three counter/timers**
  - **Expanded interrupt system**
  - **Two data pointers**
- **3.3-volt operation**
- **Smart Serial Interface Engine (SIE)**
- **Vectored USB interrupts**
- **Separate buffers for the SETUP and DATA portions of a CONTROL transfer**
- **Integrated I^2C™ controller**
- **48-MHz or 24-MHz 8051 operation**
- **Enhanced IO**
  - **IO port registers mapped to SFRs**
  - **Port bits can be controlled using 8051 bit addressing instructions**
- **Four integrated general purpose 8-bit FIFOs**
  - **64 bytes each**
  - **Automatic conversion to and from 16-bit buses**

2.3 Endpoints

Endpoint	Type	Buffer Size
EP0-IN EP0-OUT	Control	64 64
EP1-IN	Bulk/Interrupt	64
EP1-OUT	Bulk/Interrupt	64
EP2-IN	Bulk/Interrupt	64
EP2-OUT	Bulk/Interrupt	64
EP3-IN	Bulk/Interrupt	64
EP3-OUT	Bulk/Interrupt	64
EP4-IN	Bulk/Interrupt	64
EP4-OUT	Bulk/Interrupt	64
EP5-IN	Bulk/Interrupt	64
EP5-OUT	Bulk/Interrupt	64
EP6-IN	Bulk/Interrupt	64
EP6-OUT	Bulk/Interrupt	64
EP7-IN	Bulk/Interrupt	64
EP7-OUT	Bulk/Interrupt	64
EP8-IN	Isochronous	0–1023[1]
EP8-OUT	Isochronous	0–1023[1]
EP9-IN	Isochronous	0–1023[1]
EP9-OUT	Isochronous	0–1023[1]
EP10-IN	Isochronous	0–1023[1]
EP10-OUT	Isochronous	0–1023[1]
EP11-IN	Isochronous	0–1023[1]
EP11-OUT	Isochronous	0–1023[1]
EP12-IN	Isochronous	0–1023[1]
EP12-OUT	Isochronous	0–1023[1]
EP13-IN	Isochronous	0–1023[1]
EP13-OUT	Isochronous	0–1023[1]
EP14-IN	Isochronous	0–1023[1]
EP14-OUT	Isochronous	0–1023[1]
EP15-IN	Isochronous	0–1023[1]
EP15-OUT	Isochronous	0–1023[1]

Note:
1. 1023 FIFO bytes may be divided among all Isochronous endpoints.

The CY7C646xx has Control, Bulk, and Interrupt endpoints which each have 64-byte buffers to accommodate the maximum USB specified packet size, giving the highest USB throughput. One endpoint pair is dedicated to endpoint zero, with separate EP0-IN and EP0-OUT buffers to simplify programming. Fourteen additional 64-byte buffers may be used as Bulk or Interrupt endpoints. These endpoints may also be double-buffered by using an endpoint paring mechanism. Double buffering allows the 8051 to access a packet as another is being transmitted or received over USB. This technique is essential in high-bandwidth applications where NAKs by the USB function would reduce performance.

The CY7C646xx also has sixteen Isochronous (ISO) endpoints which share 1024 bytes of double-buffered endpoint memory (2 KB total). The ISO buffer sizes are programmable within 16-byte increments. The Isochronous endpoint buffers are accessed as FIFOs.

Endpoint data is serviced either directly by the 8051, or moved on or off-chip using the DMA system built into the CY7C646xx. Bulk data is available in 64-byte random-access buffers that can also be addressed as a FIFO using the special AutoPointer feature. Each endpoint has a unique interrupt vector. This allows ISRs (Interrupt Service Routines) automatically to be called with minimum overhead and latency, simply by including the ISR address in an interrupt jump table.

2.4 Default USB Machine

When the CY7C64613 is plugged into USB with no EEPROM attached to its I^2C port (but **with** the SCL and SDA pull-ups installed), the intelligent SIE enumerates as a generic USB device with the following characteristics:

ID bytes (hex)

VID (Vendor ID)	0547
PID (Product ID)	2235
DID (Device ID)	0000

Default Endpoints

Endpoint	Type	Alternate Setting		
		0	**1**	**2**
		Max Packet Size (bytes)		
0	CTL	64	64	64
1 IN	INT	0	16	64
2 IN	BULK	0	64	64
2 OUT	BULK	0	64	64
4 IN	BULK	0	64	64
4 OUT	BULK	0	64	64
6 IN	BULK	0	64	64
6 OUT	BULK	0	64	64
8 IN	ISO	0	16	256
8 OUT	ISO	0	16	256
9 IN	ISO	0	16	16
9 OUT	ISO	0	16	16
10 IN	ISO	0	16	16
10 OUT	ISO	0	16	16

Powering up with default USB characteristics allows code to be written without initial consideration of the enumeration code that establishes the default USB device, speeding the learning process.

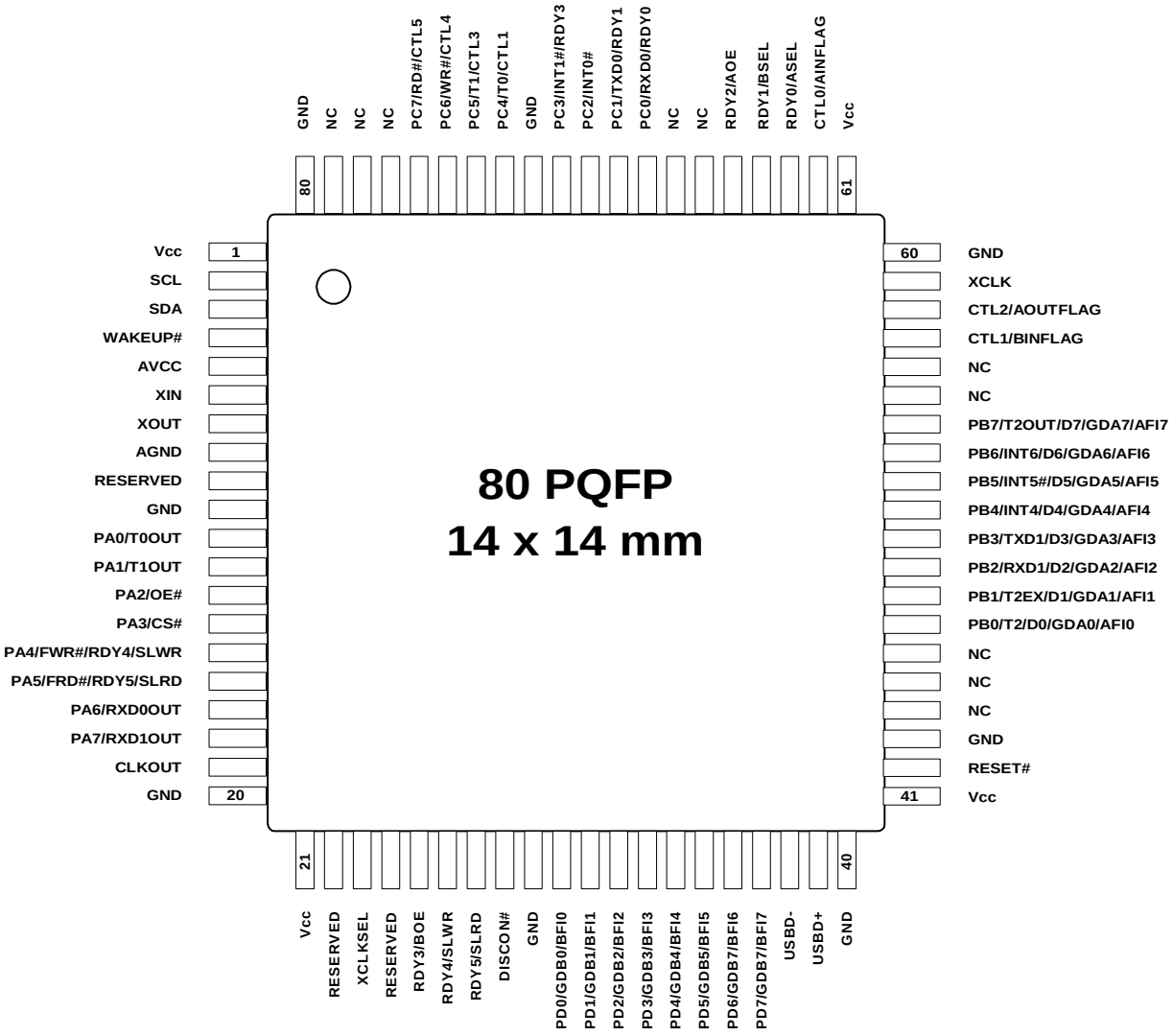
2.5 IBN (In-Bulk-NAK) Interrupts

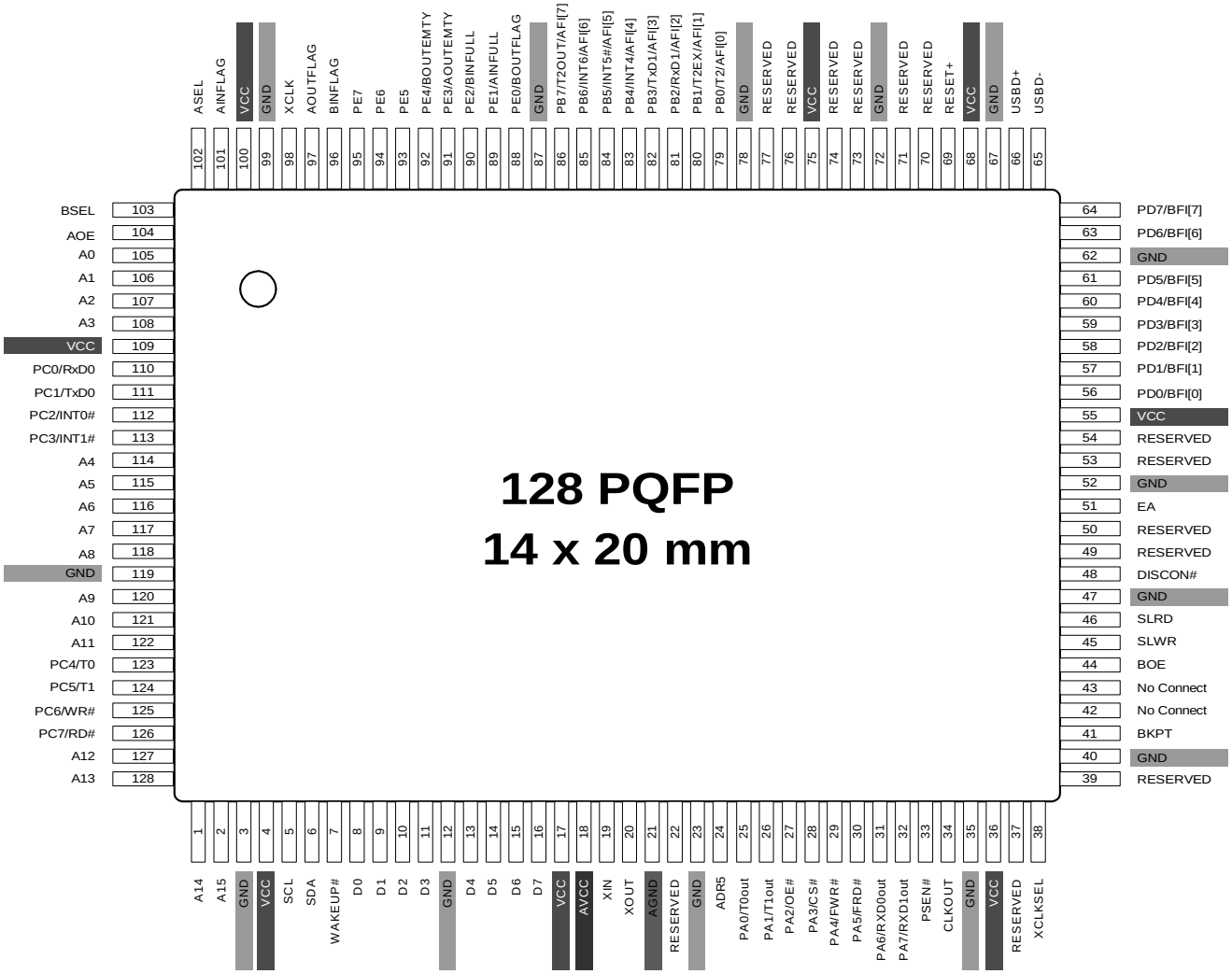
The CY7C646xx has an interrupt that indicates that an IN token has been received by an endpoint, and the SIE has NAK'd the transfer due to no data being available in the endpoint buffer. Interrupt request bits are provided for endpoints EP1N through EP7IN, and a previously reserved vector is added to the USB vectored interrupts.

2.6 Slave FIFOs

Many high-bandwidth USB designs use a FIFO between the USB interface chip and external logic to match data rates, or to smooth the USB data delivery (which, being packet oriented, occurs in bursts). The CY7C646xx moves this glue logic into the part by providing four 64-byte internal slave FIFOs. The FIFOs also provide two important interface functions, external clocking and bus width conversion.

Using external clocking, external logic (such as a DSP or ASIC) can clock data into or out of the slave FIFOs under control of its own clock, rather than synchronizing with the clock supplied by the CY7C646xx (24 or 48 MHz). The FIFOs can be controlled


80 PQFP
14 x 14 mm
1 Vcc
2 SCL
3 SDA
4 WAKEUP#
5 AVCC
6 XIN
7 XOUT
8 AGND
9 RESERVED
10 GND
11 PA0/T0OUT
12 PA1/T1OUT
13 PA2/OE#
14 PA3/CS#
15 PA4/FWR#/RDY4/SLWR
16 PA5/FRD#/RDY5/SLRD
17 PA6/RXD0OUT
18 PA7/RXD1OUT
19 CLKOUT
20 GND
21 Vcc
22 RESERVED
23 XCLKSEL
24 RESERVED
25 RDY3/BOE
26 RDY4/SLWR
27 RDY5/SLRD
28 DISCON#
29 GND
30 PD0/GDB0/BFI0
31 PD1/GDB1/BFI1
32 PD2/GDB2/BFI2
33 PD3/GDB3/BFI3
34 PD4/GDB4/BFI4
35 PD5/GDB5/BFI5
36 PD6/GDB7/BFI6
37 PD7/GDB7/BFI7
38 USBD-
39 USBD+
40 GND
41 Vcc
42 RESET#
43 GND
44 PB0/T2/D0/GDA0/AFI0
45 PB1/T2EX/D1/GDA1/AFI1
46 PB2/RXD1/D2/GDA2/AFI2
47 PB3/TXD1/D3/GDA3/AFI3
48 PB4/INT4/D4/GDA4/AFI4
49 PB5/INT5#/D5/GDA5/AFI5
50 PB6/INT6/D6/GDA6/AFI6
51 PB7/T2OUT/D7/GDA7/AFI7
52 NC
53 NC
54 NC
55 NC
56 XCLK
57 GND
58 CTL0/AINFLAG
59 RDY0/ASEL
60 RDY1/BSEL
61 RDY2/AOE
62 NC
63 NC
64 PC0/RXD0/RDY0
65 PC1/TXD0/RDY1
66 PC2/INT0#
67 PC3/INT1#/RDY3
68 GND
69 PC4/T0/CTL1
70 PC5/T1/CTL3
71 PC6/WR#/CTL4
72 PC7/RD#/CTL5
73 NC
74 NC
75 NC
76 GND
77 CTL1/BINFLAG
78 CTL2/AOUTFLAG
79 NC
80 GND



3.2 CY7C646xx Pin Descriptions

128	80	52	Name	Type	Default	Description
18	5	5	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
21	8	8	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
48	28	18	DISCON#	O/Z	H	**Disconnect**. This pin can drive HIGH, LOW, or float. DISCON# pin floats when the register bit USBCS.2 is LOW, and drives when it is HIGH. The drive level of the DISCON# pin is the invert of register bit USBCS.3. The DISCON# pin is normally connected to the USB D+ line through a 1500Ω resistor. The CY7C646xx signals a USB connection by setting USBCS.3=0 (drive 3.3V) and USBCS.2=1 (output enable). The CY7C646xx signals a USB disconnect by setting USBCS.2=0 which floats the pin and disconnects the 1500Ω resistor from D+.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
82	50	32	PB3 or TXD1 or D[3] or GDA[3] or AFI [3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.3 and IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **TXD1**is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode. **AFI [3]** is the bidirectional A-FIFO data bus.
83	51	33	PB4 or INT4 or D[4] or GDA[4] or AFI [4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.4 and IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH. **AFI [4]** is the bidirectional A-FIFO data bus.
84	52	34	PB5 or INT5# or D[5] or GDA[5] or AFI [5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.5 and IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW. **AFI [5]** is the bidirectional A-FIFO data bus.
85	53	35	PB6 or INT6 or D[6] or GDA[6] or AFI [6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.6 and IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **INT6** is the 8051 INT5 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH. **AFI [6]** is the bidirectional A-FIFO data bus.
86	54	36	PB7 or T2OUT or D[7] or GDA[7] or AFI [7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: PORTBCFG.7 and IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **T2OUT** is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows. **AFI [7]** is the bidirectional A-FIFO data bus.
Port C						
110	68	43	PC0 or RXD0 or RDY0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by the PORTCCFG.0 and PORTCGPIF.0 bits. **PC0** is a bidirectional I/O port pin. **RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes. **RDY0** is a GPIF input signal.
111	69	44	PC1 or TXD0 or RDY1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by the PORTCCFG.1 and PORTCGPIF.1 bits. **PC1** is a bidirectional I/O port pin. **TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. **RDY1** is a GPIF input signal.
112	70	45	PC2 or INT0#	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by the PORTCCFG.2 bit. **PC2** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
113	71	46	PC3 or INT1# or RDY3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by the: PORTCCFG.3 and PORTCGPIF.3 bits. **PC3** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0). **RDY3** is a GPIF input signal.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
123	73	48	PC4 or T0 or CTL1	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by the PORTCCFG.4 and PORTCGPIF.4 bits. **PC4** is a bidirectional I/O port pin. **T0** is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit. **CTL1** is a GPIF output signal.
124	74	49	PC5 or T1 or CTL3	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by the PORTCCFG.5 and PORTCGPIF.5 bits. **PC5** is a bidirectional I/O port pin. **T1** is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit. **CTL3** is a GPIF output signal.
125	75	50	PC6 or WR# or CTL4	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by the PORTCCFG.6 and PORTCGPIF.6 bits. **PC6** is a bidirectional I/O port pin. **WR#** is the active-LOW write strobe output for external memory. If the WR# signal is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on. **CTL4** is a GPIF output signal.
126	76	51	PC7 or RD# or CTL5	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by the PORTCCFG.7 and PORTCGPIF.7 bits. **PC7** is a bidirectional I/O port pin. **RD#** is the active-LOW read strobe output for external memory. If the RD# signal is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on. **CTL5** is a GPIF output signal.
Port D						
						Port D is multiplexed between three sources: **PD0–PD7** are bidirectional I/O port pins. **GDB[7..0]** is the GPIF B data bus. **BFI[7..0]** is the bidirectional B-FIFO data bus.
56	30		PD0 or GDB[0] or BFI [0]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [0]** is the bidirectional B-FIFO data bus.
57	31		PD1 or GDB[1] or BFI [1]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [1]** is the bidirectional B-FIFO data bus.
58	32		PD2 or GDB[2] or BFI [2]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [2]** is the bidirectional B-FIFO data bus.
59	33		PD3 or GDB[3] or BFI [3]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [3]** is the bidirectional B-FIFO data bus.
60	34		PD4 or GDB[4] or BFI [4]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [4]** is the bidirectional B-FIFO data bus.
61	35		PD5 or GDB[5] or BFI [5]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [5]** is the bidirectional B-FIFO data bus.
63	36		PD6 or GDB[6] or BFI [6]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[2..0] bits. **BFI [6]** is the bidirectional B-FIFO data bus.

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
104	65	42	RDY2 or AOE	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY2** is a GPIF input signal. **AOE** is the output enable input for the A-OUT FIFO.
44	25		RDY3 or BOE	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY3** is a GPIF input signal. **BOE** is the output enable input for the B-OUT FIFO.
45	26		RDY4 or SLWR	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY4** is a GPIF input signal. **SLWR** is the input-only write strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
46	27		RDY5 or SLRD	Input	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY5** is a GPIF input signal. **SLRD** is the input-only read strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
101	62	41	CTL0 or AINFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL0** is a GPIF control output. **AINFLAG** is the A-IN FIFO flag output which indicates a programmable level of FIFO fullness.
96	57		CTL1 or BINFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL1** is a GPIF control output. **BINFLAG** is the B-IN FIFO flag output which indicates a programmable level of FIFO fullness.
97	58	37	CTL2 or AOUTFLAG	Output	X	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL2** is a GPIF control output. **AOUTFLAG** is the A-OUT FIFO flag output which indicates a programmable level of FIFO fullness.
98	59	38	XCLK	Input	N/A	External clock input, used for synchronously clocking data into the slave FIFOs. XCLK also serves as a timing reference for all slave FIFO control signals and GPIF.
53		22	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
54		23	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
70			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
71			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
73			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
74			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
76			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
77			Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
50		20	Reserved	Rsrvd	N/A	Reserved. Leave open.
49		19	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
7	4	4	WAKEUP#	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, a HIGH-to-LOW edge on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP# LOW inhibits the EZ-USB chip from suspending.
5	2	2	SCL	OD	Z	**I^2C Clock**. Connect to V_{CC} with a 1K resistor, **even if no I^2C peripheral is attached.**

3.2 CY7C646xx Pin Descriptions (continued)

128	80	52	Name	Type	Default	Description
6	3	3	SDA	OD	Z	**I^2C Data**. Connect to V_{CC} with a 1K resistor, **even if no I^2C peripheral is attached.**
38	23	16	XCLKSEL	Input	N/A	HIGH: Use XCLK pin for GPIF and slave FIFOs. LOW: Use internal 48-MHz clock for GPIF and slave FIFOs.
39	24	17	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
37	22	15	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
22	9	9	Reserved	Rsrvd	N/A	Reserved. Connect to Ground.
4	1	1	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
17			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
36	21	14	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
55			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
68	41	27	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
75			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
100	61	40	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
109			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3 V power source.
3	80	52	GND	Ground	N/A	Ground.
12			GND	Ground	N/A	Ground.
23	10		GND	Ground	N/A	Ground.
35	20	13	GND	Ground	N/A	Ground.
40			GND	Ground	N/A	Ground.
47			GND	Ground	N/A	Ground.
52	29	21	GND	Ground	N/A	Ground.
62			GND	Ground	N/A	Ground.
67	40	26	GND	Ground	N/A	Ground.
72	43		GND	Ground	N/A	Ground.
78			GND	Ground	N/A	Ground.
87			GND	Ground	N/A	Ground.
99	60	39	GND	Ground	N/A	Ground.
119	72	47	GND	Ground	N/A	Ground.
42	79		NC	N/A	N/A	No-connect. This pin must be left open.
43	44		NC	N/A	N/A	No-connect. This pin must be left open.
	45		NC	N/A	N/A	No-connect. This pin must be left open.
	46		NC	N/A	N/A	No-connect. This pin must be left open.
	55		NC	N/A	N/A	No-connect. This pin must be left open.
	56		NC	N/A	N/A	No-connect. This pin must be left open.
	66		NC	N/A	N/A	No-connect. This pin must be left open.
	67		NC	N/A	N/A	No-connect. This pin must be left open.
	77		NC	N/A	N/A	No-connect. This pin must be left open.
	78		NC	N/A	N/A	No-connect. This pin must be left open.

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
781D	ABPOLAR	FIFO Control Signals Polarity	0	0	BOE	AOE	SLRD	SLWR	ASEL	BSEL
781E	ABFLUSH	Write (data=x) to reset all flags	*	*	*	*	*	*	*	*
781F-7823 (reserved)										
7824	WFSELECT	Waveform Selector	SINGLEWR		SINGLERD		FIFOWR		FIFORD	
7825	IDLE_CS	GPIF IDLE State control	DONE	0	0	0	0	0	0	IDLEDRV
7826	IDLECTLOUT	GPIF IDLE CTL states	IOE3	IOE2	IOE1/ CTL5	IOE0/ CTL4	CTL3	CTL2	CTL1	CTL0
7827	CTLOUTCFG	GPIF CTL Drive mode	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0
7828-7829 (reserved)										
782A	GPIFADRL	GPIF Address	*	*	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
782B (reserved)										
782C	AINTC	FIFO A In Transfer Count	FITC	Transfer Count						
782D	AOUTTC	FIFO A Out Transfer Count	FITC	Transfer Count						
782E	ATRIG	Trigger a FIFO A RD/WR	*	*	*	*	*	*	*	*
782F (reserved)										
7830	BINTC	FIFO B In Transfer Count	FITC	Transfer Count						
7831	BOUTTC	FIFO B Out Transfer Count	FITC	Transfer Count						
7832	BTRIG	Trigger a FIFO B RD/WR	*	*	*	*	*	*	*	*
7833 (reserved)										
7834	SGLDATH	GPIF Data High	D15	D14	D13	D12	D11	D10	D9	D8
7835	SGLDATLTRIG	GPIF Data Low and Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7836	SGLDATLN-TRIG	GPIF Data Low and No Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7837(reserved)										
7838	READY	GPIF Ready flags	INTRDY	SAS	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
7839	ABORT	Abort current GPIF cycle	*	*	*	*	*	*	*	*
783A (reserved)										
783B	GENIE	GPIF/DMA Interrupt Enable	0	0	0	0	0	DMADN	GPWR	GPDONE
783C	GENIRQ	GPIF/DMA Interrupt Request	0	0	0	0	0	DMADN	GPWR	GPDONE
783D-7840 (reserved)										
	IO Ports D, E									
7841	OUTD	Output Port D	OUTD7	OUTD6	OUTD5	OUTD4	OUTD3	OUTD2	OUTD1	OUTD0
7842	PINSD	Input Port D pins	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
7843	OED	Port D Output Enable	0ED7	0ED6	0ED5	0ED4	0ED3	0ED2	0ED1	0ED0
7844 (reserved)										
7845	OUTE	Output Port E	OUTE7	OUTE6	OUTE5	OUTE4	OUTE3	OUTE2	OUTE1	OUTE0
7846	PINSE	Input Port E pins	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0
7847	OEE	Port E Output Enable	OEE7	OEE6	OEE5	OEE4	OEE3	OEE2	OEE1	OEE0
7848 (reserved)										
7849	PORTSETUP	Timer0 Clock source, Port-to-SFR mapping	0	0	0	0	0	0	T0CLK	SFRPORT
784A	IFCONFIG	Select 8/16 bit data bus, configure buses (IF)	52ONE	0	0	0	GSTATE	BUS16	IF1	IF0
784B	PORTACF2	Port A Configuration #2	0	0	SLRD	SLWR	0	0	0	0

4.0 Register Summary (continued)

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
	Isochronous Byte Counts									
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F80-7F91 (reserved)										
	CPU Registers									
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	24/48	CLKINV	CLKOUT OE	8051RES
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
	Input-Output Port Registers									
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0

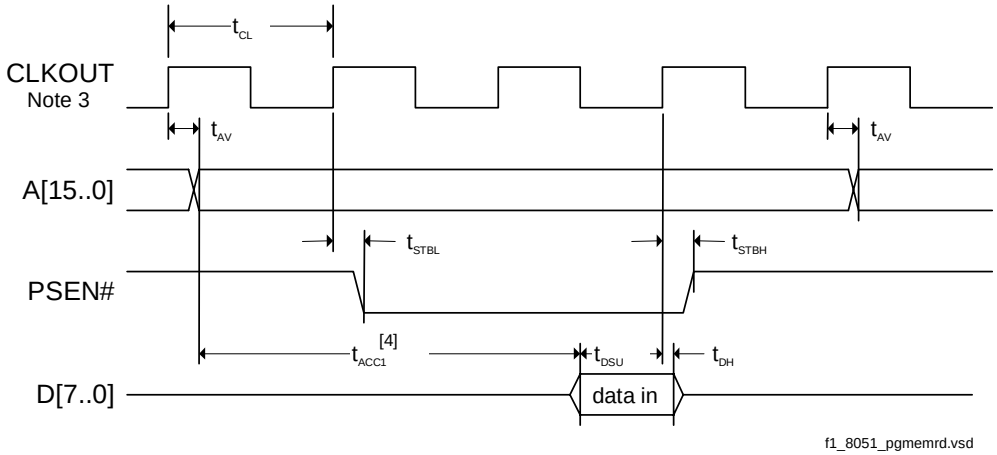
9.0 AC Electrical Characteristics

9.1 USB Transceiver

Specified Conditions: Per Table 7-6 of Revision 1.1 of USB specification

Parameter	Description	Condition	Min.	Max.	Unit
Trise	Rise and Fall Times Full Speed		4	20	ns
Tfall			4	20	ns
t_{RFM}	Rise/Fall Time Matching		90	110	%
Vcr	Crossover Point		1.3	2.0	V

9.2 Program Memory Read



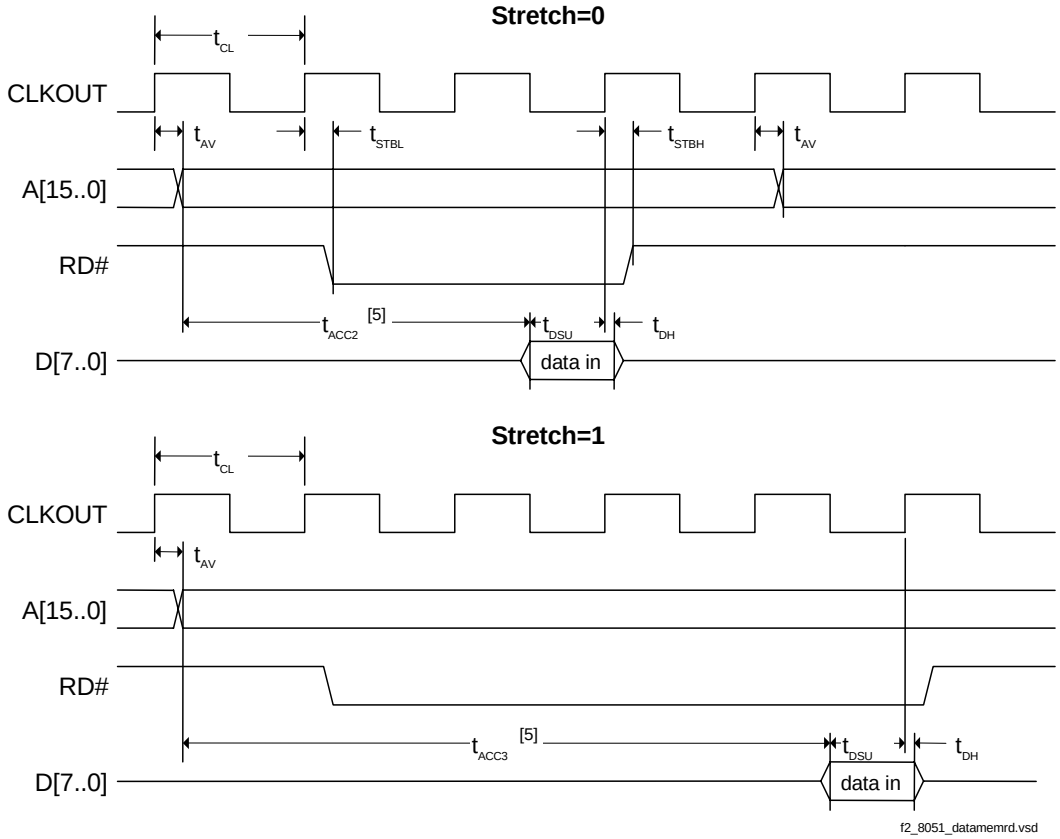
f1_8051_pgmemrd.vsd

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to PSEN Low	0		8	ns	
t_{STBH}	Clock to PSEN High	0		8	ns	
t_{DSU}	Data Set-up to Clock			10	ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

3. CLKOUT is shown with positive polarity.
4. t_{ACC1} is computed from the above parameters as follows:
   t_{ACC1}(24 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 106 ns
   t_{ACC1}(48 Mhz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 44 ns

9.3 Data Memory Read



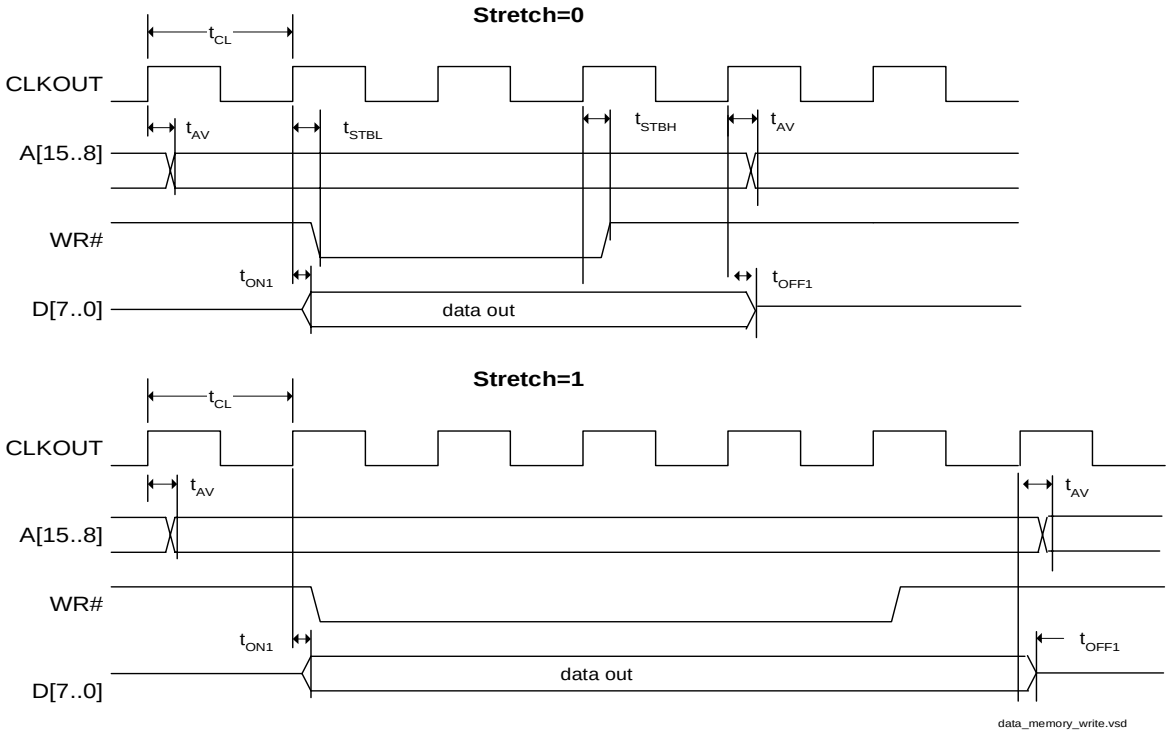
Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to RD Low	0		8	ns	
t_{STBH}	Clock to RD High	0		8	ns	
t_{DSU}	Data Set-up to Clock			10	ns	
t_{DH}	Data Hold Time	0			ns	

Note:

5. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:
   t_{ACC2}(24 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 106 ns
   t_{ACC2}(48 Mhz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 44 ns

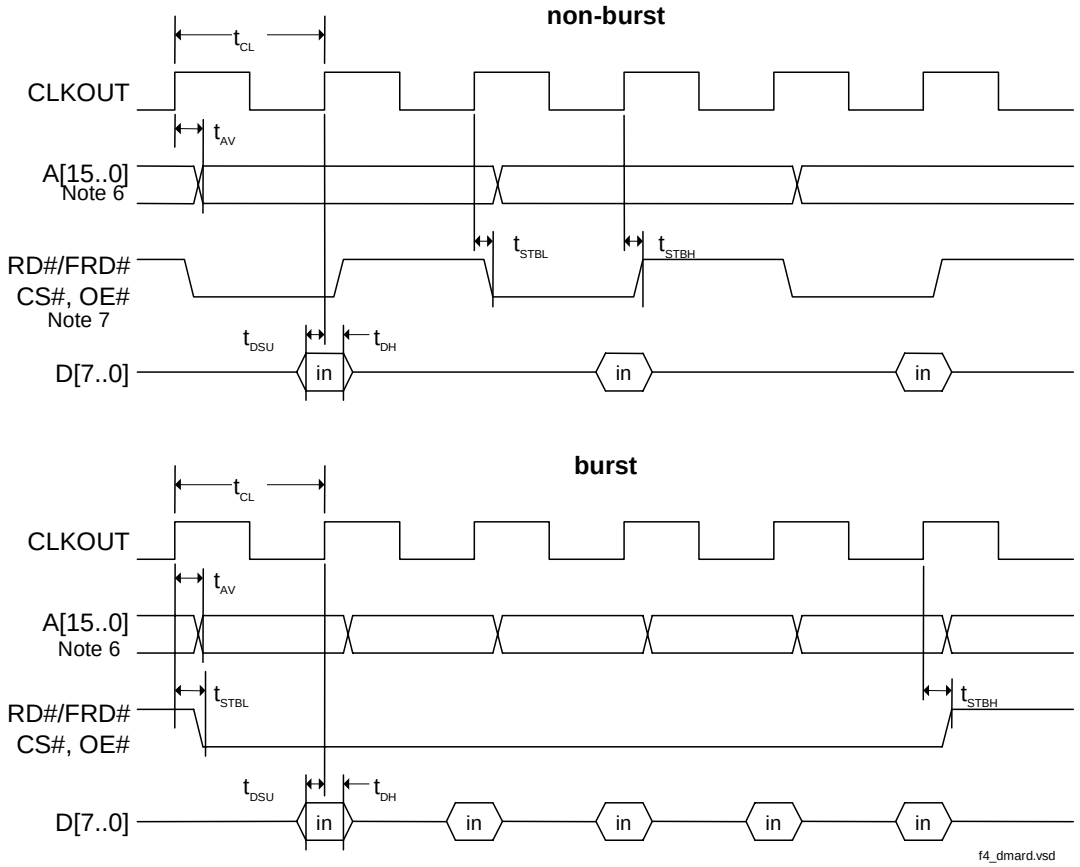
   t_{ACC3}(24 MHz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 188 ns
   t_{ACC3}(48 Mhz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 85 ns

9.4 Data Memory Write



Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to WR Pulse Low	0	8	ns	
t_{STBH}	Clock to WR Pulse High	0	8	ns	
t_{ON1}	Clock to Data Turn-on	0	7	ns	
t_{OFF1}	Clock to Data Hold Time	–2	7	ns	

9.5 DMA Read

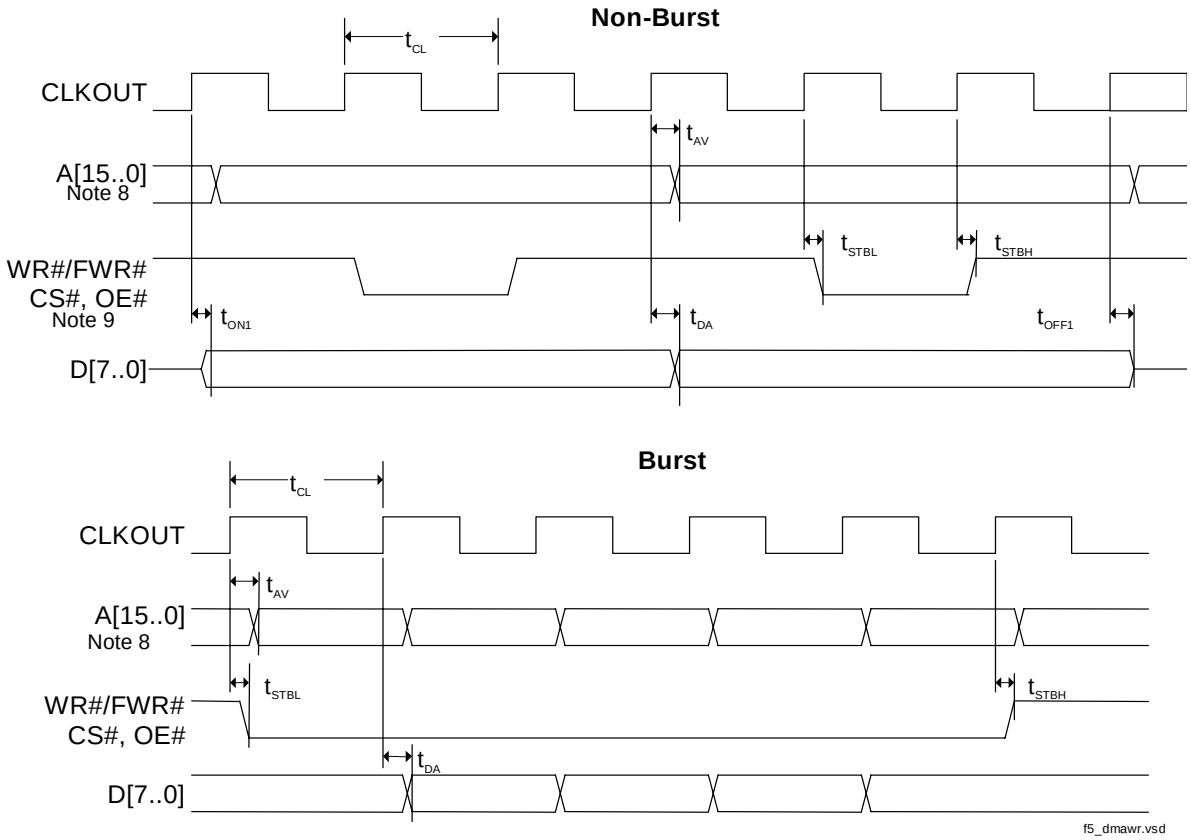


Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to Strobe Low	0	8	ns	Non-burst
t_{STBH}	Clock to Strobe High	0	8	ns	Non-burst
t_{DSU}	Data to Clock Set-up		10	ns	
t_{DH}	Clock to Data Hold	0		ns	

Notes:

6. The address bus is not used in external FIFO transfers that use FRD#.
7. This is the maximum data rate. The strobes are programmable for longer access times.

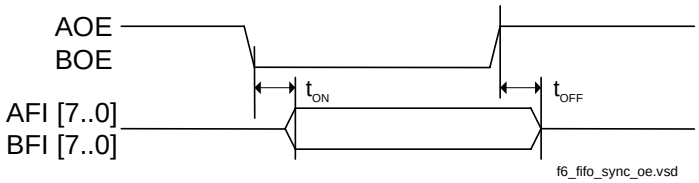
9.6 DMA Write



Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Clock to Address Valid	0	10	ns	
t_{STBL}	Clock to Strobe Low	0	8	ns	Non-burst
t_{STBH}	Clock to Strobe High	0	8	ns	Non-burst
t_{DA}	Clock to Valid Data		12	ns	
t_{ON1}	Clock to Data Turn-on	0	7	ns	
t_{OFF1}	Clock to Data Hold Time	–2	7	ns	

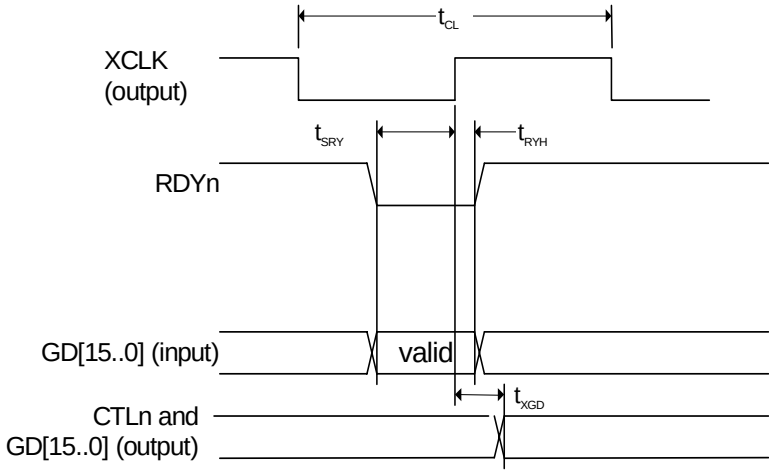
Notes:
8. The address bus in not used in external FIFO transfers (FWR# strobe).
9. This is the maximum data rate. The WR/FWR pulses are programmable for longer access times.

9.7 Slave FIFOs—Output Enables



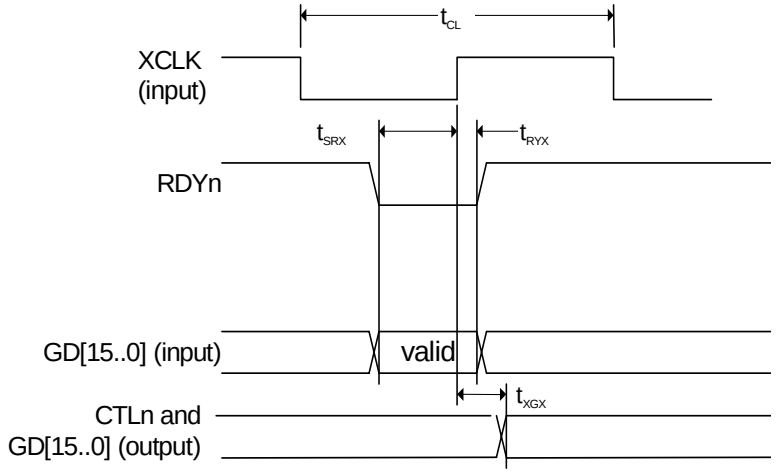
Parameter	Description	Min.	Max.	Unit
t_{ON}	FIFO Data Bus Turn-on Time	0	10	ns
t_{OFF}	FIFO Data Bus Turn-off Time	0	10	ns

9.12 GPIF Signals (Internally Clocked)



Parameter	Description	Min.	Max.	Unit
t_{SRY}	RDYn and GPIF Data to External Clock Set-up Time		9	ns
t_{RYH}	External Clock to RDYn and GPIF Data Hold Time	2		ns
t_{XGD}	Clock to GPIF Data and CTLn output		13	ns

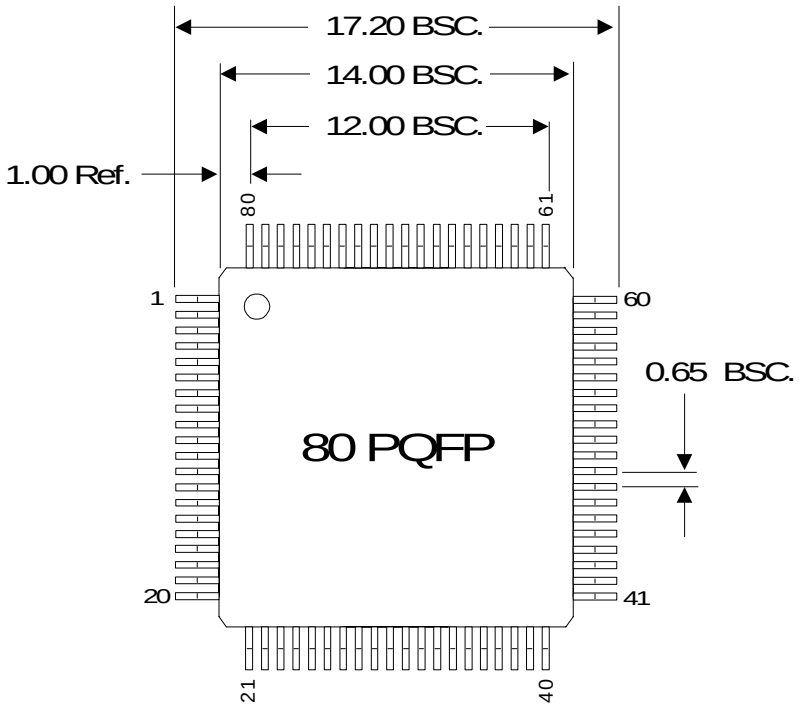
9.13 GPIF Signals (Externally Clocked)

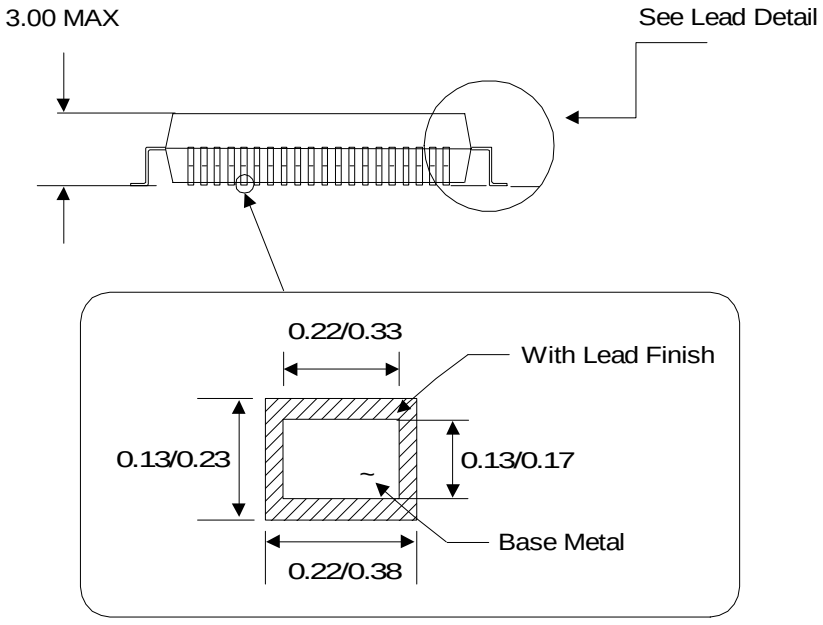


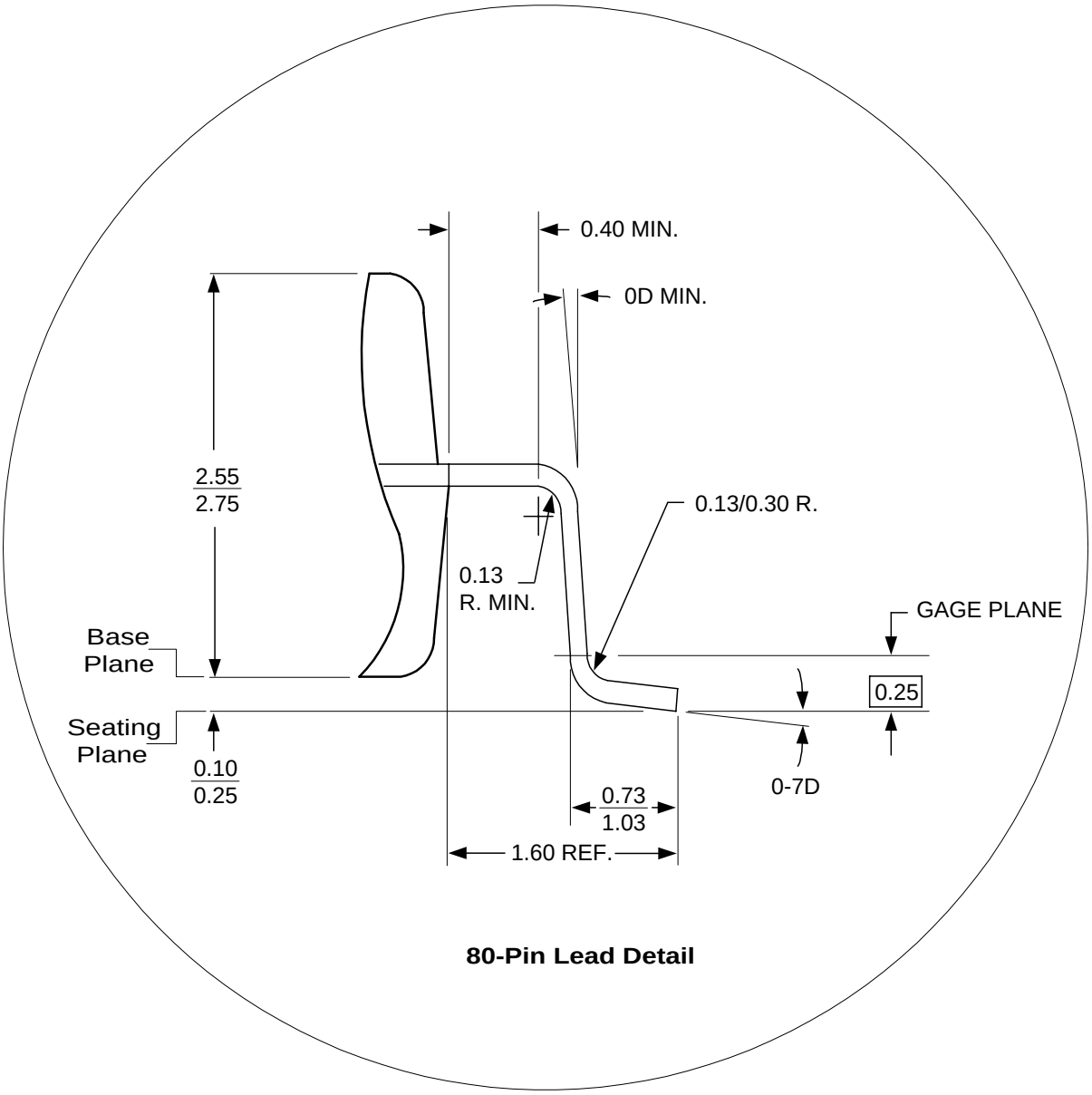
Parameter	Description	Min.	Max.	Unit
t_{SRX}	RDYn and GPIF Data to External Clock Set-up Time		9	ns
t_{RYX}	External Clock to RDYn and GPIF Data Hold Time	2		ns
t_{XGX}	Clock to GPIF Data and CTLn output		13	ns

Note:
13. t_{cl} for an XCLK input must be greater than 20.83 ns.

11.2 80 PQFP


17.20 BSC.
14.00 BSC.
12.00 BSC.
1.00 Ref.
80
61
1
60
0.65 BSC.
80 PQFP
20
41
21
40


3.00 MAX
See Lead Detail
0.22/0.33
With Lead Finish
0.13/0.23
0.13/0.17
Base Metal
0.22/0.38



80-Pin Lead Detail